



# F100302

## Low Power Quint 2-Input OR/NOR Gate

### General Description

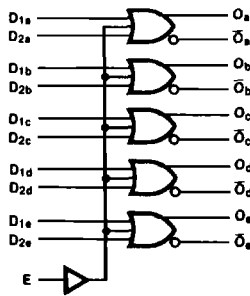
The F100302 is a monolithic quint 2-input OR/NOR gate with common enable. All inputs have 50 kΩ pull-down resistors and all outputs are buffered.

### Features

- 43% power reduction of the F100102
- 2000V ESD protection
- Pin/function compatible with F100102
- Voltage compensated operating range = -4.2V to -5.7V

**Ordering Code:** See Section 8

### Logic Symbol



TL/F/10580-1

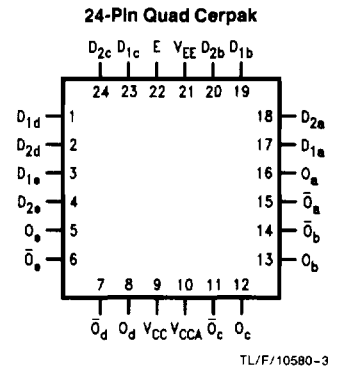
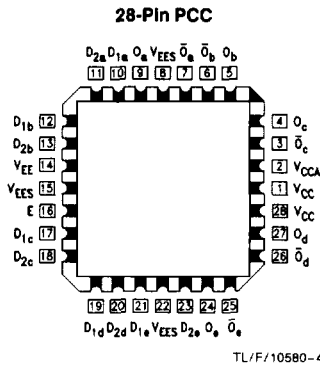
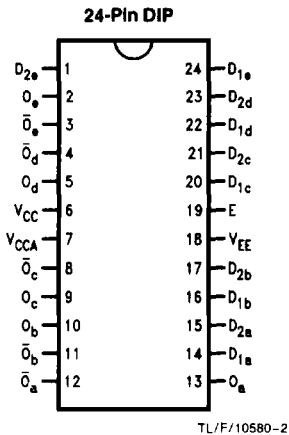
Pin Names	Description
D <sub>na</sub> -D <sub>ne</sub>	Data Inputs
E	Enable Input
O <sub>a</sub> -O <sub>e</sub>	Data Outputs
$\bar{O}_a$ - $\bar{O}_e$	Complementary Data Outputs

### Truth Table

D <sub>1X</sub>	D <sub>2X</sub>	E	O <sub>X</sub>	$\bar{O}_X$
L	L	L	L	H
L	L	H	H	L
L	H	L	H	L
L	H	H	H	L
H	L	L	H	L
H	L	H	H	L
H	H	L	H	L
H	H	H	H	L

H = HIGH Voltage Level  
L = LOW Voltage Level

### Connection Diagrams



## Absolute Maximum Ratings

Above which the useful life may be impaired (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature ( $T_{STG}$ ) -65°C to +150°C

Maximum Junction Temperature ( $T_J$ )  
 Ceramic +175°C  
 Plastic +150°C

$V_{EE}$  Pin Potential to Ground Pin -7.0V to +0.5V

Input Voltage (DC)  $V_{EE}$  to +0.5V

Output Current (DC Output HIGH) -50 mA

ESD (Note 2)  $\geq 2000V$

## Recommended Operating Conditions

Case Temperature ( $T_C$ )

Commercial 0°C to +85°C  
 Military -55°C to +125°C

Supply Voltage ( $V_{EE}$ )

Commercial -5.7V to -4.2V  
 Military -5.7V to -4.2V

## Commercial Version

### DC Electrical Characteristics

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $T_C = 0^\circ C$  to  $+85^\circ C$  (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
$V_{OH}$	Output HIGH Voltage	-1025	-955	-870	mV	$V_{IN} = V_{IH(Max)}$ or $V_{IL(Min)}$	Loading with 50 $\Omega$ to -2.0V
$V_{OL}$	Output LOW Voltage	-1830	-1705	-1620	mV		
$V_{OHC}$	Output HIGH Voltage	-1035			mV	$V_{IN} = V_{IH(Min)}$ or $V_{IL(Max)}$	Loading with 50 $\Omega$ to -2.0V
$V_{OLC}$	Output LOW Voltage			-1610	mV		
$V_{IH}$	Input HIGH Voltage	-1165		-870	mV	Guaranteed HIGH Signal for All Inputs	
$V_{IL}$	Input LOW Voltage	-1830		-1475	mV	Guaranteed LOW Signal for All Inputs	
$I_{IL}$	Input LOW Current	0.50			$\mu A$	$V_{IN} = V_{IL(Min)}$	
$I_{IH}$	Input HIGH Current			240	$\mu A$	$V_{IN} = V_{IH(Max)}$	
$I_{EE}$	Power Supply Current	-45	-36	-20	mA	Inputs Open	

**Note 1:** Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** ESD testing conforms to MIL-STD-883, Method 3015.

**Note 3:** The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

### Ceramic Dual-In-Line Package AC Electrical Characteristics

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = 0^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
$t_{PLH}$ $t_{PHL}$	Propagation Delay Data to Output	0.50	1.15	0.50	1.15	0.50	1.25	ns	Figures 1 and 2 (Note 1)
$t_{PLH}$ $t_{PHL}$	Propagation Delay Enable to Output	1.10	1.90	1.10	1.90	1.20	2.00	ns	
$t_{TLH}$ $t_{THL}$	Transition Time 20% to 80%, 80% to 20%	0.40	1.20	0.40	1.20	0.40	1.20	ns	Figures 1 and 2

**Note 1:** The propagation delay specified is for single output switching. Delays may vary up to 100 ps with multiple outputs switching.

**Commercial Version (Continued)****PCC and Cerpak AC Electrical Characteristics**

$$V_{EE} = -4.2V \text{ to } -5.7V, V_{CC} = V_{CCA} = GND$$

Symbol	Parameter	T <sub>C</sub> = 0°C		T <sub>C</sub> = +25°C		T <sub>C</sub> = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Data to Output	0.50	1.05	0.50	1.05	0.50	1.15	ns	Figures 1 and 2 (Note 2)
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Enable to Output	1.10	1.80	1.10	1.80	1.20	1.90	ns	
t <sub>TLH</sub> t <sub>THL</sub>	Transition Time 20% to 80%, 80% to 20%	0.40	1.10	0.40	1.10	0.40	1.10	ns	Figures 1 and 2
t <sub>S, G-G</sub>	Skew, Gate to Gate	TBD		TBD		TBD		ps	PCC Only (Note 1)

**Note 1:** Gate to gate skew is defined as the difference in propagation delays between each of the outputs.

**Note 2:** The propagation delay specified is for single output switching. Delays may vary up to 100 ps with multiple outputs switching.

**Military Version—Preliminary****DC Electrical Characteristics**

$$V_{EE} = -4.2V \text{ to } -5.7V, V_{CC} = V_{CCA} = GND, T_C = -55^\circ\text{C to } +125^\circ\text{C (Note 3)}$$

Symbol	Parameter	Min	Max	Units	T <sub>C</sub>	Conditions	Notes	
V <sub>OH</sub>	Output HIGH Voltage	-1025	-870	mV	0°C to +125°C	V <sub>IN</sub> = V <sub>IH(Max)</sub> or V <sub>IL</sub> (Min)	Loading with 50Ω to -2.0V	1, 2, 3
		-1085	-870	mV	-55°C			
V <sub>OL</sub>	Output LOW Voltage	-1830	-1620	mV	0°C to +125°C	V <sub>IN</sub> = V <sub>IH(Max)</sub> or V <sub>IL</sub> (Min)	Loading with 50Ω to -2.0V	1, 2, 3
		-1830	-1555	mV	-55°C			
V <sub>OHC</sub>	Output HIGH Voltage	-1035		mV	0°C to +125°C	V <sub>IN</sub> = V <sub>IH(Max)</sub> or V <sub>IL</sub> (Min)	Loading with 50Ω to -2.0V	1, 2, 3
		-1085		mV	-55°C			
V <sub>OLC</sub>	Output LOW Voltage		-1610	mV	0°C to +125°C	V <sub>IN</sub> = V <sub>IH(Max)</sub> or V <sub>IL</sub> (Min)	Loading with 50Ω to -2.0V	1, 2, 3
			-1555	mV	-55°C			
V <sub>IH</sub>	Input HIGH Voltage	-1165	-870	mV	-55°C to +125°C	Guaranteed HIGH Signal for All Inputs	1, 2, 3, 4	
V <sub>IL</sub>	Input LOW Voltage	-1830	-1475	mV	-55°C to +125°C	Guaranteed LOW Signal for All Inputs	1, 2, 3, 4	
I <sub>IL</sub>	Input LOW Current	0.50		μA	-55°C to +125°C	V <sub>EE</sub> = -5.7V V <sub>IN</sub> = V <sub>IH</sub> (Max)	1, 2, 3	
I <sub>IH</sub>	Input HIGH Current		240	μA	0°C to +125°C	V <sub>EE</sub> = -4.2V V <sub>IN</sub> = V <sub>IL</sub> (Min)	1, 2, 3	
			340	μA	-55°C			
I <sub>EE</sub>	Power Supply Current	-48	-17	mA	-55°C to +125°C	Inputs Open	1, 2, 3	

**Note 1:** F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals -55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

**Note 2:** Screen tested 100% on each device at -55°C, +25°C, and +125°C, Subgroups 1, 2, 3, 7, and 8.

**Note 3:** Sample tested (Method 5005, Table I) on each manufactured lot at -55°C, +25°C, and +125°C, Subgroups A1, 2, 3, 7, and 8.

**Note 4:** Guaranteed by applying specified input condition and testing V<sub>OH</sub>/V<sub>OL</sub>.

**Military Version—Preliminary** (Continued)**Ceramic Dual-In-Line Package AC Electrical Characteristics** $V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$ 

Symbol	Parameter	$T_C = -55^\circ\text{C}$		$T_C = +25^\circ\text{C}$		$T_C = +125^\circ\text{C}$		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
$t_{PLH}$ $t_{PHL}$	Propagation Delay Data to Output	0.30	1.80	0.40	1.50	0.40	1.70	ns	Figures 1 and 2	1, 2, 3, 5
$t_{PLH}$ $t_{PHL}$	Propagation Delay Enable to Output	0.60	2.60	0.80	2.30	0.80	2.80	ns		
$t_{TLH}$ $t_{THL}$	Transition Time 20% to 80%, 80% to 20%	0.30	1.20	0.30	1.20	0.30	1.20	ns		4

**Cerpak AC Electrical Characteristics** $V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$ 

Symbol	Parameter	$T_C = -55^\circ\text{C}$		$T_C = +25^\circ\text{C}$		$T_C = +125^\circ\text{C}$		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
$t_{PLH}$ $t_{PHL}$	Propagation Delay Data to Output	0.30	1.60	0.40	1.30	0.40	1.50	ns	Figures 1 and 2	1, 2, 3, 5
$t_{PLH}$ $t_{PHL}$	Propagation Delay Enable to Output	0.60	2.40	0.80	2.10	0.80	2.60	ns		
$t_{TLH}$ $t_{THL}$	Transition Time 20% to 80%, 80% to 20%	0.30	1.10	0.30	1.10	0.30	1.10	ns		4

**Note 1:** F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals  $-55^\circ\text{C}$ ), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

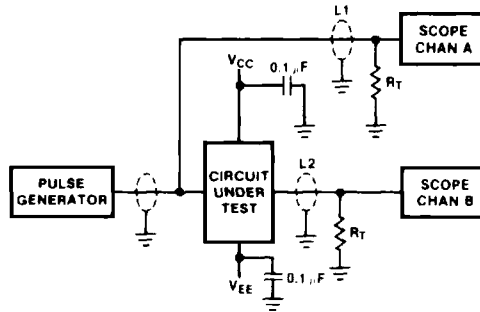
**Note 2:** Screen tested 100% on each device at  $+25^\circ\text{C}$  temperature only, Subgroup A9.

**Note 3:** Sample tested (Method 5005, Table I) on each manufactured lot at  $+25^\circ\text{C}$ , Subgroup A9, and at  $+125^\circ\text{C}$  and  $-55^\circ\text{C}$  temperatures, Subgroups A10 and A11.

**Note 4:** Not tested at  $+25^\circ\text{C}$ ,  $+125^\circ\text{C}$ , and  $-55^\circ\text{C}$  temperature (design characterization data).

**Note 5:** The propagation delay specified is for single output switching. Delays may vary up to 100 ps with multiple outputs switching.

# Test Circuitry



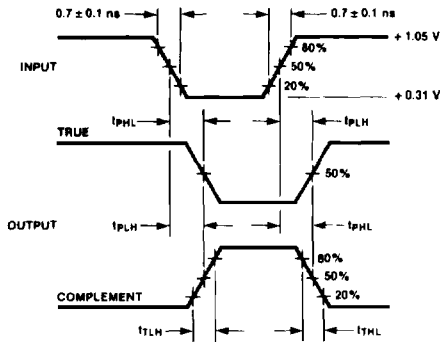
TL/F/10580-5

**Notes:**

- V<sub>CC</sub>, V<sub>CCA</sub> = +2V, V<sub>EE</sub> = -2.5V
- L1 and L2 = equal length 50Ω impedance lines
- R<sub>T</sub> = 50Ω terminator internal to scope
- Decoupling 0.1 μF from GND to V<sub>CC</sub> and V<sub>EE</sub>
- All unused outputs are loaded with 50Ω to GND
- C<sub>L</sub> = Fixture and stray capacitance ≤ 3 pF

FIGURE 1. AC Test Circuit

## Switching Waveforms



TL/F/10580-6

FIGURE 2. Propagation Delay and Transition Times