MICRON TECHNOLOGY, INC.

MT24D88C240
2 MEG x 40, 4 MEG x 20 IC DRAM CARD

T-46-23-18

IC DRAM CARD

8 MEGABYTES

2 MEG x 40, 4 MEG x 20

NEW IC DRAM CARD

FEATURES

- JEIDA, JEDEC and PCMCIA standard 88-pin IC DRAM card
- Polarized receptacle connector
- Industry standard DRAM functions and timing
- High-performance, CMOS silicon-gate process
- All outputs are fully TTL compatible
- All inputs buffered except $\overline{RAS}$ inputs
- Multiple $\overline{RAS}$ inputs for x16/18/20 or x32/36/40 selectability
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), HIDDEN and BATTERY BACKUP (BBU)
- FAST PAGE MODE access cycle
- Single +5V ±5% power supply
- Low power; 24mW standby, 3.3W active (typical)
- Extended refresh standard: 1,024 cycles every 128ms

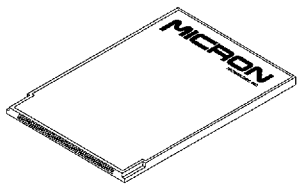
OPTIONS

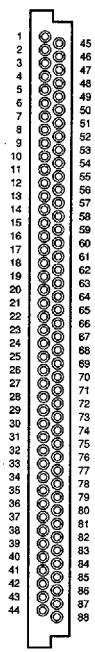
MARKING

- Timing

60ns access	-6
70ns access	-7
80ns access	-8

PIN ASSIGNMENT (End View)
88-Pin Card (U-1)





PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	31	DQ36	61	A9
2	DQ0	32	DQ37	62	NC
3	DQ1	33	DQ17	63	Vss
4	DQ2	34	DQ9	64	NC
5	DQ3	35	NC	65	$\overline{RAS1}$
6	DQ4	36	DQ10	66	$\overline{CAS2}$
7	DQ5	37	Vcc	67	Vss
8	DQ6	38	DQ11	68	$\overline{CAS3}$
9	Vcc	39	DQ12	69	$\overline{RAS3}$
10	DQ7	40	DQ13	70	$\overline{WE}$
11	NC	41	DQ14	71	PD1 (Vss)
12	DQ8	42	DQ15	72	PD3 (Vss)
13	A0	43	DQ16	73	Vss
14	A2	44	Vss	74	PD5 (Vss)
15	Vcc	45	Vss	75	PD7 (TBD)
16	A4	46	DQ18	76	PD8 (NC)
17	NC	47	DQ19	77	DQ38
18	A6	48	DQ20	78	DQ39
19	A8	49	DQ21	79	DQ35
20	NC	50	DQ22	80	DQ27
21	NC	51	DQ23	81	DQ28
22	$\overline{RAS0}$	52	DQ24	82	DQ29
23	$\overline{CAS0}$	53	DQ25	83	DQ30
24	$\overline{CAS1}$	54	DQ26	84	DQ31
25	NC	55	$\overline{OE}$ (Vss)	85	DQ32
26	$\overline{RAS2}$	56	Vss	86	DQ33
27	Vcc	57	A1	87	DQ34
28	PD2 (NC)	58	A3	88	Vss
29	PD4 (Vss)	59	A5		
30	PD6 (TBD)	60	A7		

GENERAL DESCRIPTION

The MT24D88C240 is an 8 megabyte, IC DRAM card organized primarily as a 2 Meg x 40 bit memory array for EDC applications. It may be used as a x32 or x36 bit memory array (the unused DQs should be tied to Vss or Vcc through current limiting resistors). It may also be configured as a 4 Meg x 20 bit memory array, provided the corresponding DQs on the host system are made common and memory bank control procedures are implemented. Separate $\overline{CAS}$ inputs allow byte accesses.

All inputs to the DRAMs are buffered, with the exception of $\overline{RAS}$. The line drivers used for buffers reduce reflections on the card and ensure compatibility in a wide range of systems. At the same time, the line drivers add delays to the buffered input timings when compared to standard DRAMs.

The MT24D88C240 is designed for low power operation using 1 Meg x 4 low power, extended refresh DRAMs. These devices support BATTERY BACKUP (BBU) cycle refresh; a very low current, data retention mode. Standard component DRAM refresh modes are supported as well.

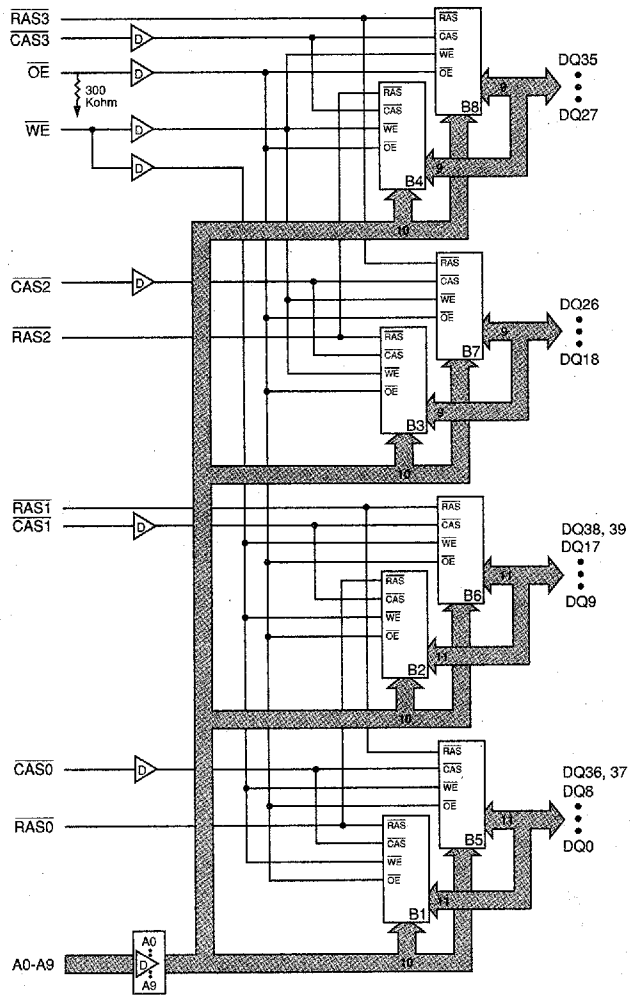
Multiple $\overline{RAS}$ inputs conserve power by allowing individual bank selection. In the x32/36/40 organization, the memory array may be divided into two banks, each with four separate bytes (x32/36 only). In the x16/18/20 organization, up to four banks, each with two separate bytes, may be independently selected. One bank is activated by each $\overline{RAS}$ selection; the others not selected remain in standby mode, drawing minimum power.

T-46-23-18

Eight presence detect pins may be read by the host to identify the MT24D88C240 organization, number of banks, access time and refresh mode. These extensive presence detect functions allow systems to utilize the advanced power saving features.

The MT24D88C240 is built with a plastic frame covered by stainless steel panels. This package, containing an 88-pin receptacle connector, is keyed to prevent improper installation or insertion into other types of IC card sockets.

FUNCTIONAL BLOCK DIAGRAM



NOTE:
1. D = 74AC11244 line drivers.
2. B1, B2, B5 and B6 = 1 Meg x 8 memory blocks; B3, B4, B7 and B8 = 1 Meg x 9 memory blocks.
3. $\overline{OE}$ is internally connected to ground via a 300 Kohm resistor and is also buffered to the DRAMs.

PIN DESCRIPTIONS

T-46-23-18

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
22, 26, 65, 69	$\overline{RAS}$0-3	Input	Row Address Strobe: $\overline{RAS}$ is used to clock-in the 10 row-address bits. Four $\overline{RAS}$ inputs allow for two x32/36/40 banks or four x16/18/20 banks.
23, 24, 66, 68	$\overline{CAS}$0-3	Input	Column Address Strobe: $\overline{CAS}$ is used to clock-in the 10 column-address bits, enable the DRAM output buffers, and strobe the data inputs on WRITE cycles. Four $\overline{CAS}$ inputs allow byte access control for any memory bank configuration (not in x40 mode).
70	$\overline{WE}$	Input	Write Enable: $\overline{WE}$ is the READ/WRITE control for the DQ pins. If $\overline{WE}$ is LOW prior to $\overline{CAS}$ going LOW, the access is an EARLY-WRITE cycle. If $\overline{WE}$ is HIGH while $\overline{CAS}$ is LOW, the access is a READ cycle, provided $\overline{OE}$ is also LOW. If WE goes LOW after $\overline{CAS}$ goes LOW, then the cycle is a LATE-WRITE cycle. A LATE-WRITE cycle is generally used in conjunction with a READ cycle to form a READ-MODIFY-WRITE cycle.
55	$\overline{OE}$	Input	Output Enable: $\overline{OE}$ is the input/output control for the DQ pins. $\overline{OE}$ is connected to ground through a 300 Kohm resistor and is intended to be LOW, allowing for EARLY-WRITE cycles only. This signal may be driven, allowing for LATE-WRITE cycles.
13, 57, 14, 58, 16, 59 18, 60, 19, 61	A0-A9	Input	Address Inputs: These inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$.
2-8, 10, 12, 34, 36 38-43, 33, 46-54, 80-87 79, 31, 32, 77, 78	DQ0-DQ39	Input/ Output	Data I/O: For WRITE cycles, DQ0-DQ39 act as inputs to the addressed DRAM location. BYTE WRITEs may be performed by using the corresponding $\overline{CAS}$ select (x32/36 mode only). For READ access cycles, DQ0-DQ39 act as outputs for the addressed DRAM location.
71, 28, 72, 29 74, 30, 75, 76	PD1-PD8	-	Presence Detect: These pins are read by the host system and tell the system the card's personality. They will be either left floating (NC) or they will be grounded (Vss).
11, 17, 20, 21, 25 35, 62, 64	NC	-	No Connect: These pins should be left unconnected (reserved for future use).
9, 15, 27, 37	Vcc	Supply	Power Supply: +5V ± 5%
1, 44, 45, 56 63, 67, 73, 88	Vss	Supply	Ground

MICRON TECHNOLOGY, INC.

MT24D88C240
2 MEG x 40, 4 MEG x 20 IC DRAM CARD

T-46-23-18

FUNCTIONAL DESCRIPTION

The MT24D88C240 is an 8 megabyte memory card structured as a 2 Meg x 32/36/40 bit memory array ($\overline{RAS0}$ = $\overline{RAS2}$, $\overline{RAS1}$ = $\overline{RAS3}$). It also may be configured as a 4 Meg x 16/18/20 bit memory array, provided the corresponding DQs on the host are connected and memory bank control procedures are implemented by interleaving all four $\overline{RAS}$ lines.

Most x32/36/40 bit applications use the same signal to control the $\overline{CAS}$ inputs. $\overline{RAS0}$ and $\overline{RAS1}$ control the lower 16/18 bits, and $\overline{RAS2}$ and $\overline{RAS3}$ control the upper 16/18 bits, to obtain a x32/36/40 memory array. For x16/18 applications, the corresponding DQs and the corresponding $\overline{CAS}$ pins must be connected together (DQ0 to DQ18, DQ1 to DQ19 and so forth, and $\overline{CAS0}$ to $\overline{CAS2}$ and $\overline{CAS1}$ to $\overline{CAS3}$). Each $\overline{RAS}$ is then a bank select for the 4 Meg x 16/18 memory organization.

DRAM OPERATION

DRAM REFRESH

Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle [READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), HIDDEN or BATTERY BACKUP (BBU) REFRESH] so that all 1,024 combinations of $\overline{RAS}$ addresses (A0-A9) are executed at least every 128ms, regardless of sequence.

The implied method of choice for refreshing the memory card is the BBU cycle. This is a very low current, data retention mode made possible by using the CBR REFRESH cycle over the extended refresh range (I_{CC7}).

The memory card may be used with the other refresh modes common in standard DRAMs. This allows the memory card to be used on existing systems that do not utilize the BBU REFRESH cycle. However, the memory card will draw more current in the STANDBY mode. The CBR REFRESH mode is recommended when not using the BBU mode.

DRAM READ AND WRITE CYCLES

During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits. READ or WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{CAS}$. $\overline{WE}$ must fall prior to $\overline{CAS}$ (EARLY WRITE); if $\overline{WE}$ goes LOW after $\overline{CAS}$, the outputs (Q) will be activated and will drive invalid data to the inputs, unless LATE-WRITE cycle timing specifications are met. The data inputs and data outputs are routed through pins using common I/O, and pin direction is controlled by $\overline{WE}$.

FAST PAGE MODE operation allows faster data operations (READ or WRITE) within a row address (A0-A9) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation. Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time.

DRAM TIMING

In accordance with JEDEC standard specifications, all inputs to the IC DRAM card are buffered, with the exception of $\overline{RAS}$ inputs. The line drivers used for buffers reduce reflections on the card and ensure compatibility in a wide range of systems. The implementation of buffers on the card may relieve the need for additional host system lin drivers. Notes 23 though 29 indicate which parameters on the IC DRAM card are affected by the line drivers, and to what magnitude they are affected. The component DRAM timing specifications, rather than those of the IC DRAM card (in systems that use both), may cause timing incompatibilities.

All traces on the IC DRAM card (buffered and non-buffered) are approximately 50 ohms characteristic impedance. Matching impedance on the system board to 50 ohms characteristic impedance on traces to the IC DRAM card will decrease signal noise to the IC DRAM card, enhancing overall system reliability.

PHYSICAL DESIGN

The MT24D88C240 is constructed with a molded plastic frame and covered with stainless steel panels. Inside, 24 thin small-outline package (TSOP) DRAMs are mounted on both sides of an ultrathin printed circuit board. The board is attached to a high insertion, 88-pin receptacle connector. The package has a polarized key to prevent improper installation, including insertion into other types of IC card sockets. The MT24D88C240 operates reliably up to 55°C.

MICRON TECHNOLOGY, INC.

MT24D88C240
2 MEG x 40, 4 MEG x 20 IC DRAM CARD

T-46-23-18

MEMORY TRUTH TABLE

FUNCTION		RAS	CAS	WE	OE	ADDRESSES		DATA IN/OUT
						t_R	t_C	DQ0-DQ39
Standby		H	H→X	X	X	X	X	High-Z
READ		L	L	H	L (NC)	ROW	COL	Data Out
EARLY-WRITE		L	L	L	X	ROW	COL	Data In
READ-WRITE		L	L	H→L	L→H	ROW	COL	Data Out
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	L (NC)	ROW	COL	Data Out
	2nd Cycle	L	H→L	H	L (NC)	n/a	COL	Data Out
FAST-PAGE-MODE EARLY-WRITE	1st Cycle	L	H→L	L	X	ROW	COL	Data In
	2nd Cycle	L	H→L	L	X	n/a	COL	Data In
FAST-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data In
	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data In
RAS-ONLY REFRESH		H	X	X	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	L (NC)	ROW	COL	Data Out
	WRITE	L→H→L	L	L	X	ROW	COL	Data In
CAS-BEFORE-RAS REFRESH		H→L	L	H	H	X	X	High-Z
BATTERY BACKUP REFRESH		H→L	L	H	H	X	X	High-Z

PRESENCE DETECT TRUTH TABLE

CHARACTERISTICS						PRESENT DETECT PIN (PDx)							
Card Density	DRAM Organizations	Card Address	RAS Address	CAS Address	Page Depth	1	2	3	4	5	6	7	8
0MB	No card installed	X	X	X	X	NC	NC	NC	NC	NC	X	X	X
1MB	256K x 1, 4, 16, 18	18	9	9	512	Vss	Vss	Vss	Vss	NC	X	X	X
2MB	256K x 1, 4, 16, 18	18	9	9	512	Vss	Vss	Vss	Vss	Vss	X	X	X
2MB	512K x 8, 9	19	10	9	512	NC	Vss	Vss	Vss	NC	X	X	X
4MB	512K x 8, 9	19	10	9	512	NC	Vss	Vss	Vss	Vss	X	X	X
4MB	1 Meg x 1, 4, 16, 18	20	10	10	1,024	Vss	NC	Vss	Vss	NC	X	X	X
• 8MB	1 Meg x 1, 4, 16, 18	20	10	10	1,024	Vss	NC	Vss	Vss	Vss	X	X	X
8MB	2 Meg x 8, 9	21	11	10	1,024	NC	NC	Vss	Vss	NC	X	X	X
16MB	2 Meg x 8, 9	21	11	10	1,024	NC	NC	Vss	Vss	Vss	X	X	X
16MB	4 Meg x 1, 4, 16, 18	22	12	11	1,024	Vss	Vss	NC	Vss	NC	X	X	X
32MB	4 Meg x 1, 4, 16, 18	22	12	11	1,024	Vss	Vss	NC	Vss	Vss	X	X	X
Access Timing		100ns				X	X	X	X	X	Vss	Vss	X
		80ns				X	X	X	X	X	NC	Vss	X
		70ns				X	X	X	X	X	Vss	NC	X
		60ns				X	X	X	X	X	NC	NC	X
		50ns				X	X	X	X	X	Vss	Vss	X
Refresh Control		Standard				X	X	X	X	X	X	X	NC
		Auto				X	X	X	X	X	X	X	Vss

NOTE: Vss = Ground.

MICRON TECHNOLOGY, INC.

MT24D88C240
2 MEG x 40, 4 MEG x 20 IC DRAM CARD

T-46-23-18

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -0.5V to +5.25V
Operating Temperature T_A (Ambient) ..... 0°C to 55°C
Storage Temperature ..... -20°C to +80°C
Power Dissipation 15W
Short Circuit Output Current 50mA
Card Insertions (Connector's Life Cycle) 10,000

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 55°C; V_{CC} = 5V ±5%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.75	5.25	V	1
Input High (Logic 1) Voltage, All Inputs		V_{IH}	3.5	V_{CC}+0.5	V	1
Input Low (Logic 0) Voltage, All Inputs		V_{IL}	-0.5	0.8	V	1
INPUT LEAKAGE CURRENT, Any input	Non-buffered	I_{IN}	-12	12	µA	
(0V ≤ V_{IN} ≤ 5.25V; all other pins not under test = 0V)	Buffered	I_{IB}	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 5.25V)		I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)		V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)		V_{OL}		0.4	V	

PARAMETER/CONDITION	SYMBOL	MAX -6	MAX -7	MAX -8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	48	48	48	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Other Inputs = V_{CC} -0.2V)	I_{CC2}	4.8	4.8	4.8	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	1.26	1.14	1.02	A	3, 4, 30
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))	I_{CC4}	900	780	660	mA	3, 4, 30
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	1.26	1.14	1.02	A	3, 30
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	1.26	1.14	1.02	A	3, 5, 30
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BBU: $\overline{CAS}$ = 0.2V or CBR cycling; $\overline{RAS}$ = ^tRAS (MIN) up to 300ns; ^tRC = 125µs; $\overline{WE}$, A0-A9 and DQ = Vcc -0.2V or 0.2V (DQ may be left open)	I_{CC7}	7.2	7.2	7.2	mA	3, 5

MICRON TECHNOLOGY, INC.

MT24D88C240
2 MEG x 40, 4 MEG x 20 IC DRAM CARD

CAPACITANCE

T-46-23-18

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: $\overline{CAS0}$, $\overline{CAS1}$, $\overline{CAS2}$, $\overline{CAS3}$, A0-A9, $\overline{OE}$	C_{I1}		9	pF	2
Input Capacitance: $\overline{WE}$	C_{I2}		13	pF	2
Input Capacitance: $\overline{RAS0}$, $\overline{RAS1}$, $\overline{RAS2}$, $\overline{RAS3}$	C_{I3}		50	pF	2
Input/Output Capacitance: DQ	C_{IO}		20	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \le T_A \le 55°C$; V_{CC} = 5V ±5%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t_{RC}	110		130		150		ns	23
FAST-PAGE-MODE READ or WRITE cycle time	t_{PC}	40		40		45		ns	23
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	14, 23
Access time from $\overline{CAS}$	t_{CAC}		25		30		30	ns	15, 26
Access time from column address	t_{AA}		40		45		50	ns	26
Access time from $\overline{CAS}$ precharge	t_{CPA}		50		50		55	ns	26
$\overline{RAS}$ pulse width	t_{RAS}	60	100,000	70	100,000	80	100,000	ns	23
$\overline{RAS}$ pulse width (FAST PAGE MODE)	t_{RASP}	60	100,000	70	100,000	80	100,000	ns	23
$\overline{RAS}$ hold time	t_{RSH}	25		30		30		ns	26
$\overline{RAS}$ precharge time	t_{RP}	45		50		60		ns	23
$\overline{CAS}$ pulse width	t_{CAS}	15	100,000	20	100,000	20	100,000	ns	23
$\overline{CAS}$ hold time	t_{CSH}	55		65		75		ns	25
$\overline{CAS}$ precharge time	t_{CPN}	10		10		10		ns	16, 23
$\overline{CAS}$ precharge time (FAST PAGE MODE)	t_{CP}	10		10		10		ns	23
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	10	35	15	40	15	50	ns	17, 28
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	15		15		15		ns	26
Row address setup time	t_{ASR}	10		10		10		ns	26
Row address hold time	t_{RAH}	5		5		5		ns	25
$\overline{RAS}$ to column address delay time	t_{RAD}	10	20	10	25	10	30	ns	18, 28
Column address setup time	t_{ASC}	5		5		5		ns	24
Column address hold time	t_{CAH}	15		20		20		ns	24
Column address hold time (referenced to $\overline{RAS}$)	t_{AR}	45		50		55		ns	25
Column address to $\overline{RAS}$ lead time	t_{RAL}	40		45		50		ns	26
Read command setup time	t_{RCS}	5		5		5		ns	25
Read command hold time (referenced to $\overline{CAS}$)	t_{RCH}	5		5		5		ns	19, 24
Read command hold time (referenced to $\overline{RAS}$)	t_{RRH}	-5		-5		-5		ns	19, 25
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		5		ns	24
Output buffer turn-off delay	t_{OFF}	5	30	5	30	5	30	ns	20, 29, 35
$\overline{WE}$ command setup time	t_{WCS}	5		5		5		ns	24

T-46-23-18

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \le T_A \le 55°C$; $V_{CC} = 5V \pm 5\%$)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Write command hold time	tWCH	15		20		20		ns	24
Write command hold time (referenced to $\overline{RAS}$)	tWCR	40		50		55		ns	25
Write command pulse width	tWP	10		15		15		ns	23
Write command to $\overline{RAS}$ lead time	tRWL	25		30		30		ns	26
Write command to $\overline{CAS}$ lead time	tCWL	20		25		25		ns	24
Data-in setup time	tDS	5		5		5		ns	24, 32
Data-in hold time	tDH	5		10		10		ns	25, 32
Data-in hold time (referenced to $\overline{RAS}$)	tDHR	45		55		60		ns	23
Transition time (rise or fall)	tT	2	15	2	15	2	15	ns	9, 10, 23
Refresh period (1,024 cycles)	tREF		128		128		128	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	10		10		10		ns	26
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tCSR	20		20		20		ns	5, 26
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tCHR	10		10		10		ns	5, 25
$\overline{WE}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tWRH	5		5		5		ns	22, 25
$\overline{WE}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tWRP	20		20		20		ns	22, 26
$\overline{WE}$ hold time (WCBR test cycle)	tWTH	5		5		5		ns	22, 25
$\overline{WE}$ setup time	tWTS	20		20		20		ns	22, 26
READ-WRITE cycle time	tRWC	165		185		205		ns	
FAST-PAGE-MODE READ-WRITE cycle time	tPRWC	90		95		100		ns	23
$\overline{RAS}$ to $\overline{WE}$ delay time	tRWD	80		90		100		ns	31, 27
Column Address to $\overline{WE}$ delay time	tAWD	65		70		75		ns	31, 24
$\overline{CAS}$ to $\overline{WE}$ delay time	tCWD	50		65		55		ns	31, 24
Output buffer turn-off delay	tOE		25		30		30	ns	20, 33, 26
Output disable	tOD		25		30		30	ns	35, 26
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	tOEH	5		10		10		ns	34, 27
$\overline{OE}$ hold time from $\overline{RAS}$ during HIDDEN REFRESH cycle	tORD	10		10		10		ns	21, 26

T-46-23-18

NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%, f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^{t}RCD < {}^{t}RCD$ (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that $^{t}RCD \geq {}^{t}RCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CPN.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RCD (MAX) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
22. ^{t}WTS and ^{t}WTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverse of ^{t}WRP and ^{t}WRH in the CBR refresh cycle.
23. Timing between the DRAMs and the DRAM card did not change with the addition of the line drivers.
24. A +5ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
25. A -5ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
26. A +10ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
27. A -10ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
28. A -5ns (MIN) and a -10ns (MAX) timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
29. A +5ns (MIN) and a +10ns (MAX) timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
30. The maximum current ratings are based with the memory operating or being refreshed in the x32/36/40 mode. The stated maximums may be reduced by one half when used in the x16/18/20 mode.
31. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are restrictive operating parameters in late WRITE, and READ-MODIFY-WRITE cycles only. If $^{t}WCS \geq {}^{t}WCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^{t}RWD \geq {}^{t}RWD$ (MIN), $^{t}AWD \geq {}^{t}AWD$ (MIN) and $^{t}CWD \geq {}^{t}CWD$ (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data out is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE-WRITE ($\overline{OE}$ controlled) cycle.

T-46-23-18

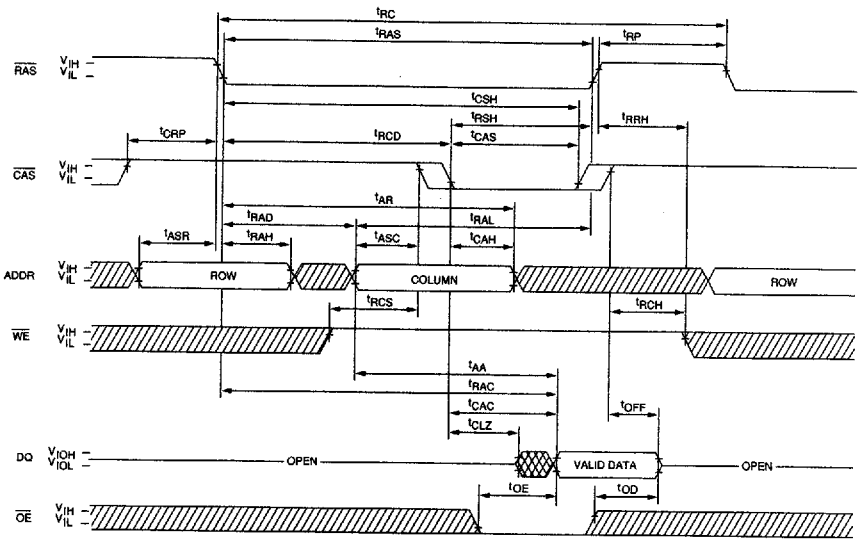
NOTES (continued)

32. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{WE}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
33. If $\overline{OE}$ is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
34. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ^tOEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
35. The DQs open during READ cycles once ^tOD or ^tOFF occur. If $\overline{CAS}$ goes HIGH first, $\overline{OE}$ becomes a "don't care." If $\overline{OE}$ goes HIGH and $\overline{CAS}$ stays LOW, $\overline{OE}$ is not a "don't care;" and the DQs will provide the previously read data if $\overline{OE}$ is taken back LOW (while $\overline{CAS}$ remains LOW).

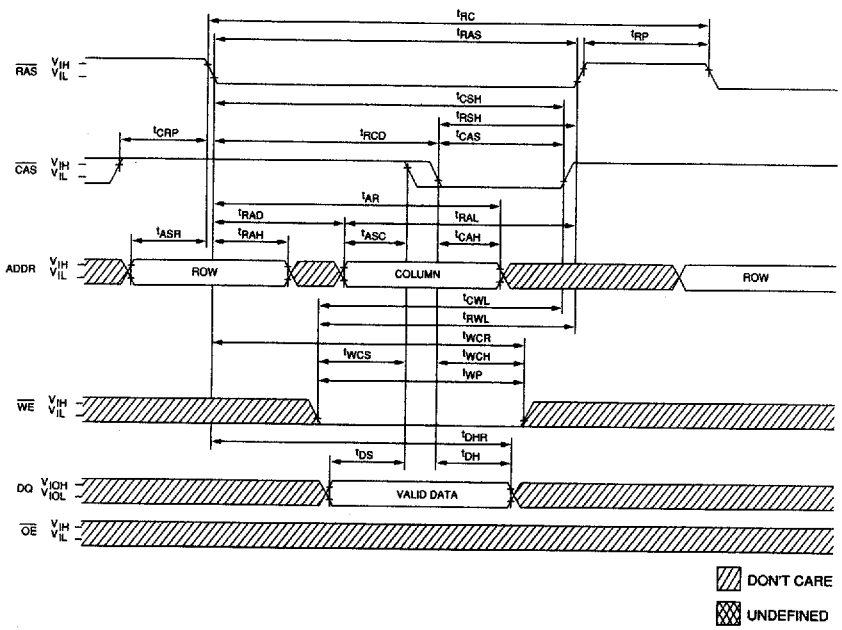
NEW IC DRAM CARD

READ CYCLE

T-46-23-18

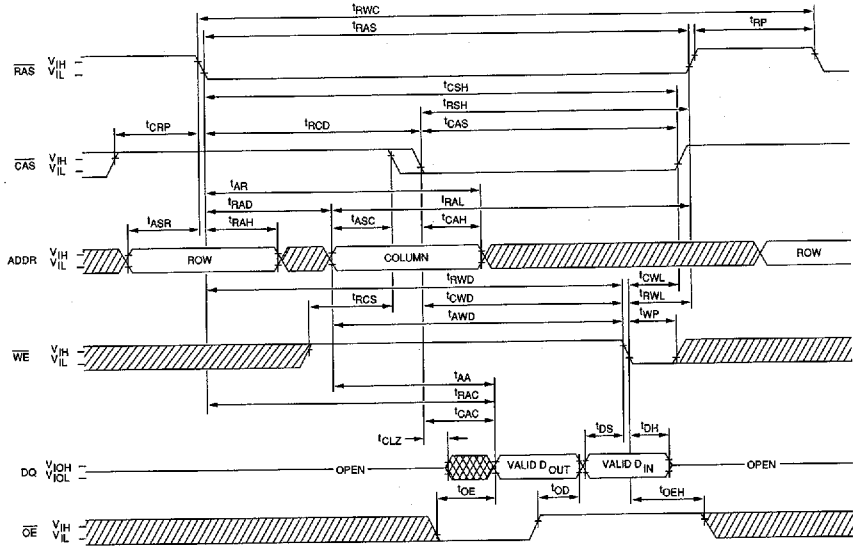


EARLY-WRITE CYCLE

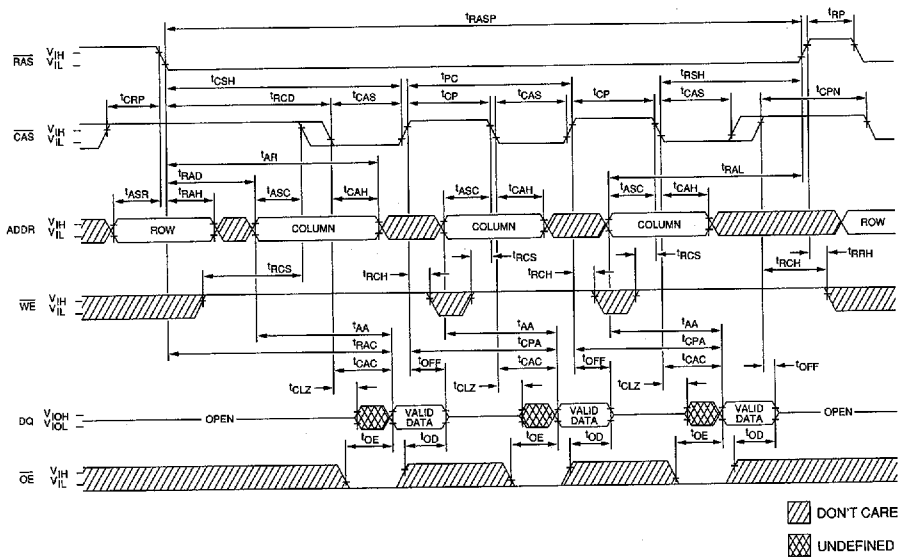


T-46-23-18

READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)

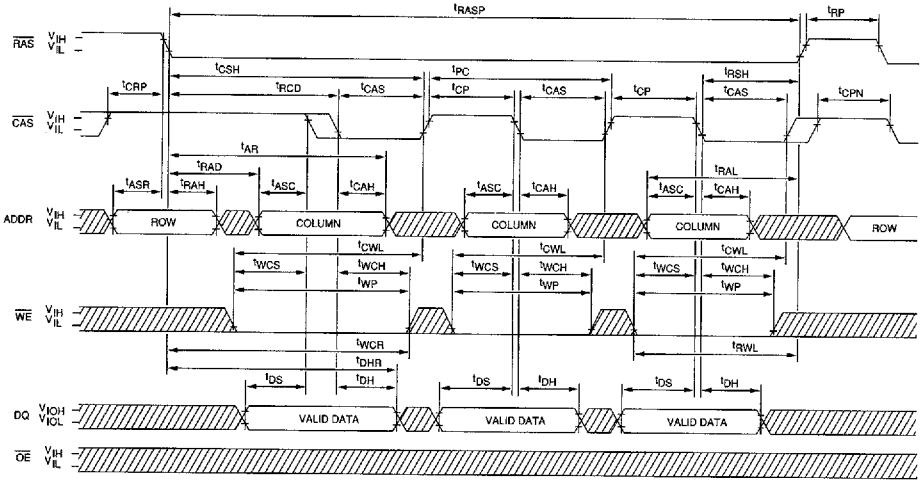


FAST-PAGE-MODE READ CYCLE

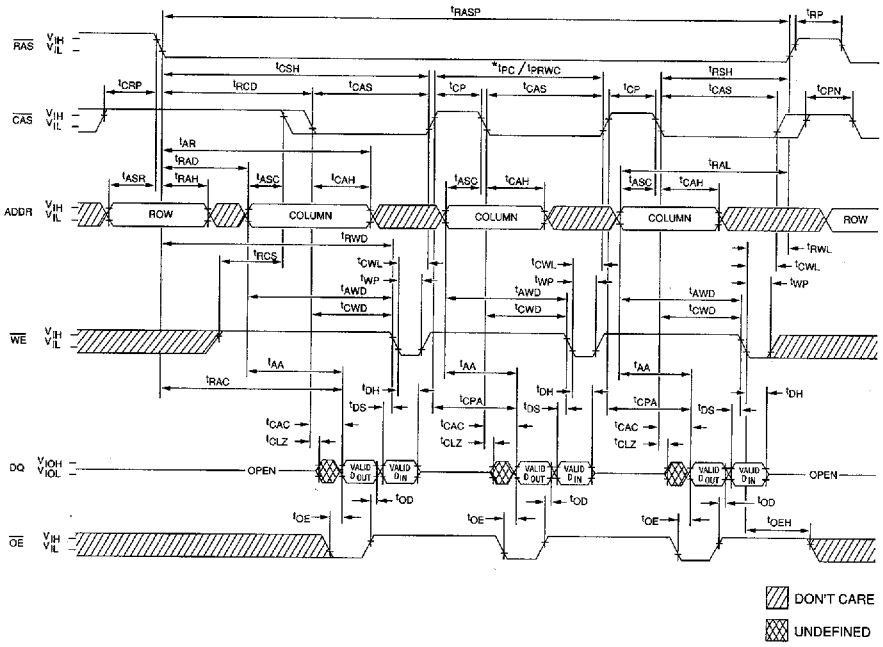


T-46-23-18

FAST-PAGE-MODE EARLY-WRITE CYCLE



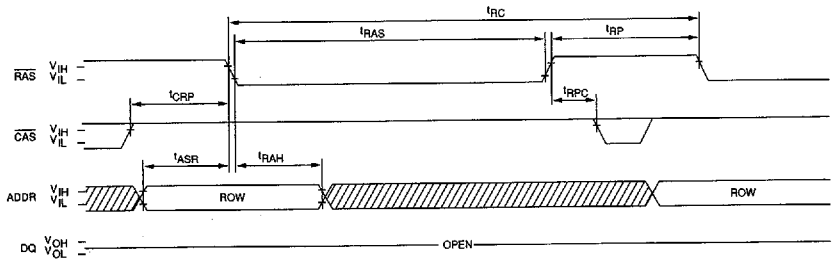
FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



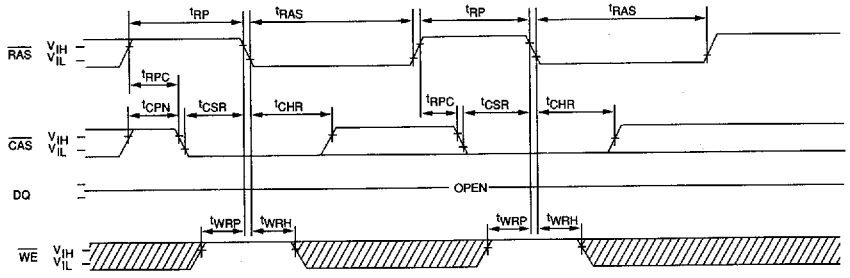
NEW IC DRAM CARD

T-46-23-18

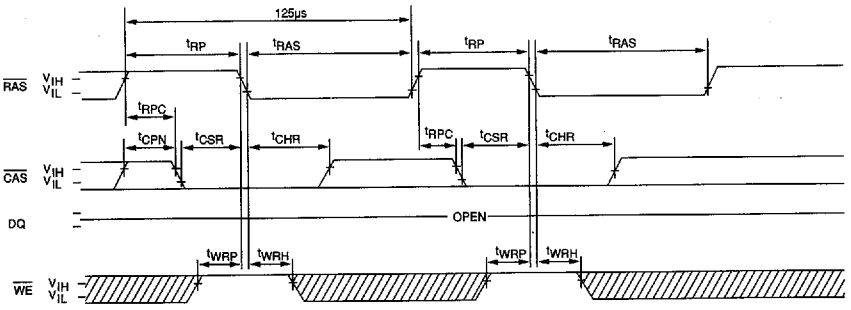
RAS-ONLY REFRESH CYCLE
(ADDR = A0-A9; WE = DON'T CARE)



CAS-BEFORE-RAS REFRESH CYCLE
(A0-A9 = DON'T CARE)

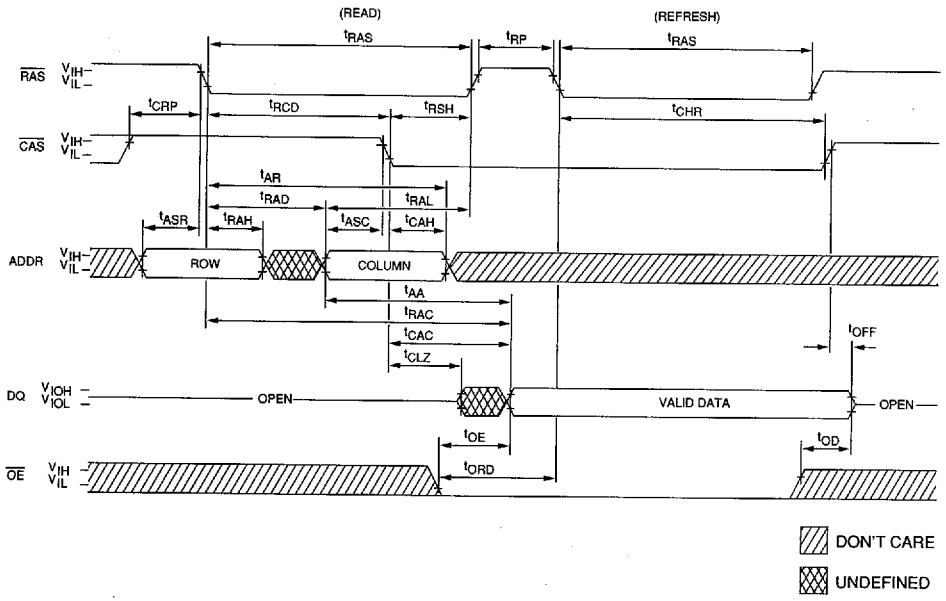


BATTERY BACKUP REFRESH CYCLE
(A0-A9 = DON'T CARE)



HIDDEN REFRESH CYCLE [21]
($\overline{WE}$ = HIGH)

T-46-23-18



NEW IC DRAM CARD

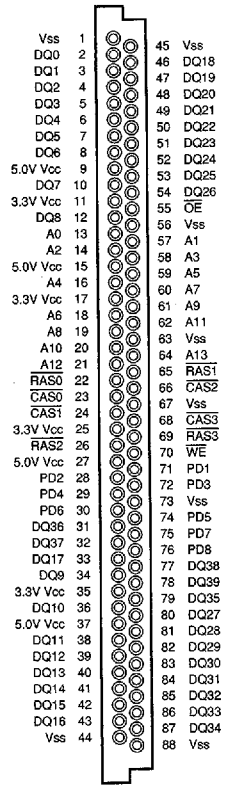
MICRON TECHNOLOGY, INC.

MT24D88C240
2 MEG x 40, 4 MEG x 20 IC DRAM CARD

T-46-23-18

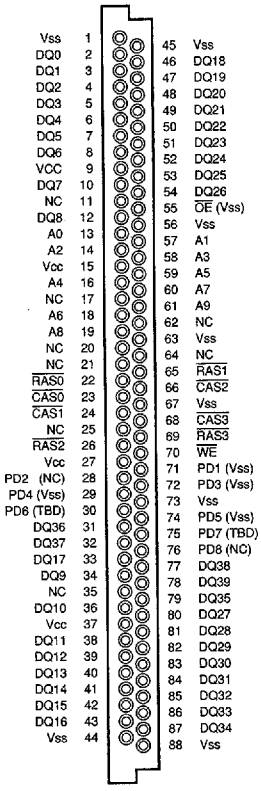
NEW IC DRAM CARD

RESERVED JEDEC, JEIDA and PCMCIA 88-PIN ASSIGNMENT
(All Possible Combinations)



Vss	1	45	Vss
DQ0	2	46	DQ18
DQ1	3	47	DQ19
DQ2	4	48	DQ20
DQ3	5	49	DQ21
DQ4	6	50	DQ22
DQ5	7	51	DQ23
DQ6	8	52	DQ24
5.0V Vcc	9	53	DQ25
DQ7	10	54	DQ26
3.3V Vcc	11	55	$\overline{OE}$
DQ8	12	56	Vss
A0	13	57	A1
A2	14	58	A3
5.0V Vcc	15	59	A5
A4	16	60	A7
3.3V Vcc	17	61	A9
A6	18	62	A11
A8	19	63	Vss
A10	20	64	A13
A12	21	65	$\overline{RAS1}$
$\overline{RAS0}$	22	66	$\overline{CAS2}$
$\overline{CAS0}$	23	67	Vss
$\overline{CAS1}$	24	68	$\overline{CAS3}$
3.3V Vcc	25	69	$\overline{RAS3}$
$\overline{RAS2}$	26	70	$\overline{WE}$
5.0V Vcc	27	71	PD1
PD2	28	72	PD3
PD4	29	73	Vss
PD6	30	74	PD5
DQ36	31	75	PD7
DQ37	32	76	PD8
DQ17	33	77	DQ38
DQ9	34	78	DQ39
3.3V Vcc	35	79	DQ35
DQ10	36	80	DQ27
5.0V Vcc	37	81	DQ28
DQ11	38	82	DQ29
DQ12	39	83	DQ30
DQ13	40	84	DQ31
DQ14	41	85	DQ32
DQ15	42	86	DQ33
DQ16	43	87	DQ34
Vss	44	88	Vss

MT24D88C240 PIN ASSIGNMENT
(JEDEC Standard)



Vss	1	45	Vss
DQ0	2	46	DQ18
DQ1	3	47	DQ19
DQ2	4	48	DQ20
DQ3	5	49	DQ21
DQ4	6	50	DQ22
DQ5	7	51	DQ23
DQ6	8	52	DQ24
VCC	9	53	DQ25
DQ7	10	54	DQ26
NC	11	55	$\overline{OE}$ (Vss)
DQ8	12	56	Vss
A0	13	57	A1
A2	14	58	A3
Vcc	15	59	A5
A4	16	60	A7
NC	17	61	A9
A6	18	62	NC
A8	19	63	Vss
NC	20	64	NC
NC	21	65	$\overline{RAS1}$
$\overline{RAS0}$	22	66	$\overline{CAS2}$
$\overline{CAS0}$	23	67	Vss
$\overline{CAS1}$	24	68	$\overline{CAS3}$
NC	25	69	$\overline{RAS3}$
$\overline{RAS2}$	26	70	$\overline{WE}$
Vcc	27	71	PD1 (Vss)
PD2 (NC)	28	72	PD3 (Vss)
PD4 (Vss)	29	73	Vss
PD6 (TBD)	30	74	PD5 (Vss)
DQ36	31	75	PD7 (TBD)
DQ37	32	76	PD8 (NC)
DQ17	33	77	DQ38
DQ9	34	78	DQ39
NC	35	79	DQ35
DQ10	36	80	DQ27
Vcc	37	81	DQ28
DQ11	38	82	DQ29
DQ12	39	83	DQ30
DQ13	40	84	DQ31
DQ14	41	85	DQ32
DQ15	42	86	DQ33
DQ16	43	87	DQ34
Vss	44	88	Vss