

FAST 74F674

Shift Register

FAST Products

FEATURES

- 16-bit serial I/O shift register
- 16-bit parallel-in/serial-out converter
- Recirculating serial shifting
- Common serial data I/O pin (3-state)

DESCRIPTION

The 74F674 is a 16 bit shift register with serial and parallel load capability and serial output. A single pin serves alternately as an input for serial entry or as 3-state serial output. In the serial out mode the data recirculates in the register. Chip Select, Read/Write and Mode inputs provide control flexibility. The 'F674 operates in one of four modes, as indicated in the Function Table.

Hold : a High signal on the Chip Select (\overline{CS}) input prevents clocking and forces the Serial Input/Output (S/I/O) 3-state buffer into the high impedance state.

Serial load : data present on the S/I/O pin shifts into the register on the falling edge of \overline{CP} . Data enters the Q_0 position and shifts toward Q_{15} on successive clocks.

Serial output : the S/I/O 3-state buffer is active and the register contents are shifted out from Q_{15} and simultaneously shifted back into Q_0 .

16-Bit Serial/Parallel-In, Serial-Out Shift Register (3-State)

Product Specification

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F674	95MHz	55mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0^\circ C$ to $+70^\circ C$
24-Pin Plastic Slim DIP (300mil)	N74F674N
24-Pin Plastic SOL	N74F674D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$D_0 - D_{15}$	Parallel data inputs	1.0/1.0	20 μ A/0.6mA
\overline{CS}	Chip Select input (active Low)	1.0/1.0	20 μ A/0.6mA
\overline{CP}	Clock Pulse input (active falling edge)	1.0/1.0	20 μ A/0.6mA
M	Mode select input	1.0/1.0	20 μ A/0.6mA
R/\overline{W}	Read/Write input	1.0/1.0	20 μ A/0.6mA
S/I/O	Serial data input or	3.5/1.0	70 μ A/0.6mA
	Serial 3-state output	150/40	3.0mA/24mA

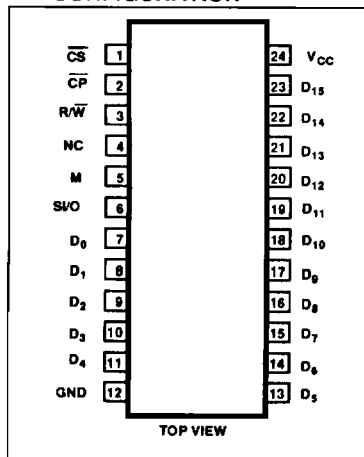
NOTE:

One (1.0) FAST Unit Load is defined as: 20 μ A in the High state and 0.6mA in the Low state.

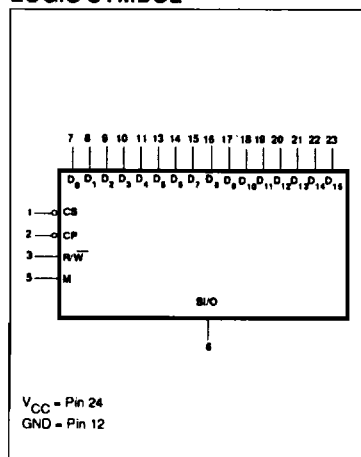
Parallel load : data present on $D_0 - D_{15}$ is entered into the register on the falling edge of \overline{CP} . The S/I/O 3-state buffer is active and represents the Q_{15} output.

To prevent false clocking, \overline{CP} must be Low during a Low-to-High transition of \overline{CS} .

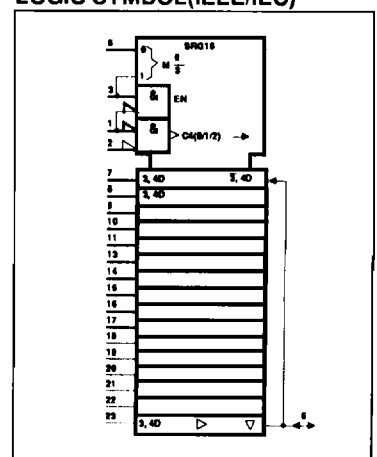
PIN CONFIGURATION



LOGIC SYMBOL



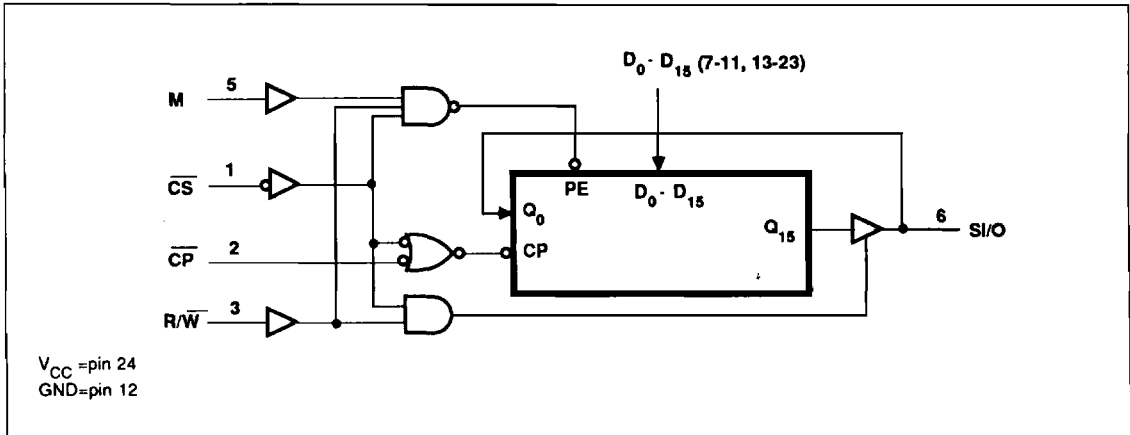
LOGIC SYMBOL (IEEE/IEC)



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LOGIC DIAGRAM



FUNCTION TABLE

CONTROL INPUTS				SI/O STATUS	OPERATING MODE
\overline{CS}	R/\overline{W}	M	\overline{CP}		
H	X	X	X	High Z	Hold
L	L	X	↓	Data in	Serial load
L	H	L	↓	Data out	Serial output with recirculation
L	H	H	↓	Active	Parallel load ; no shifting

- H = High voltage level
- L = Low voltage level
- X = Don't care
- ↓ = High-to-Low transition of designated input

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-3	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS ¹	LIMITS			UNIT		
				Min	Typ ²	Max			
V_{OH}	High-level output voltage		$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}$	$\pm 10\%V_{CC}$	2.4		V		
			$V_{IH} = \text{MIN}, I_{OH} = \text{MAX}$	$\pm 5\%V_{CC}$	2.7	3.3		V	
V_{OL}	Low-level output voltage		$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}$	$\pm 10\%V_{CC}$		0.35	0.50	V	
			$V_{IH} = \text{MIN}, I_{OL} = \text{MAX}$	$\pm 5\%V_{CC}$		0.35	0.50	V	
V_{IK}	Input clamp voltage		$V_{CC} = \text{MIN}, I_I = I_{IK}$			-0.73	-1.2	V	
I_I	Input current at maximum input voltage	SI/O only	$V_{CC} = \text{MAX}, V_I = 5.5\text{V}$				100	μA	
		others	$V_{CC} = \text{MAX}, V_I = 7.0\text{V}$						
I_{IH}	High-level input current		$V_{CC} = \text{MAX}, V_I = 2.7\text{V}$				20	μA	
I_{IL}	Low-level input current		$V_{CC} = \text{MAX}, V_I = 0.5\text{V}$				-0.6	mA	
$I_{OZH} + I_{IH}$	Off state output current, High-level voltage applied	SI/O only	$V_{CC} = \text{MAX}, V_O = 2.7\text{V}$				70	μA	
			$V_{CC} = \text{MAX}, V_O = 0.5\text{V}$					-600	μA
I_{OS}	Short circuit output current ³		$V_{CC} = \text{MAX}$			-60		mA	
I_{CC}	Supply current (total)		$V_{CC} = \text{MAX}$				55	80	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5\text{V}, T_A = 25^\circ\text{C}$.
- Not more than one output should be shorted at a time. For testing I_{OS} , the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

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AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$T_A = +25^\circ\text{C}$ $V_{CC} = 5\text{V}$ $C_L = 50\text{pF}$ $R_L = 500\Omega$			$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = 5\text{V} \pm 10\%$ $C_L = 50\text{pF}$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	80	95		70		MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{\text{CP}}$ to S/O	Waveform 1	7.0 6.0	9.5 8.5	12.5 11.5	6.5 5.5	14.0 12.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{\text{CS}}$ to S/O	Waveform 3 Waveform 4	5.5 7.0	8.5 9.5	11.0 12.5	5.0 6.5	12.5 14.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{\text{CS}}$ to S/O	Waveform 3 Waveform 4	3.0 4.5	6.0 7.5	8.5 10.0	3.0 4.5	10.0 11.5	ns
t_{PZH} t_{PZL}	Output Enable time R/W to S/O	Waveform 3 Waveform 4	6.0 7.5	8.5 10.0	11.5 13.0	5.5 7.0	13.0 14.0	ns
t_{PHZ} t_{PLZ}	Output Disable time R/W to S/O	Waveform 3 Waveform 4	5.0 5.5	7.5 8.0	10.5 11.0	4.5 5.0	12.0 13.5	ns

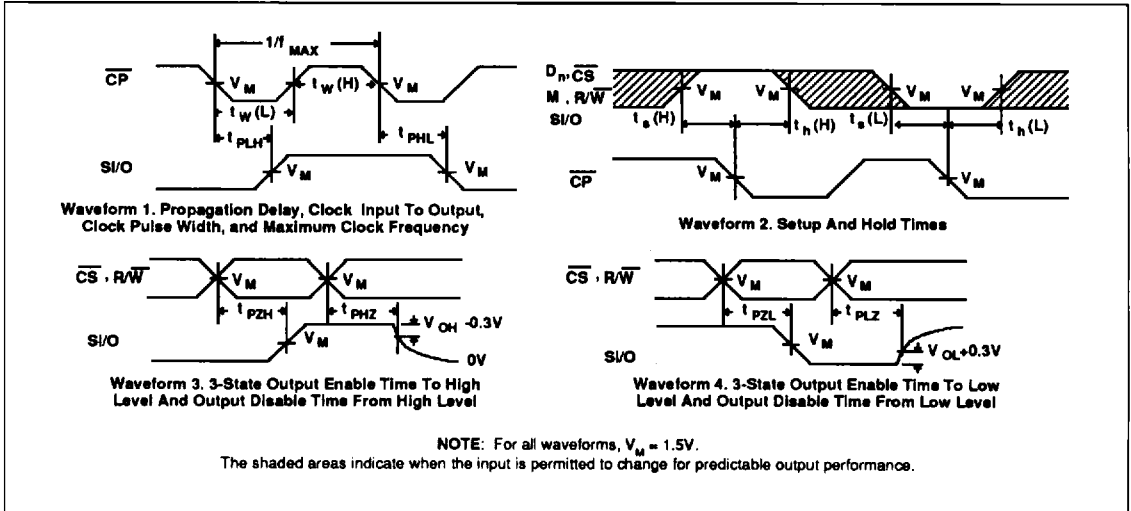
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$T_A = +25^\circ\text{C}$ $V_{CC} = 5\text{V}$ $C_L = 50\text{pF}$ $R_L = 500\Omega$			$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = 5\text{V} \pm 10\%$ $C_L = 50\text{pF}$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_{\text{s}}(\text{H})$ $t_{\text{s}}(\text{L})$	Setup time, High or Low S/O to $\overline{\text{CP}}$	Waveform 2	2.0 2.0			2.5 2.5		ns
$t_{\text{h}}(\text{H})$ $t_{\text{h}}(\text{L})$	Hold time, High or Low S/O to $\overline{\text{CP}}$	Waveform 2	1.5 1.5			2.0 2.0		ns
$t_{\text{s}}(\text{H})$ $t_{\text{s}}(\text{L})$	Setup time, High or Low D_n to $\overline{\text{CP}}$	Waveform 2	1.5 1.0			2.0 1.0		ns
$t_{\text{h}}(\text{H})$ $t_{\text{h}}(\text{L})$	Hold time, High or Low D_n to $\overline{\text{CP}}$	Waveform 2	3.0 4.0			3.0 4.0		ns
$t_{\text{s}}(\text{H})$ $t_{\text{s}}(\text{L})$	Setup time, High or Low M to $\overline{\text{CP}}$	Waveform 2	2.0 5.5			2.5 6.0		ns
$t_{\text{h}}(\text{H})$ $t_{\text{h}}(\text{L})$	Hold time, High or Low M to $\overline{\text{CP}}$	Waveform 2	0.0 0.0			1.0 1.0		ns
$t_{\text{s}}(\text{L})$	Setup time, Low $\overline{\text{CS}}$ to $\overline{\text{CP}}$	Waveform 2	8.0			9.0		ns
$t_{\text{h}}(\text{H})$	Hold time, High $\overline{\text{CS}}$ to $\overline{\text{CP}}$	Waveform 2	0.0			0.0		ns
$t_{\text{w}}(\text{H})$ $t_{\text{w}}(\text{L})$	$\overline{\text{CP}}$ Pulse width, High or Low	Waveform 1	3.5 4.5			4.0 5.0		ns

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AC WAVEFORMS



TEST CIRCUIT AND WAVEFORMS

