SL6140

400MHz WIDEBAND AGC AMPLIFIER

(Supersedes Edition in May 1991 Professional Products I.C. Handbook)

The SL6140 is an integrated broadband AGC amplifier, designed on an advanced 3–micron all implanted bipolar process. The amplifier provides over 15dB of linear gain into 50Ω at 400MHz.

Accurate gain control is also provided with over 70dB of dynamic range.

The SL6140 provides over 45dB of voltage gain with an R_L of 1kΩ.

FEATURES

- 400MHz Bandwidth (R_L=50Ω)
- High voltage Gain 45dB (R_L=1kΩ)
- 70dB Gain Control Range
- High Output Level at Low Gain
- Accurate Gain Control
- Full Military Temperature Range (CM only)
- MC1590 Replacement with Improved Perforance in most applications

APPLICATIONS

- RF/IF Amplifier
- High Gain Mixers
- Video Amplifiers

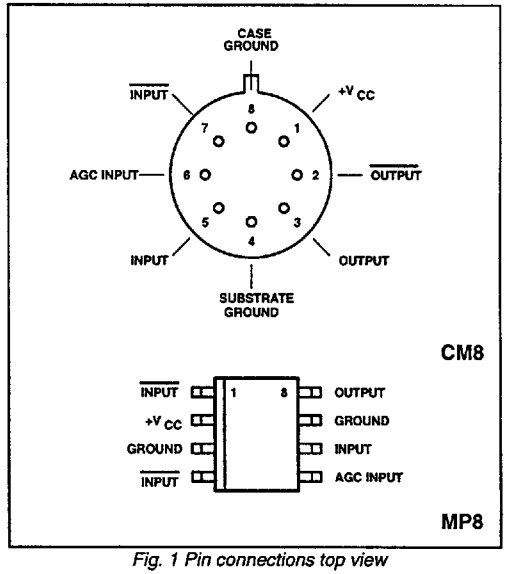

Fig. 1 Pin connections top view

ORDERING INFORMATION

SL6140/NA/MP Industrial temperature range miniature plastic package.
SL6140A/CM Military temperature range metal can package.
SL6140AC/CM MIL STD 883 "Class B" compliant metal can package.

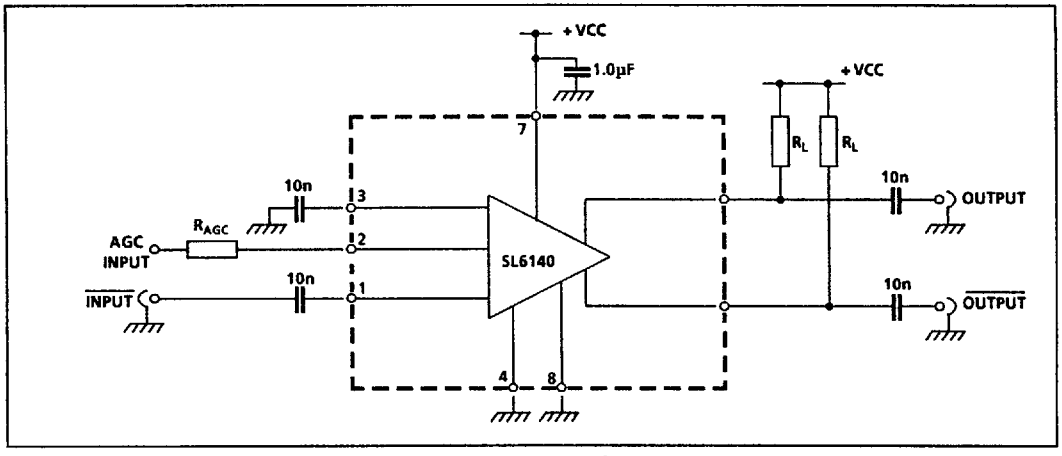

Fig.2 Typical application (CM pinout)

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)

T_{amb} = 25°C, V_{CC} = 12V ±5%, V_{IN} = 1mV_{RMS}, Frequency = 6MHz, Load (R_L) = 1KOHms, R_{AGC} = 22KOHm

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply current	5,6,7		19	23	mA	No input signal
Output stage current	5,6 (sum)	5	7	9	mA	No input signal
Output current matching (magnitude of difference of output currents)	5,6		1.0		mA	See note 2
AGC range	2	60	75		dB	See Fig. 4 & Note 1 (VAGC = 0V to 10V)
Voltage gain (single ended)	5,6	40	45		dB	R_L = 1kΩ See Fig. 5 & Note 1
			55		dB	Tuned input and Output
	5,6		15		dB	R_L = 50Ω
Bandwidth (-3dB)	5,6		25		MHz	RL = 1kΩ See Fig. 5 See note 2
			400			RL = 50Ω
Maximum output level (single ended)						
0dB AGC	5,6	2.5	3.5		V p-p	Note 1
-30dB AGC	5,6	2.5	3.5		V p-p	R_L = 1kΩ. Note 1
Noise figure	5,6		5		dB	Test CCT Fig. 13
Gain change with temp.	5,6		+4.5		dB	At -55°C W.R.T R/T See note 2
V_{AGC} = 9V	5,6		-3		dB	At +125°C W.R.T R/T See note 2
Gain change with temp.	5,6		+2		dB	At -55°C W.R.T R/T See note 2
V_{AGC} = 10V	5,6		-3		dB	At +125°C W.R.T R/T See note 2

Note: 1 Guaranteed but not tested for MP package

Note: 2 Guaranteed but not tested

DESCRIPTION

The SL6140 (Fig. 3) is a high gain amplifier with an AGC control capable of reducing the gain of the amplifier by over 70dB. The gain is adjustable by applying a voltage to the AGC input via an external resistor (R_{AGC}), the value of which adjusts the curve of gain reduction versus control voltage (see Fig. 4). As the output stage of the amplifier is an open collector the maximum voltage gain is determined by R_L. With load resistance of 1kΩ the single ended voltage gain is 45dB and with a load resistance of 50Ω the voltage gain is 15dB ($20\log_{10} V_{OUT}/V_{IN}$). Another parameter that depends on the load resistance is the bandwidth: 25MHz for R_L = 1kΩ, as compared with 400MHz for R_L = 50Ω. R_L is chosen to give either the required bandwidth or voltage gain for the circuit.

Figs. 7 through to 10 show the typical S parameters for the device. Figs 11 and 12 show the typical variation in 3rd order intercept performance with AGC.

In any application, the substrate (pin 4 in CM 8, pin 7 in MP 8) should be connected to the most negative point in the circuit, usually to the same point as pin 8 (pin 3 in MP 8).

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	+18V
Input voltage (differential)	+5V
AGC supply	V_{CC}
Storage temperature	-55°C to +150°C
Operating temperature range	
SL6140 MP	-40°C to +85°C
SL6140 A CM	-55°C to +125°C
	at 200mW
Chip operating temperature	
SL6140 MP	+150°C
SL6140 (CM variants)	+175°C

THERMAL RESISTANCE

Chip-to-ambient	
SL6140 MP	163°c/w
SL6140 (CM variants)	225°C/W
Chip-to-case	
SL6140 MP	57°C/W
SL6140 (CM variants)	65°C/W

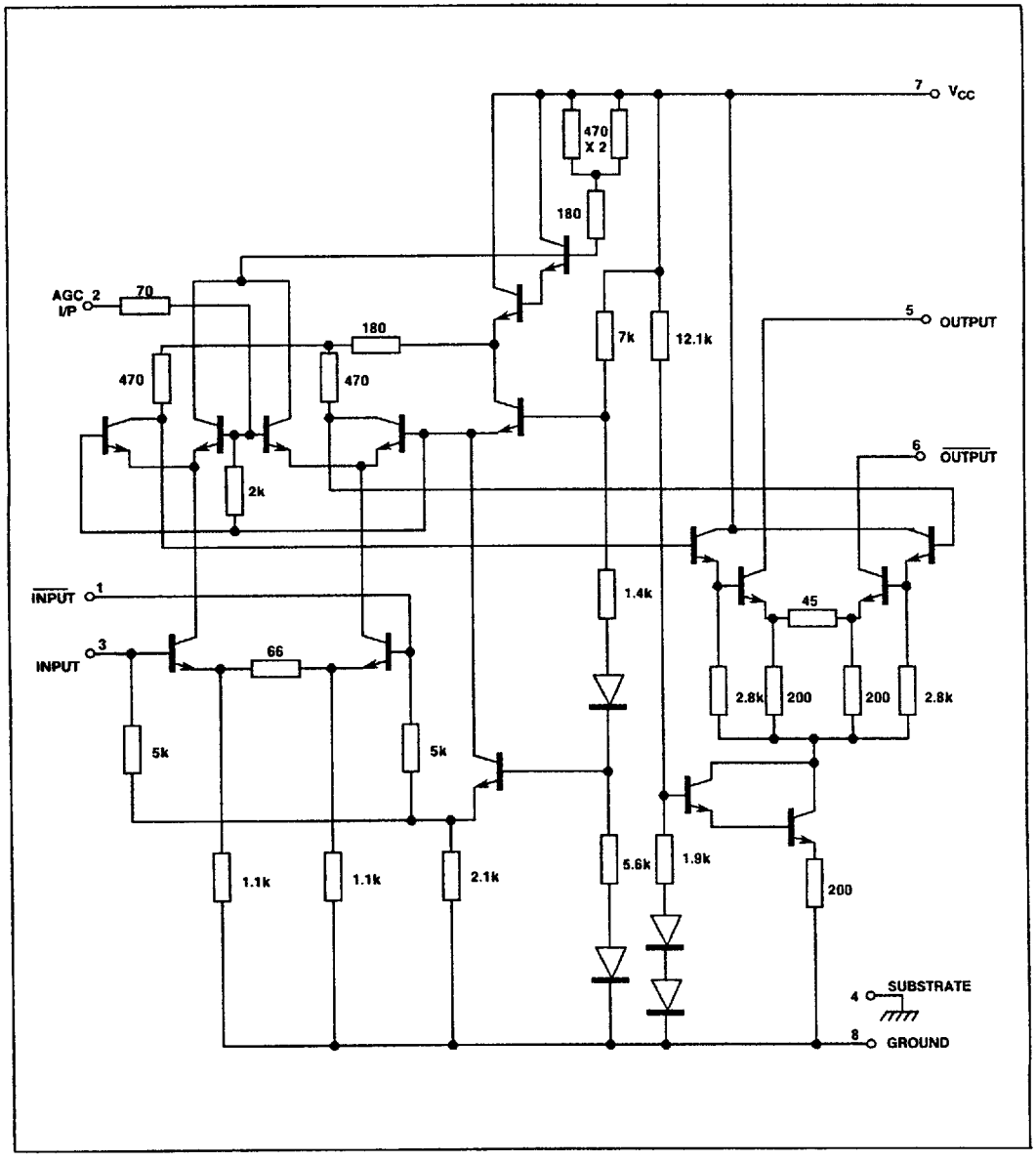

Fig. 3 Full circuit diagram of SL6140 (CM pinout)

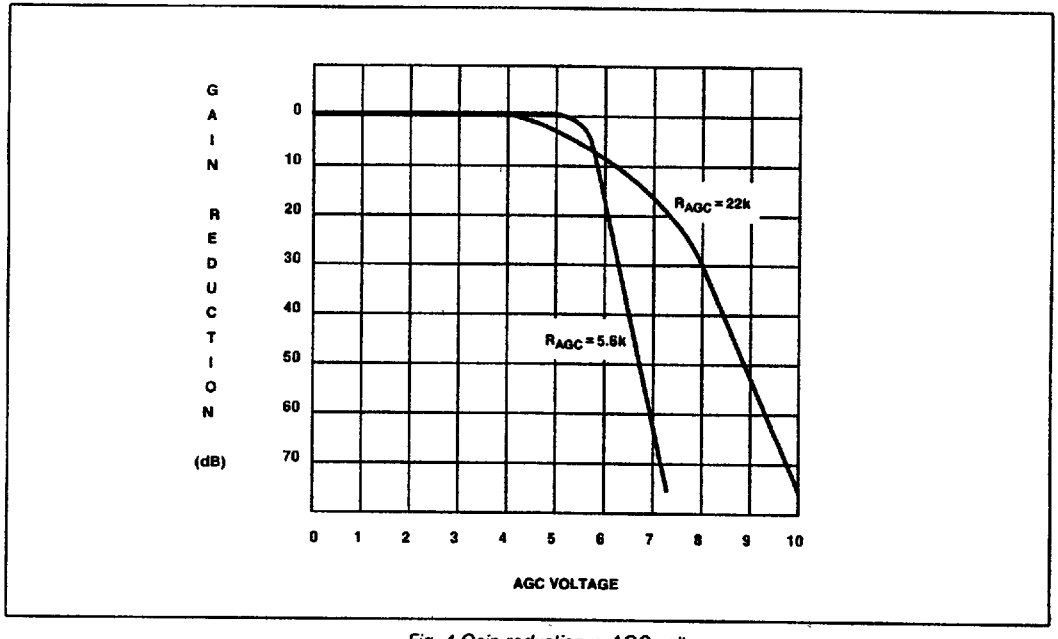

Fig. 4 Gain reduction v. AGC voltage

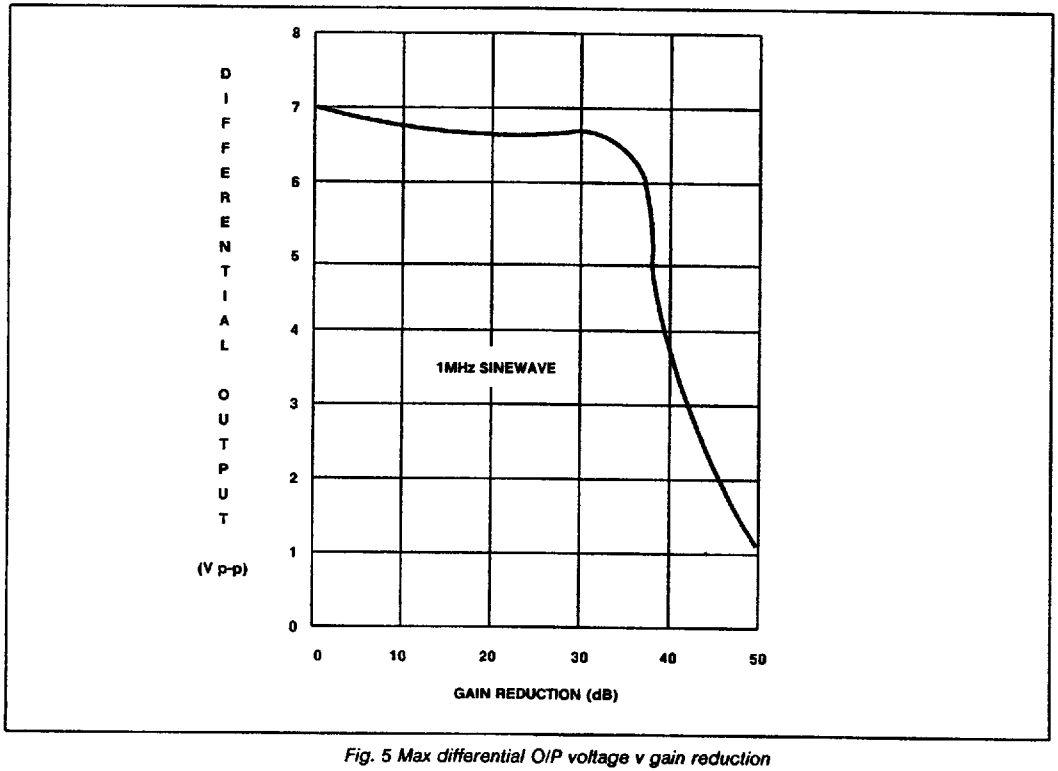

Fig. 5 Max differential O/P voltage v gain reduction

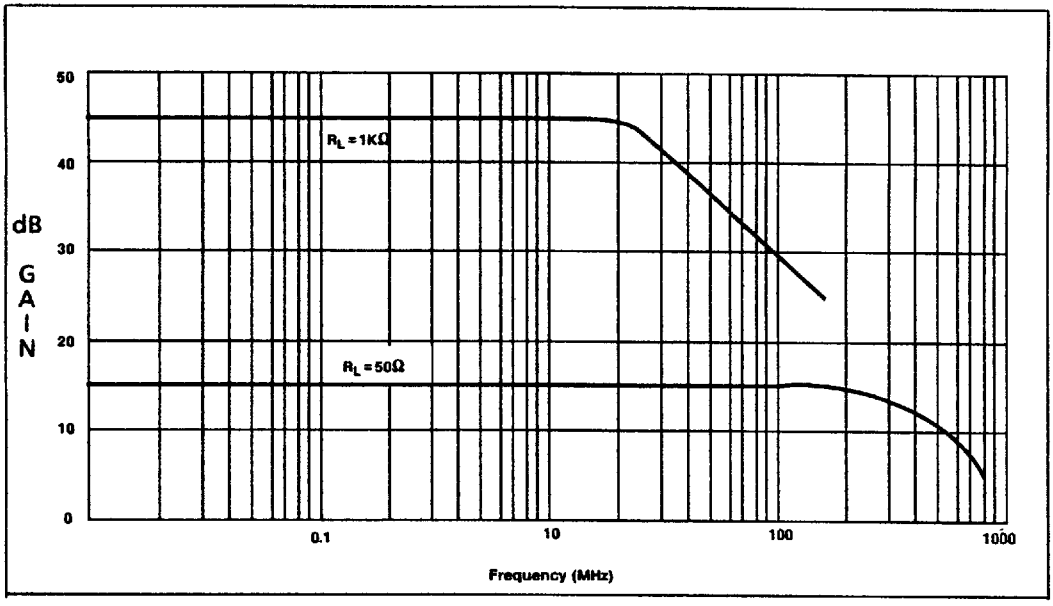

Fig. 6 Voltage Gain V. Frequency

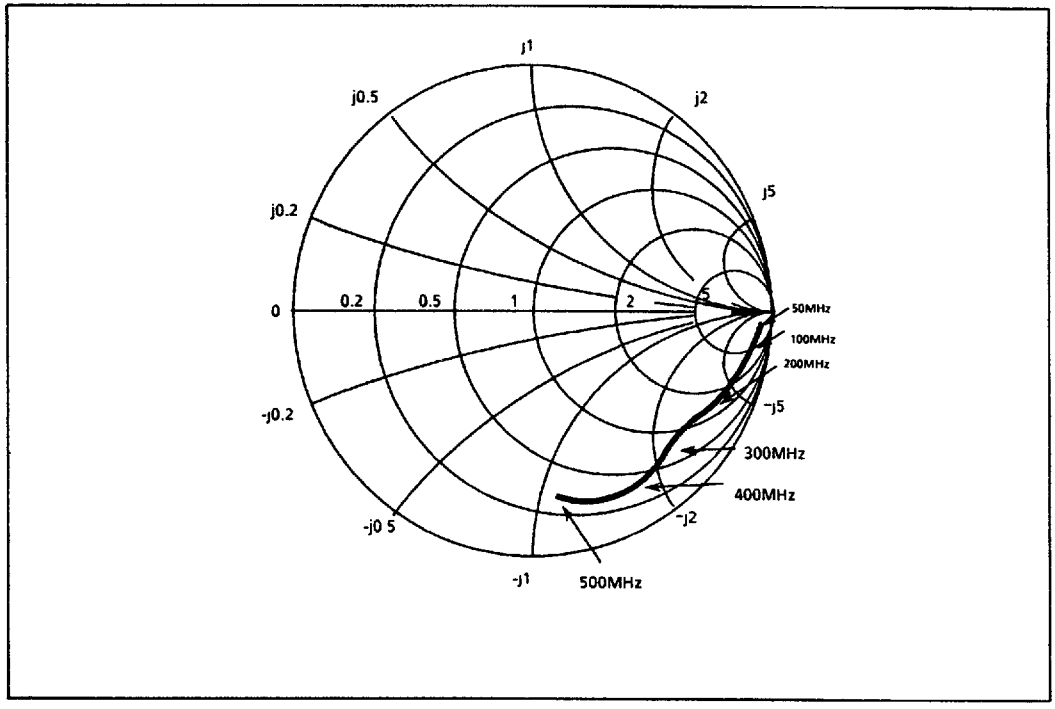

Fig. 7 Input impedance 50Ω system

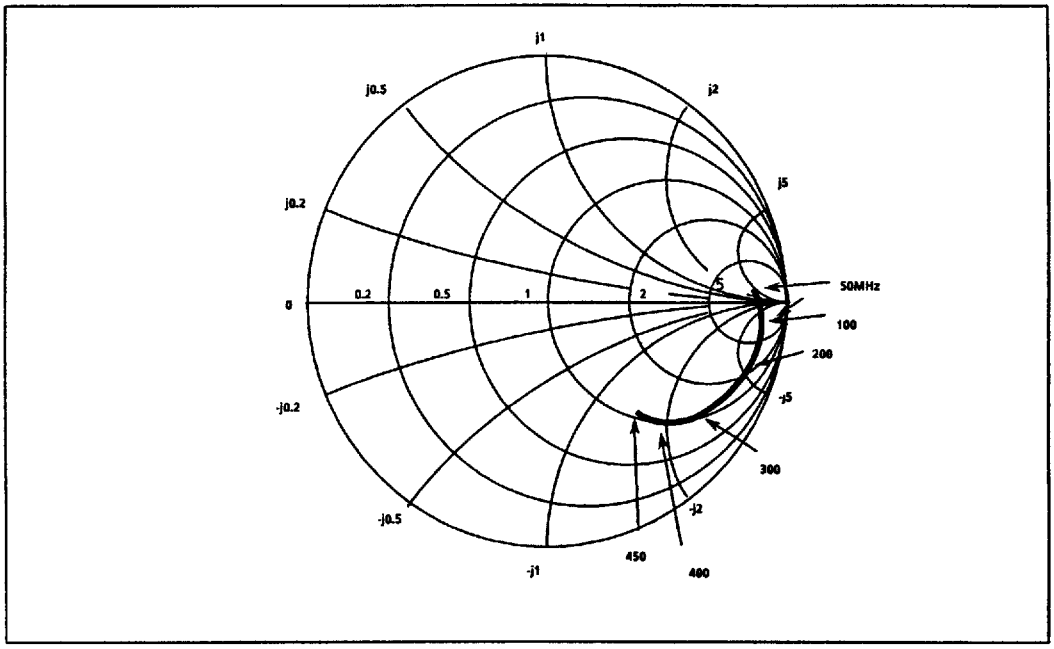

Fig. 8 Output impedance 50Ω system

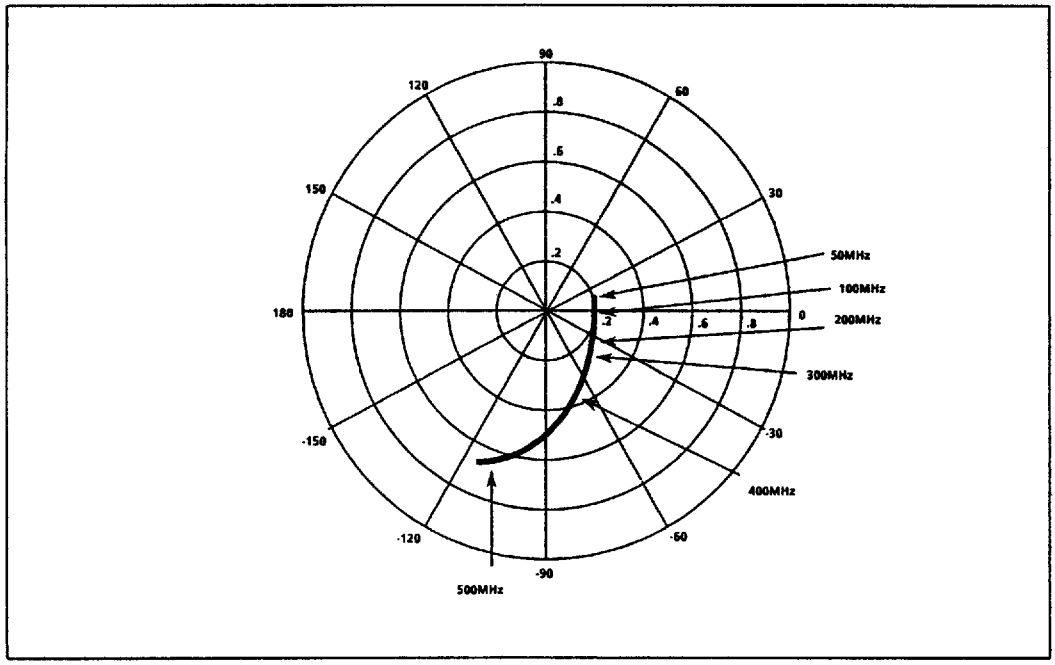

Fig. 9 Reverse transmission coefficient S_{12} SL6140

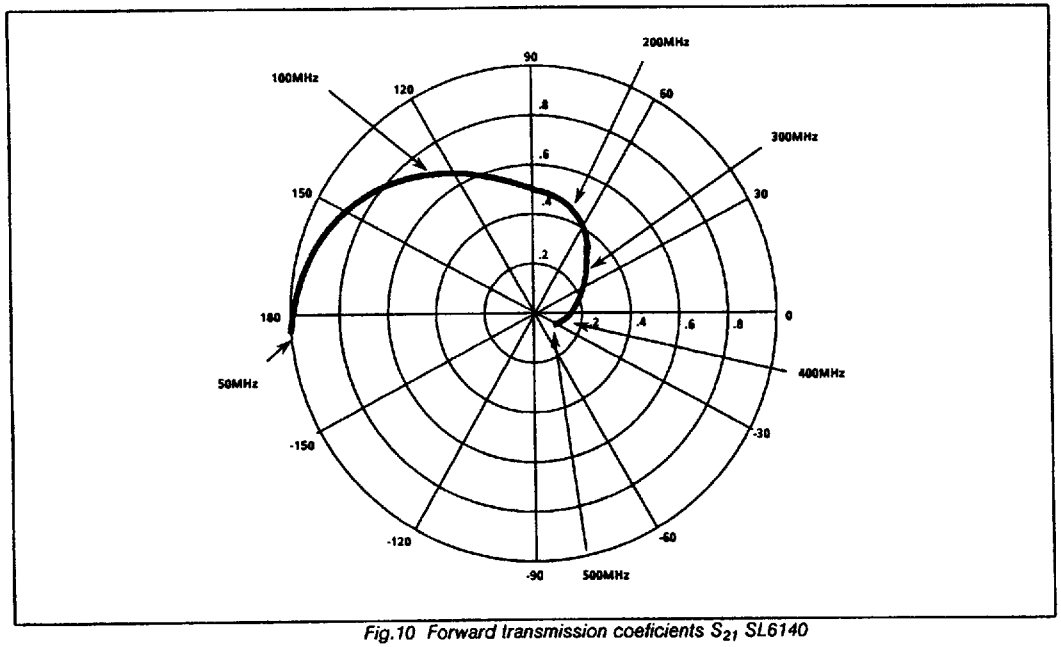

Fig.10 Forward transmission coeficients S_{21} SL6140

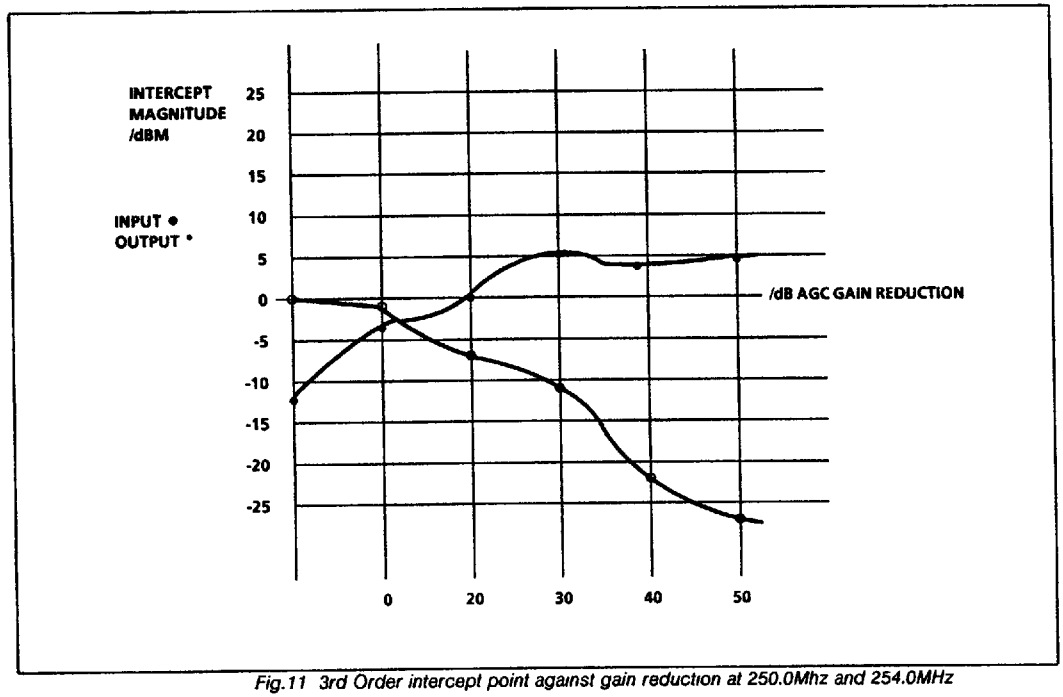

Fig.11 3rd Order intercept point against gain reduction at 250.0Mhz and 254.0MHz

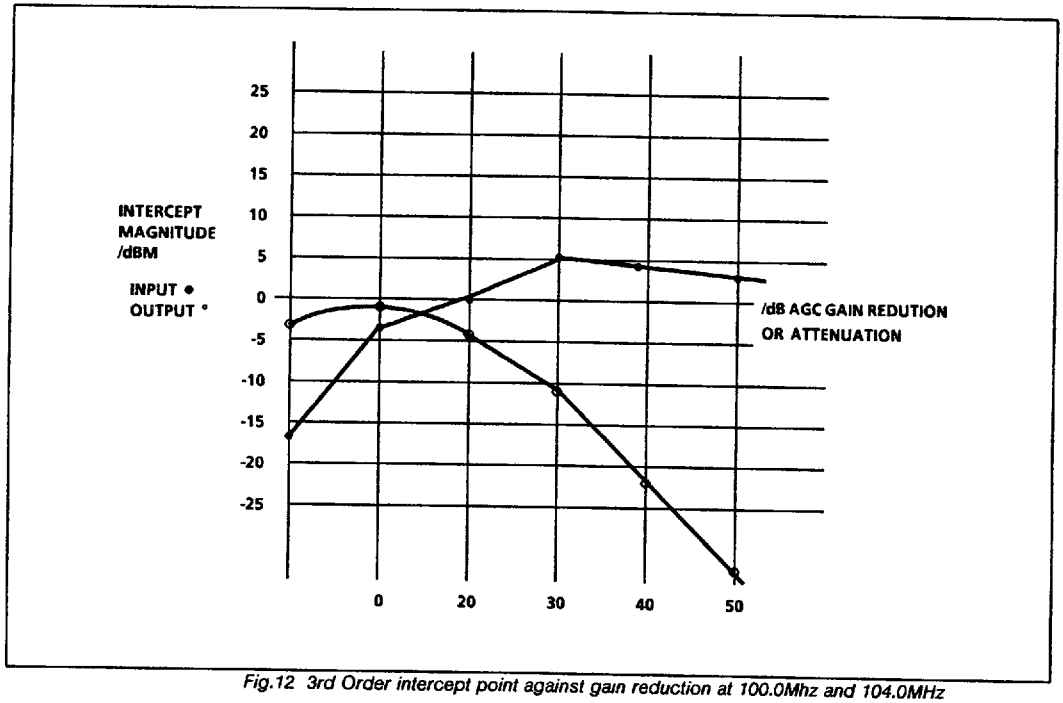

Fig.12 3rd Order intercept point against gain reduction at 100.0Mhz and 104.0MHz

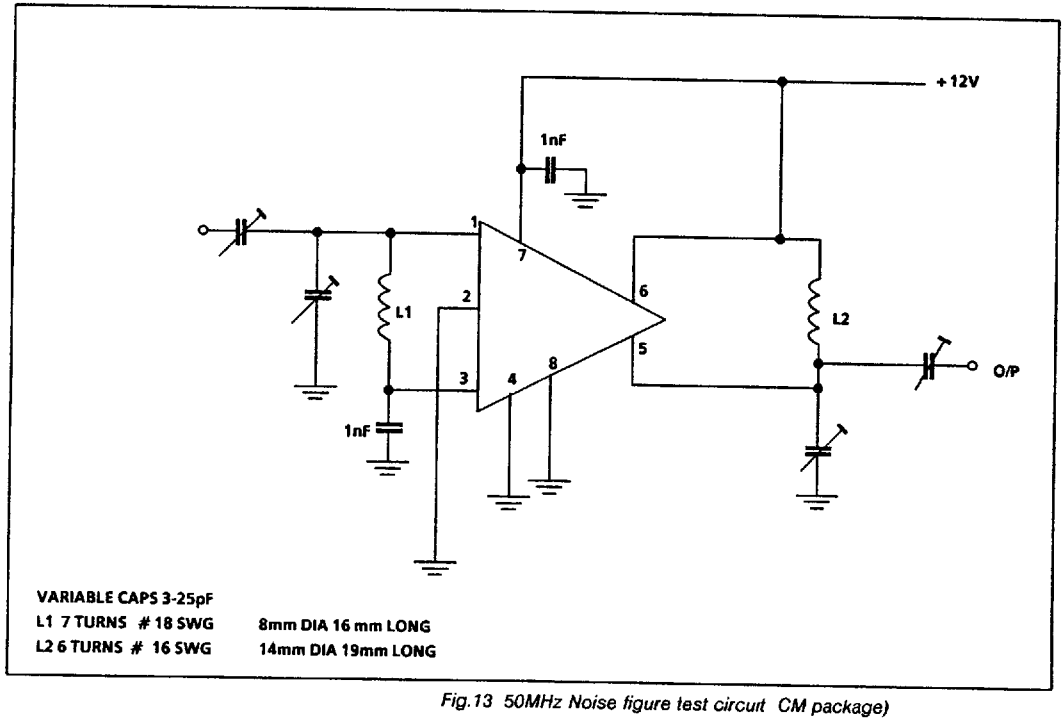

Fig.13 50MHz Noise figure test circuit CM package)