

MC74LVX393

Product Preview

Dual 4-Bit Binary Ripple Counter

The MC74LVX393 is an advanced high speed CMOS dual 4-bit binary ripple counter fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

This device consists of two independent 4-bit binary ripple counters with parallel outputs from each counter stage. A $\div 256$ counter can be obtained by cascading the two binary counters.

Internal flip-flops are triggered by high-to-low transitions of the clock input. Reset for the counters is asynchronous and active-high. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used as clocks or as strobes except when gated with the Clock of the LVX393.

The inputs tolerate voltages up to 7 V, allowing the interface of 5 V systems to 3 V systems.

- High Speed: $f_{\max} = 90$ MHz (Typ) at V_{CC}
- Low Power Dissipation: $I_{CC} = 4$ μ A (Max) at $T_A = 25^\circ\text{C}$
- High Noise Immunity: $V_{NIH} = V_{NIL} = 28\% V_{CC}$
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2 V to 3.6 V Operating Range
- Low Noise: $V_{OLP} = 0.8$ V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- Chip Complexity: 236 FETs

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.



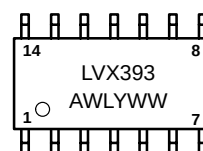
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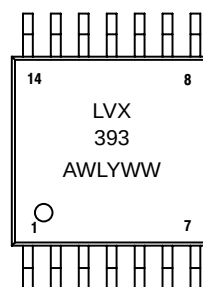
MARKING DIAGRAMS



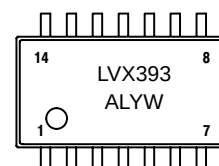
SOIC-14
D SUFFIX
CASE 751A



TSSOP-14
DT SUFFIX
CASE 948G



SOIC EIAJ-14
M SUFFIX
CASE 965



A = Assembly Location
L, WL = Wafer Lot
Y = Year
W, WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC74LVX393M	SOIC EIAJ-16	50 Units/Rail
MC74LVX393MEL	SOIC EIAJ-16	2000 Units/Reel

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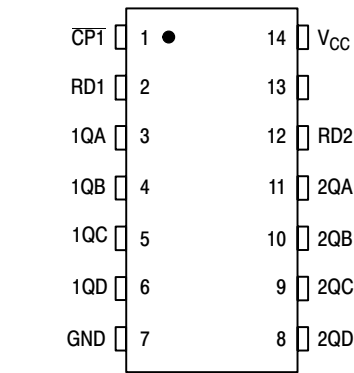


Figure 1. Pin Assignment

Inputs		Outputs
Clock	Reset	
X	H	L
H	L	No Change
L	L	No Change
↑	L	No Change
↓	L	Next State

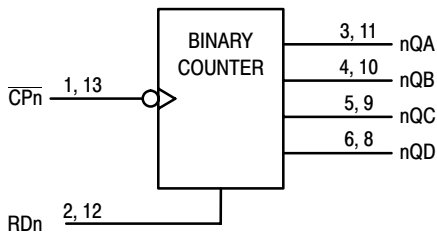


Figure 2. Logic Diagram

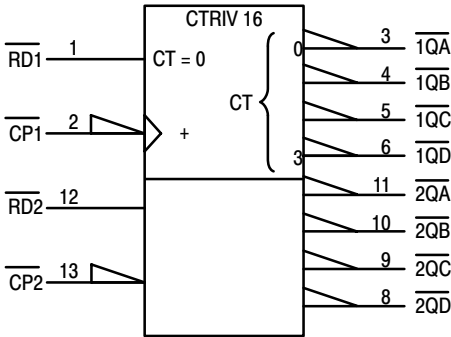


Figure 3. IEC Logic Symbol

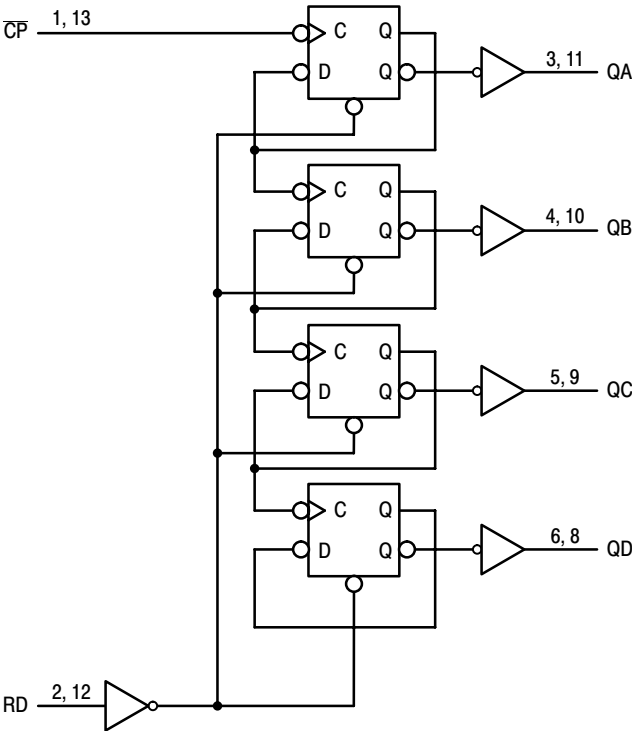


Figure 4. Expanded Logic Diagram

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage	− 0.5 to + 7.0	V
V _{IN}	DC Input Voltage	− 0.5 to + 7.0	V
V _{OUT}	DC Output Voltage	− 0.5 to V _{CC} + 0.5	V
I _{IK}	DC Input Diode Current V _I < GND	− 20	mA
I _{OK}	DC Output Diode Current V _O < GND	± 20	mA
I _{OUT}	DC Output Sink Current	± 25	mA
I _{CC}	DC Supply Current per Supply Pin	± 75	mA
T _{STG}	Storage Temperature Range	− 65 to + 150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C
T _J	Junction Temperature under Bias	+ 150	°C
θ _{JA}	Thermal Resistance (Note 1) SOIC TSSOP	125 170	°C/W
MSL	Moisture Sensitivity	Level 1	
F _R	Flammability Rating Oxygen Index: 30% – 35%	UL–94–VO (0.125 in)	
V _{ESD}	ESD Withstand Voltage Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	> 2000 > 200 N/A	V
I _{Latch-Up}	Latch-Up Performance Above V _{CC} and Below GND at 85°C (Note 5)	± 300	mA

Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm–by–1 inch, 2–ounce copper trace with no air flow.
2. Tested to EIA/JESD22–A114–A.
3. Tested to EIA/JESD22–A115–A.
4. Tested to JESD22–C101–A.
5. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	Supply Voltage	2.0	3.6	V
V _I	Input Voltage (Note 6)	0	5.5	V
V _O	Output Voltage (HIGH or LOW State)	0	5.5	V
T _A	Operating Free–Air Temperature	− 40	+ 125	°C
Δt/ΔV	Input Transition Rise or Fall Rate V _{CC} = 3.0 V ± 0.3 V	0	100	ns/V

6. Unused inputs may not be left open. All inputs must be tied to a high– or low–logic input voltage level.

NOTE: The θ_{JA} of the package is equal to 1/Derating. Higher junction temperatures may affect the expected lifetime of the device per the table and figure below.

DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

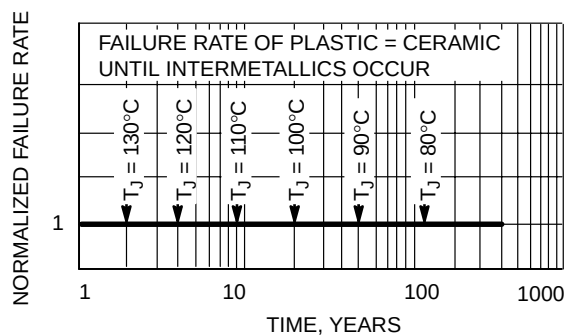


Figure 5. Failure Rate vs. Time Junction Temperature

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DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	V _{CC} (V)	T _A = 25°C			−40°C ≤ T _A ≤ 85°C		T _A ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V _{IH}	High-Level Input Voltage		2.0 to 5.5	0.72 V _{CC}			0.72 V _{CC}		0.72 V _{CC}		V
V _{IL}	Low-Level Input Voltage		2.0 to 5.5			0.28 V _C c		0.28 V _{CC}		0.28 V _{CC}	V
V _{OH}	High-Level Output Voltage V _{IN} = V _{IL} or V _{IH}	I _{OH} = 50 μA	2.0 to 5.5	V _{CC} − 0.1	V _{CC}		V _{CC} − 0.1				V
		I _{OH} = −4 mA	2.3	1.9	2.1		1.9				
		I _{OH} = −8 mA	2.7	2.2	2.4		2.2				
V _{OL}	Low-Level Output Voltage V _{IN} = V _{IL} or V _{IH}	I _{OL} = 50 μA	2.0 to 5.5			0.1		0.1			V
		I _{OL} = −4 mA	3.0			0.36		0.44			
		I _{OL} = −8 mA	4.5			0.36		0.44			
		I _{OL} = 16 mA	3.0		0.28	0.4		0.4			
		I _{OL} = 24 mA	3.0		0.38	0.55		0.55			
		I _{OL} = 32 mA	4.5		0.42	0.55		0.55			
I _{IN}	Input Leakage Current	V _{IN} = V _{CC} or GND	0 to 5.5			±0.1		±1.0			μA
I _{OFF}	Power Off-Output Leakage Current	V _{OUT} = 5.5 V	0			1		10			μA
I _{CC}	Quiescent Supply Current	V _{IN} = V _{CC} or GND	5.5			1		10			μA

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AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns)

Symbol	Parameter	Test Conditions	$T_A = 25^\circ\text{C}$			$T_A \leq 85^\circ\text{C}$		$T_A \leq 125^\circ\text{C}$		Unit
			Min	Typ	Max	Min	Max	Min	Max	
$f_{\max}$	Maximum Clock Frequency (50% Duty Cycle)	$V_{CC} = 3.3 \pm 0.3$ V $C_L = 15$ pF $C_L = 50$ pF	75 45	120 65		65 35		65 35		MHz
		$V_{CC} = 5.0 \pm 0.5$ V $C_L = 15$ pF $C_L = 50$ pF	125 85	170 115		105 75		105 75		
t_{PLH} , t_{PHL}	Maximum Propagation Delay, CP to QA	$V_{CC} = 3.3 \pm 0.3$ V $C_L = 15$ pF $C_L = 50$ pF		8.6 11.1	13.2 16.7	1.0 1.0	15.5 19.0	1.0 1.0	15.5 19.0	ns
		$V_{CC} = 5.0 \pm 0.5$ V $C_L = 15$ pF $C_L = 50$ pF		5.8 7.3	8.5 10.5	1.0 1.0	10.0 12.0	1.0 1.0	10.0 12.0	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, CP to QB	$V_{CC} = 3.3 \pm 0.3$ V $C_L = 15$ pF $C_L = 50$ pF		10.2 12.7	15.8 19.3	1.0 1.0	18.5 22.0	1.0 1.0	18.5 22.0	ns
		$V_{CC} = 5.0 \pm 0.5$ V $C_L = 15$ pF $C_L = 50$ pF		6.8 8.3	9.8 11.8	1.0 1.0	11.5 13.5	1.0 1.0	11.5 13.5	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, CP to QC	$V_{CC} = 3.3 \pm 0.3$ V $C_L = 15$ pF $C_L = 50$ pF		11.7 14.2	18.0 21.5	1.0 1.0	21.0 24.5	1.0 1.0	21.0 24.5	ns
		$V_{CC} = 5.0 \pm 0.5$ V $C_L = 15$ pF $C_L = 50$ pF		7.7 9.2	11.2 13.2	1.0 1.0	13.0 15.0	1.0 1.0	13.0 15.0	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, CP to QD	$V_{CC} = 3.3 \pm 0.3$ V $C_L = 15$ pF $C_L = 50$ pF		13.0 15.5	19.7 23.2	1.0 1.0	23.0 26.5	1.0 1.0	23.0 26.5	ns
		$V_{CC} = 5.0 \pm 0.5$ V $C_L = 15$ pF $C_L = 50$ pF		8.5 10.0	12.5 14.5	1.0 1.0	14.5 16.5	1.0 1.0	14.5 16.5	
t_{PHL}	Maximum Propagation Delay, RD to QN	$V_{CC} = 3.3 \pm 0.3$ V $C_L = 15$ pF $C_L = 50$ pF		7.9 10.4	12.3 15.8	1.0 1.0	14.5 18.0	1.0 1.0	14.5 18.0	ns
		$V_{CC} = 5.0 \pm 0.5$ V $C_L = 15$ pF $C_L = 50$ pF		5.4 6.9	8.1 10.1	1.0 1.0	9.5 11.5	1.0 1.0	9.5 11.5	
t_{OSLH} , t_{OSHL}	Output to Output Skew (Note 7)	$V_{CC} = 3.3 \pm 0.3$ V $C_L = 50$ pF			1.5		1.5		1.5	pF
		$V_{CC} = 5.0 \pm 0.5$ V $C_L = 50$ pF			1.0		1.0		1.0	
C_{IN}	Maximum Input Capacitance			4	10		10		10	pF
Typical @ 25°C , $V_{CC} = 5.0$ V										
C_{PD}	Power Dissipation Capacitance (Note 8)						23			pF

7. Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$.

8. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC}$. C_{PD} is used to determine the no-load dynamic power consumption; $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} + I_{CC} \cdot V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns, $C_L = 50$ pF, $V_{CC} = 5.0$ V)

Symbol	Parameter	$T_A = 25^\circ\text{C}$		Unit
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.5	0.8	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	-0.5	-0.8	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		3.5	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		1.5	V

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TIMING REQUIREMENTS (Input $t_r = t_f = 3.0$ ns)

Symbol	Parameter	Test Conditions	$T_A = 25^\circ\text{C}$		$T_A \leq 85^\circ\text{C}$	$T_A \leq 125^\circ\text{C}$	Unit
			Typ	Limit	Limit	Limit	
t_w	Minimum Pulse Width, $\overline{\text{CP}}$	$V_{CC} = 3.3 \pm 0.3$ V $V_{CC} = 5.0 \pm 0.5$ V		5.0 5.0	5.0 5.0	5.0 5.0	ns
t_w	Minimum Pulse Width, RD	$V_{CC} = 3.3 \pm 0.3$ V $V_{CC} = 5.0 \pm 0.5$ V		5.0 5.0	5.0 5.0	5.0 5.0	ns
t_{rec}	Minimum Recovery Time, RD to $\overline{\text{CP}}$	$V_{CC} = 3.3 \pm 0.3$ V $V_{CC} = 5.0 \pm 0.5$ V		5.0 4.0	5.0 4.0	5.0 4.0	ns
t_r, t_f	Minimum Input Rise and Fall Times	$V_{CC} = 3.3 \pm 0.3$ V $V_{CC} = 5.0 \pm 0.5$ V		330 100	330 100	330 100	ns

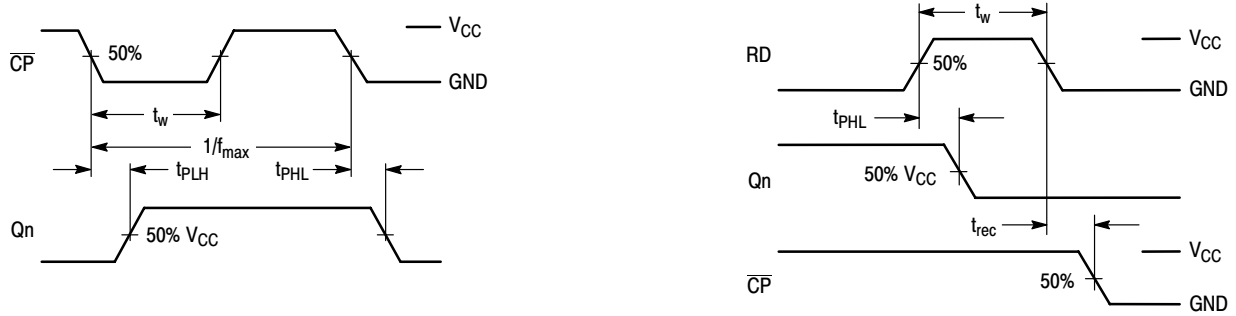
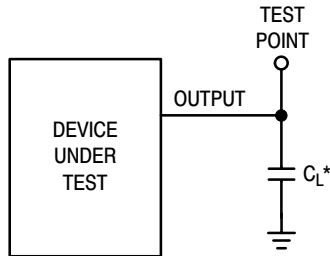


Figure 6. Switching Waveforms



*Includes all probe and jig capacitance

Figure 7. Test Circuit

MC74LVX393

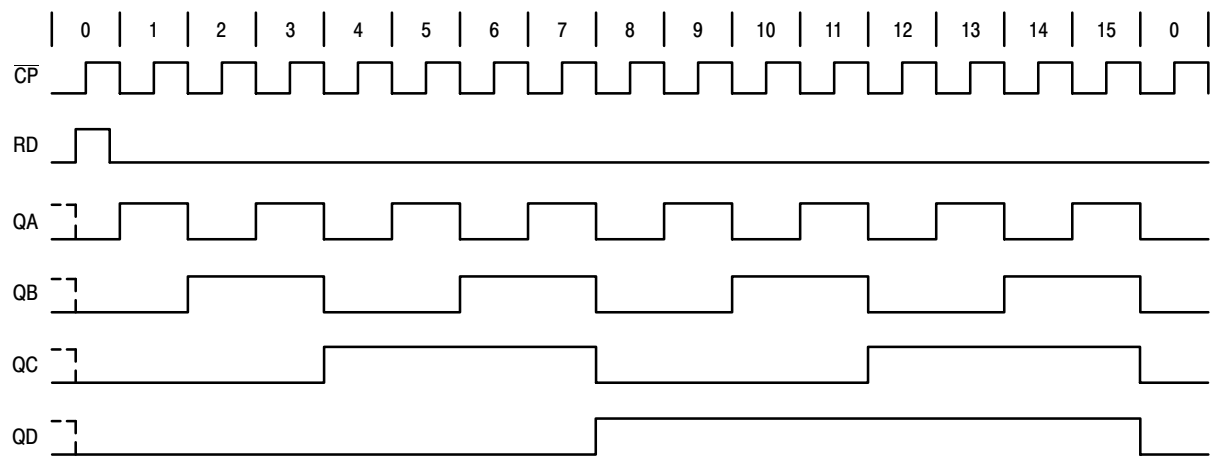


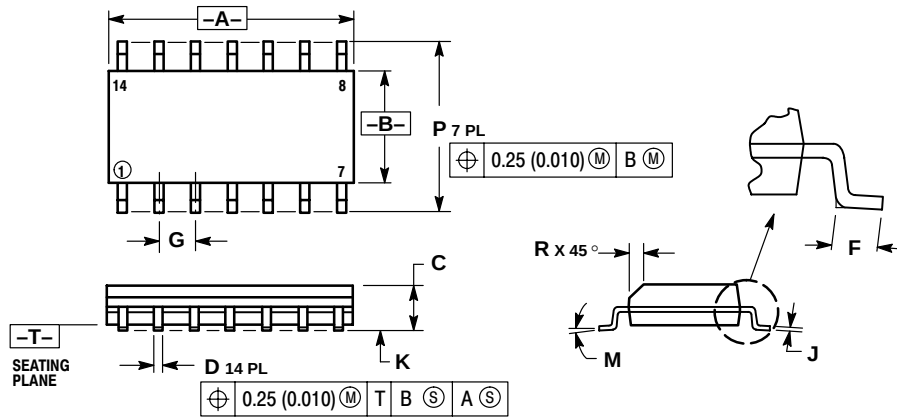
Figure 8. Timing Diagram

COUNT SEQUENCE				
Count	Outputs			
	QD	QC	QB	QA
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

MC74LVX393

PACKAGE DIMENSIONS

SOIC-14
D SUFFIX
CASE 751A-03
ISSUE F



NOTES:

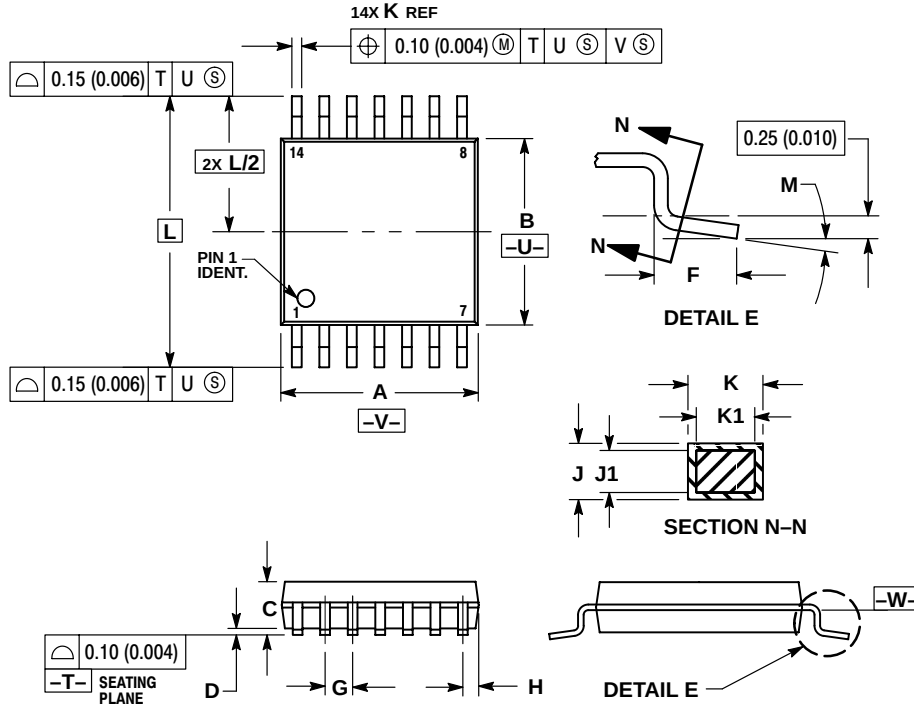
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2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

MC74LVX393

PACKAGE DIMENSIONS

TSSOP
DT SUFFIX
CASE 948G-01
ISSUE O



NOTES:

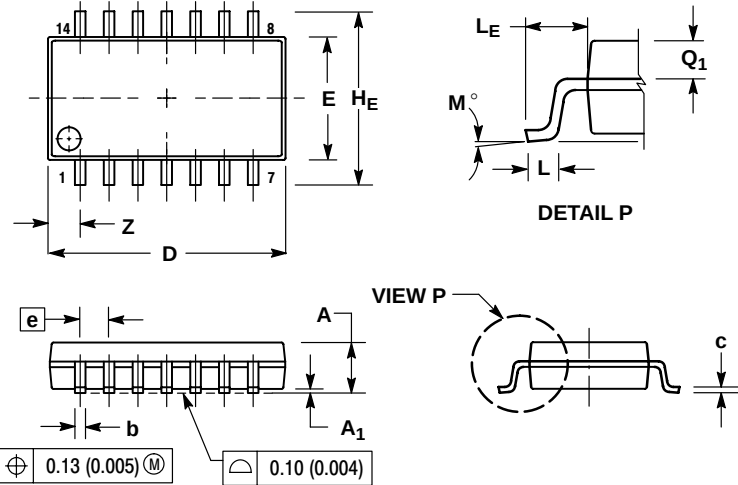
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

MC74LVX393

PACKAGE DIMENSIONS

SO-14
M SUFFIX
CASE 965-01
ISSUE O



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A ₁	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H _E	7.40	8.20	0.291	0.323
0.50	0.50	0.85	0.020	0.033
L _E	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q ₁	0.70	0.90	0.028	0.035
Z	---	1.42	---	0.056

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