μPD77220, 77P220
24-Bit Fixed-Point Digital Signal Processor

Description

The μPD77220 is a highly accurate digital signal processor (DSP). The μPD77220 has a mask ROM; the μPD77P220 has a one-time programmable (OTP) or an ultraviolet erasable (UVE) PROM. There are also two speed versions, 8 and 10 MHz. The part numbers of 10-MHz versions have a -10 suffix. The 8- and 10-MHz units process 24-bit fixed-point data at 122 and 100 ns/instruction.

Note: Unless excluded by context, μPD77220 means both the μPD77220 and the μPD77P220.

The internal circuit consists of a multiplier (24 x 24 bits), instruction ROM (2K words x 32 bits), data ROM (1K words x 24 bits), and two independent data RAMs (256 words x 24 bits each).

The μPD77220 has two operation modes: master and slave. These modes can be set using external pins. In master mode, an external 8K-word memory can be added, and 4K words in the memory can be used as an instruction area. In slave mode, the μPD77220 operates as an I/O processor for the host CPU. An external 8K-byte data memory can be added.

Features

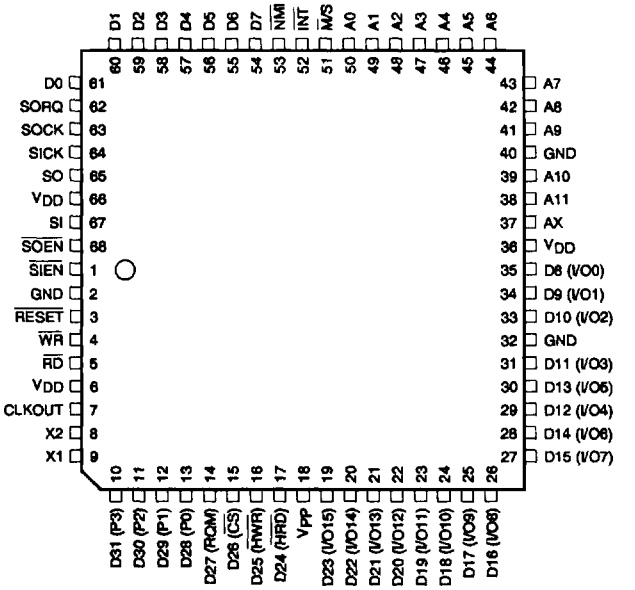
- Processes 24-bit fixed-point data
  - 24-bit fixed-point multiplication circuit
    24 bits x 24 bits → 47 bits
  - 47-bit ALU with eight working registers
  - 47-bit barrel shifter
- High-speed operation and efficient data transfer
  - Instruction cycle 122 or 100 ns
  - Three-stage pipeline processing
  - Dedicated data buses in the internal RAM, multiplication circuit, and ALU
- Architecture suitable for digital signal processing
  - Two built-in independent data RAMs and data RAM pointers
  - Each data RAM pointer consists of a base pointer and index register: the base pointer performs a ring count operation in any range
  - Data ROM pointer steps forward in two-step increments (2N) in addition to normal autoincrement/autodecrement addressing
- Flexible external interfaces
- Two modes of operation: master or slave
  - In master mode, 4K words by 32-bit instruction area
  - High-speed access to external memory
    Master mode: 4K words by 24 bits
    Slave mode: 4K words by 8 bits
- CMOS process
- Single +5-volt single power supply
- 68-pin PGA array and PLCC packages

Ordering Information

Part Number	Package	Max Speed	ROM
μPD77220R	68-pin PGA	8 MHz	Mask
L	68-pin PLCC	8 MHz	
R-10	68-pin PGA	10 MHz	
L-10	68-pin PLCC	10 MHz	
μPD77P220R	68-pin PGA	8 MHz	UVE
L	68-pin PLCC	8 MHz	OTP
R-10	68-pin PGA	10 MHz	UVE
L-10	68-pin PLCC	10 MHz	OTP

Pin Configurations

68-Pin PLCC



Notes:
The symbol in ( ) denotes the pin symbol applicable to the pin in the Slave mode.
The Vpp pin is only used for the μPD77P220.

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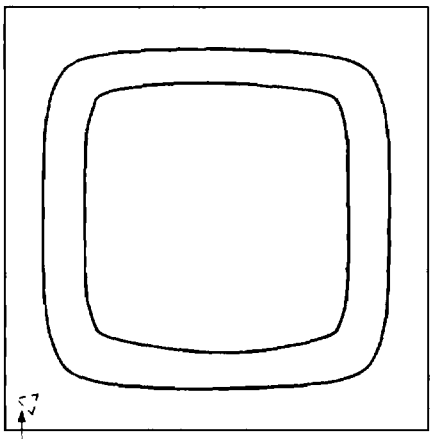
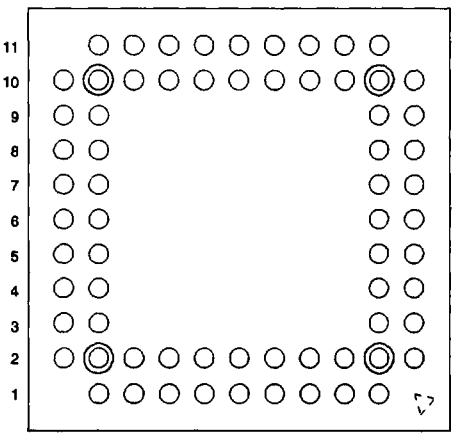
Pin Configurations (cont)

68-Pin Ceramic PGA





Terminal No.	Terminal Symbol: Master Mode	Terminal Symbol: Slave Mode	Terminal No.	Terminal Symbol: Master Mode	Terminal Symbol: Slave Mode	Terminal No.	Terminal Symbol: Master Mode	Terminal Symbol: Slave Mode	Terminal No.	Terminal Symbol: Master Mode	Terminal Symbol: Slave Mode
A_2	A_7		B_9	D_{13}	I/O_5	F_{10}	D_{23}	I/O_{15}	K_4	V_{DD}	
A_3	A_9		B_{10}	D_{14}	I/O_6	F_{11}	V_{PP}		K_5	$\overline{SOEN}$	
A_4	A_{10}		B_{11}	D_{15}	I/O_8	G_1	D_7		K_6	GND	
A_5	A_{AX}		C_1	A_4		G_2	D_6		K_7	$\overline{WR}$	
A_6	D_8	I/O_0	C_2	A_3		G_{10}	D_{24}	$\overline{HRD}$	K_8	V_{DD}	
A_7	D_{10}	I/O_2	C_{10}	D_{17}	I/O_9	G_{11}	D_{25}	$\overline{HWR}$	K_9	X2	
A_8	D_{11}	I/O_3	C_{11}	D_{18}	I/O_{10}	H_1	D_5		K_{10}	D_{30}	P_2
A_9	D_{12}	I/O_4	D_1	A_2		H_2	D_4		K_{11}	D_{31}	P_3
A_{10}	D_{15}	I/O_7	D_2	A_1		H_{10}	D_{26}	$\overline{CS}$	L_2	D_0	
A_1	A_8		D_{10}	D_{19}	I/O_{11}	H_{11}	D_{27}	RQM	L_3	SOCK	
B_2	A_5		D_{11}	D_{20}	I/O_{12}	J_1	D_3		L_4	SO	
B_3	A_8		E_1	A_0		J_2	D_2		L_5	SI	
B_4	GND		E_2	$\overline{M/S}$		J_{10}	D_{28}	P_0	L_6	$\overline{SIEN}$	
B_5	AI1		E_{10}	D_{21}	I/O_{13}	J_{11}	D_{29}	P_1	L_7	$\overline{RESET}$	
B_6	V_{DD}		E_{11}	D_{22}	I/O_{14}	K_1	D_1		L_8	$\overline{RD}$	
B_7	D_9	I/O_1	F_1	$\overline{INT}$		K_2	SORQ		L_9	CLKOUT	
B_8	GND		F_2	$\overline{NMI}$		K_3	SICK		L_{10}	X1	

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μPD77220 and μPD77230A Comparison

The μPD77220 is a 24-bit fixed-point signal processor; the μPD77230A is a 32-bit floating-point signal processor. The two processors are generally compatible on an object level. However, the following μPD77230A instructions are not available on the μPD77220.
ADDF, SUBF, NORM, CVT (OP field)

- TRNORM, RDNORM, FLTFIX, FIXMA (CNT field)
- SPIE, IESP (CNT field)
- WRBEL8, WRBL8E (CNT field)
- JEV0, JEV1 (C field)
- TRE (DST field)

Also, the CMP instruction on the μPD77220 treats data as 47-bit fixed-point data at the time of comparison (as opposed to 55-bit floating-point data on the μPD77230A).

Internal memory differences between the two processors are shown in table 1. Table 2 describes the differences in the data lengths between the μPD77220 and the μPD77230A.

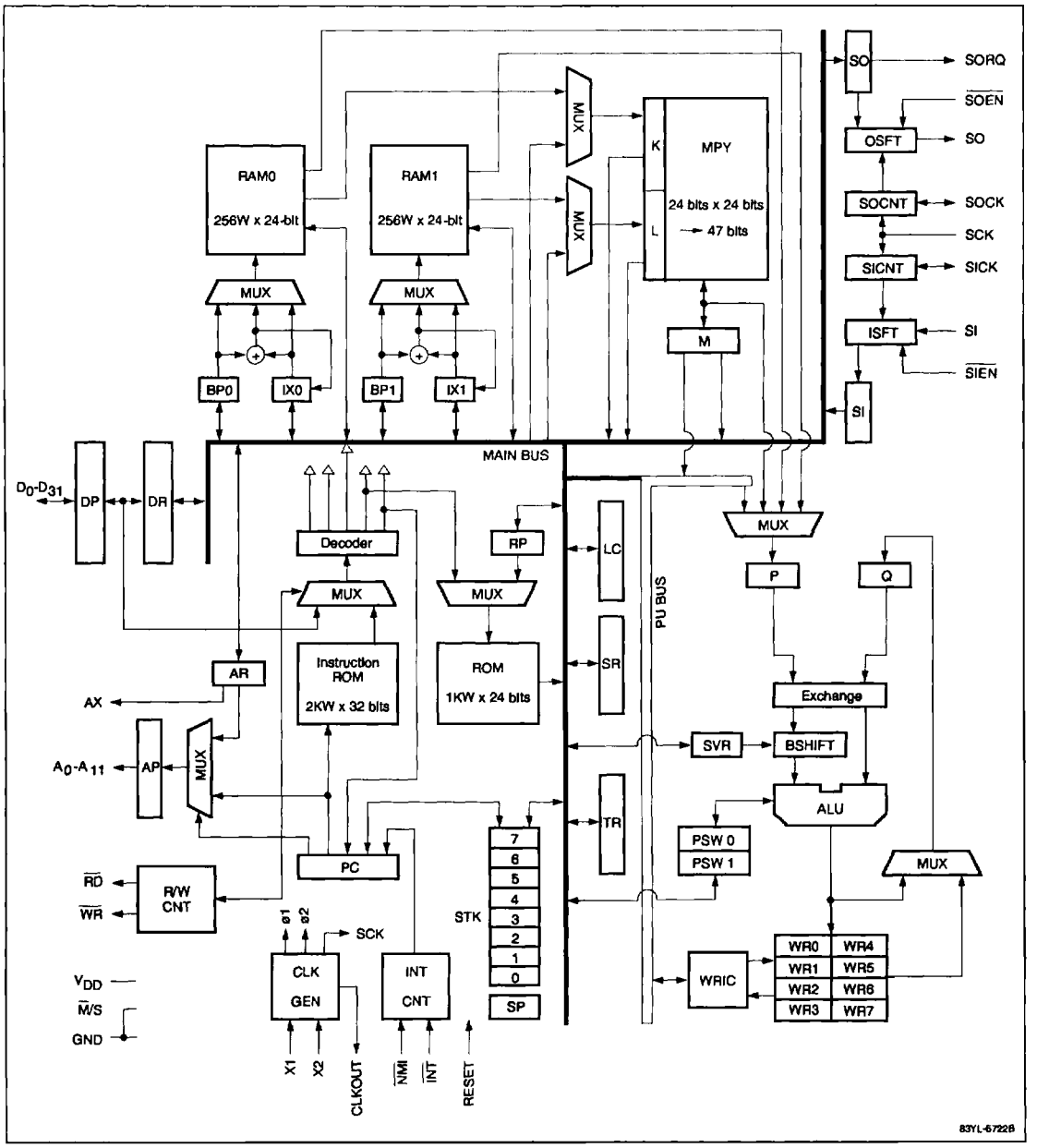
Table 1. Internal Memory Differences Between μPD77220 and μPD77230A

Memory Type	μPD77220	μPD77230A
Instruction ROM	2K words x 32 bits	2K words x 32 bits
Data ROM	1K words x 24 bits	1K words x 32 bits
RAM 0	256 x 24 bits	512 x 32 bits
RAM 1	256 x 24 bits	512 x 32 bits

Table 2. Data Length Differences Between μPD77220 and μPD77230A

Symbol	μPD77220	μPD77230A
MAIN BUS	24 bits	32 bits
P, Q	47 bits	55 bits
PSW0, PSW1	4 bits (OVFE not present)	5 bits
RAM0, RAM1	24 bits	32 bits
IX0, IX1	9 bits	←
RP	10 bits	←
M	47 bits	55 bits
DRS	32 bits	←
SI, SO	32 bits	←
LC	10 bits	←
TR	24 bits	32 bits
PU BUS	47 bits	55 bits
WR0 - WR7	47 bits	55 bits
SVR	7 bits	←
BP0, BP1	9 bits	←
ROM	24 bits	32 bits
K, L	24 bits	32 bits
DR	32 bits	←
AR	13 bits	←
STK	13 bits	←
SR	20 bits	←

Master Mode Block Diagram



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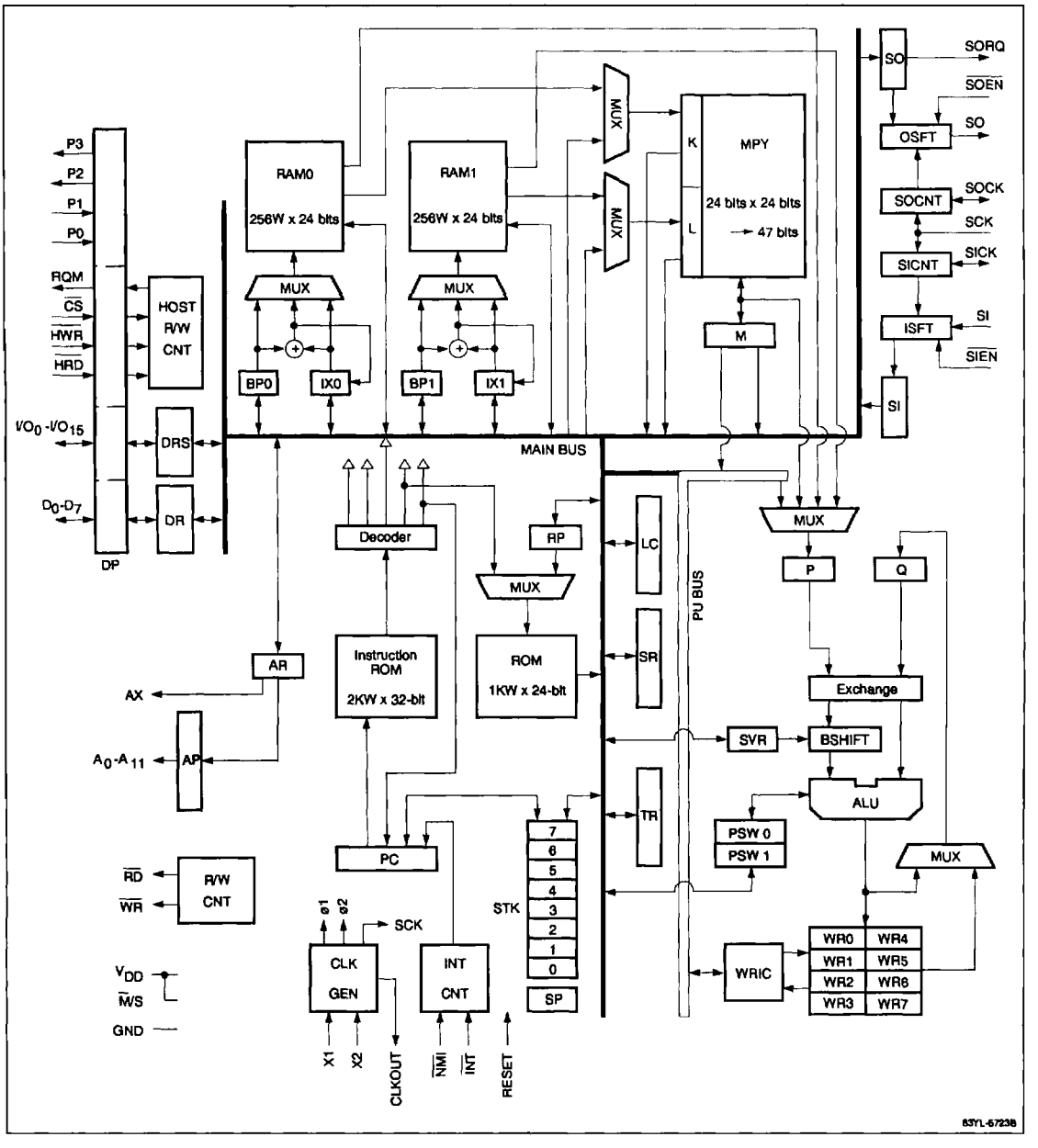
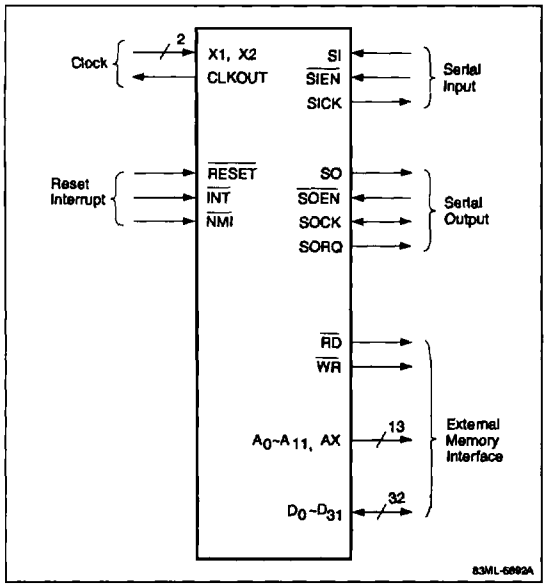
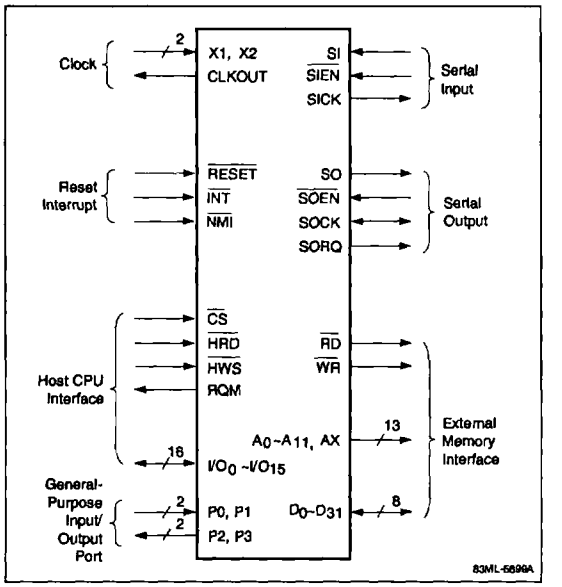
Slave Mode Block Diagram



Master Mode Operation



Slave Mode Operation



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Pin Functions

Symbol	PGA Pin Location	PLCC Pin Number	I/O	Function
Power Supply				
V_{DD}	B6	36	—	+5 V power supply Be sure to connect these three pins
	K4	66	—	
	K8	6	—	
V_{PP}	F11	18	—	PROM program power input pin. Connect +5 V for normal operation or +12.5 V for PROM program mode
GND	B4	40	—	Ground terminals Be sure to ground these three pins
	B8	32	—	
	K6	2	—	
Setting Modes				
$\overline{M}$/S	E2	51	I	Operation mode; mode cannot be changed during operation 0: Master mode 1: Slave mode
Clocks				
X1	L10	9	I	Input pins for crystal oscillator connection If an external clock is used, connect it to the X1 pin and leave X2 open
X2	K9	8	—	
CLKOUT	L9	7	O	μPD77220 internal system clock output. The output signal frequency is half the frequency of the crystal oscillator connected to the X1 or X2 pin
Reset and Interrupt				
$\overline{RESET}$	L7	3	I	Internal system reset signal input (low-level active) — Requires latitude of more than three system clock (CLKOUT) cycles

Pin Functions (cont)

Symbol	PGA Pin Location	PLCC Pin Number	I/O	Function
$\overline{NMI}$	F2	53	I	Non-maskable interrupt input (low-level active) — Requires latitude of more than three system clock (CLKOUT) cycles — Fall edge detection — The interrupt address is 10H
$\overline{INT}$	F1	52	I	Maskable interrupt input (low-level active) — Requires latitude of more than three system clock (CLKOUT) cycles — Fall edge detection — The interrupt address is 100H
Serial Interfaces				
SOCK	L3	63	I/O	Serial output data clock I/O — Serial data is output synchronously when the clock to be input or output at this pin rises — Whether the external clock is to be input or the internal clock to be output depends on the status register
SORQ	K2	62	O	Serial output request (high-level active) — When output data is in the SO register, set to 1 When output is terminated, set to 0
$\overline{SOEN}$	K5	68	I	Serial output enable (low-level active) — Enables serial data output from the SO pin
SO	L4	65	O (3 state)	Serial data output — Serial data output is synchronized with the leading edge of the SOCK signal
SICK	K3	64	I/O	Serial input data clock I/O — Serial data is latched internally at the trailing edge of the clock input to or output from this terminal — The status register determines whether to input the external clock or to output the internal clock
$\overline{SIEN}$	L6	1	I	Serial input enable (low-level active) — Enables serial data input from the SI pin
SI	L5	67	I	Serial data input — Inputs serial data synchronously when SICK falls

Note: The system clock is an internal clock generated by CLK GEN on the basis of the clock (master clock hereafter) input in X1. Its frequency is half of that of the master clock.

External Memory Interfaces (Master Mode Only)				
$\overline{WR}$	K7	4	O	Write output (low-level active) — Write control output for external memory. If 0 is set, the output address is valid and data is output to data bus (D0 to D31)
$\overline{RD}$	L8	5	O	Read output (low-level active) — Read output control for the external memory. If 0 is set, the output address is valid and data is output to data bus (D0 to D31)
AX	A5	37	O	Highest-order memory address output — If the external instruction memory is accessed (highest-order bit PC12 of the internal program counter is 1), 0 is output — If the external data memory is accessed, the value of the highest-order bit AR12 of the internal address register is output 0: High-speed access area 1: Low-speed access area

Pin Functions (cont)

Symbol	PGA Pin Location	PLCC Pin Number	I/O	Function
External Memory Interfaces (Master Mode Only) (cont)				
A0 - A11	See PGA pin configuration diagram	See PLCC pin configuration diagram	O (3 state)	Memory address output — Address output when the external memory is accessed — If the external instruction memory is accessed, the value of low-order 12 bits of the internal program counter is output — If the external data memory is accessed, the value of low-order 12 bits of the address register is output
D0 - D31	See PGA pin configuration diagram	See PLCC pin configuration diagram	I/O (3 state)	32-bit data bus for the external memory
Host CPU Interfaces (Slave Mode Only)				
$\overline{CS}$	H10	15	I	Chip select input (low-level active) — If 0 is set, read/write from host CPU through 16-bit data bus (I/O0 to I/O15) is enabled
$\overline{HWR}$	G11	16	I	Host CPU write input (low-level active) — If 0 is set, 16-bit data bus (I/O0 to I/O15) is ready for input (also $\overline{CS}$ = 0)
$\overline{HRD}$	G10	17	I	Host CPU read input (low-level active) — If 0 is set, 16-bit data bus (I/O0 to I/O15) is ready for output (for $\overline{CS}$ = 0)
I/O0 to I/O15	See PGA pin configuration diagram	See PLCC pin configuration diagram	I/O (3 state)	16-bit data buses for host CPU — Bidirectional buses that input and output data according to control signals $\overline{CS}$, $\overline{HWR}$, and $\overline{HRD}$ from the host CPU — 16-bit or 32-bit I/O data transfer format can be set in the internal status register
RQM	H11	14	O	Host request input — Signal that indicates a read or write request to host CPU
External Data Memory Interfaces (Slave Mode Only)				
$\overline{WR}$	K7	4	O	Write data output (low-level active) — Write control output for the external memory. If set to 0, the output address is valid and data is output to data buses (D0 to D7)
$\overline{RD}$	L8	5	O	Read data output (low-level active) — Read control output for the external memory. If set to 0, the output address is valid and data is input through data buses (D0 to D7)
AX	A5	37	O	Highest-order memory address output — If the external memory is accessed, the value of the highest-order bit AR12 of the internal address register is output 0: High-speed access area 1: Low-speed access area
A0 - A11	See PGA pin configuration diagram	See PLCC pin configuration diagram	O	Memory address output — Address output when the external memory is accessed. The value of the low-order 12 bits of the internal address resister is output from this address
D0 - D7	See PGA pin configuration diagram	See PLCC pin configuration diagram	I/O (3 state)	8-bit data bus for external memory — 1-byte, 2-byte, 3-byte, or 4-byte I/O data transfer format can be set in the internal status register

3c

Pin Functions (cont)

Symbol	PGA Pin Location	PLCC Pin Number	I/O	Function
General-Purpose I/O Ports (Slave Mode Only)				
P0, P1	J10, J11	13, 12	I	General-purpose input port — The status of these general-purpose input ports can be determined by an instruction
P2, P3	K10, K11	11,10	O	General-purpose output port — Data to be output from these general-purpose output pins can be set using an instruction; the data is stored unless the set value is changed

Internal Functions

Symbol	Multiplier	Description
Multiplier Peripheral Circuits		
MPY	Multiplier	24-bit fixed-point data multiplier
		24 bits x 24 bits → 47 bits
K	K Register	MPY input data storage register (24 bits)
L	L Register	MPY input data storage register (24 bits)
M	M Register	MPY multiplication result storage register (47 bits)
ALU Peripheral Circuits		
ALU	Arithmetic Logic Unit	47-bit data logical operation circuit
P	P Register	ALU input data storage register (47 bits)
Q	Q Register	ALU input data storage register (47 bits)
EXCHANGE	Data Exchanger	Selects P or Q from which the fixed-point data is to be input to the barrel shifter
BSHIFT	Barrel Shifter	Barrel shifter for fixed-point data in the P or Q register
SVR	Shift Value Register	Shift value set register
WRIC	Working Register Interface Circuit	Specifies the format of data transfer between the working register and PU bus
WR0 - WR7	Working Register (0-7)	ALU operation result storage register (47 bits)
PSW0	Program Status Word 0	ALU operation result status register
PSW1	Program Status Word 1	ALU operation result status register
Data Memory Peripheral Circuits		
ROM	Data ROM	Fixed-data storage ROM (1 kW x 24 bits)
RP	ROM Pointer	Register specifying ROM address (10 bits)
RAM0	Data RAM0	Data storage RAM0 (256 W x 24 bits)
BP0	Base Pointer 0	Register specifying RAM0 base address (9 bits)
IX0	Index Register 0	Register specifying RAM0 index address (9 bits)
RAM1	Data RAM1	Data storage RAM1 (256 W x 24 bits)
BP1	Base Pointer 1	Register specifying RAM1 base address (9 bits)
IX1	Index Register 1	Register specifying RAM1 index address (9 bits)
Instruction ROM Peripheral Circuits		
INSTRUCTION ROM	Instruction ROM	Instruction storage ROM (2 kW x 32 bits)
PC	Program Counter	Register specifying instruction ROM address (13 bits)
STK	Stack	8-level 13-bit stack

Internal Functions (cont)

Symbol	Multiplier	Description
Instruction ROM Peripheral Circuits (cont)		
SP	Stack Pointer	Pointer indicating stack address
DECODER	Instruction Decoder	Instruction decoding circuit
Parallel Interface Buses		
DP	Data Port	**Master mode:** — 32-bit parallel data bus for the external memory
		Slave mode: — 8-bit parallel data bus for the external data memory — 16-bit parallel data bus for host CPU — Read/write control signal for host CPU — General-purpose I/O port
AP	Address Port	**Master mode:** — Address bus for the external memory
		Slave mode: — Address bus for the external data memory
DR	Data Register	**Master mode:** — Register for interface between mode DP and internal data bus (main bus) (32 bits)
		Slave mode: — Register for interface between mode DP (8-bit parallel data bus for the external data memory) and main bus (32 bits)
DRS	Data Register for Slave	**Slave mode:** — Register for interface between mode DP (16-bit parallel data bus for host CPU) and main bus (32 bits)
AR	Address Register	Register specifies external data memory address (13 bits)
HOST R/W CNT	Host CPU Read/Write Control Circuit	Slave Host CPU interface control mode circuit
R/W CNT	Read/Write Control Circuit	External memory read/write control circuit
Serial Input/Output Interfaces		
SO	Serial Output Data Register	Serial output data storage register (32 bits)
OSFT	Output Shift Register	Shift register - outputs SO data serially
SOCNT	Serial Output Control Circuit	Serial output control circuit
SI	Serial Input Data Register	Serial input data storage register (32 bits)
ISFT	Input Shift Register	Shift register - inputs serial data
SICNT	Serial Input Control Circuit	Serial input control circuit
Control Circuits		
CLK GEN	Clock Generator	Circuit for generating internal system clock and serial I/O clock
INT CNT	Interrupt Controller	Internal interrupt control circuit
TR	Temporary Register	General-purpose register (24 bits)
LC	Loop Counter	Register which sets program loop count (10 bits)
SR	Status Register	Register which specifies or indicates operation mode (20 bits)

ELECTRICAL SPECIFICATIONS

For the electrical specifiactions of the μPD77P220 in PROM program/read mode, see the later section titled PROM Electrical Specifications.

Capacitance

T_A = +25°C; V_{DD} = 0 V

Parameter	Symbol	Max	Unit	Conditions
Input capacitance	C_{IN}	10	pF	f_c = 1 MHz
Output capacitance	C_{OUT}	20	pF	

Absolute Maximum Ratings

T_A = +25°C

Operating temperature, T_{OPT}	−10 to +70°C
Storage temperature, T_{STG}	−65 to +150°C
Output voltage, V_O	−0.5 to V_{DD} + 0.5 V
Input voltage, V_I (except $\overline{SIEN}$/PROG)	−0.5 to V_{DD} + 0.5 V
V_I ($\overline{SIEN}$/PROG)	−0.5 to +12.5 V
Power supply voltage, V_{DD}	−0.5 to +6.5 V
V_{PP}	−0.5 to +13.5 V

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Power supply voltage	V_{DD}	4.75	5.0	5.25	V	Normal operation
		5.75	6.0	6.25	V	PROM mode
	V_{PP}	4.75	5.0	5.25	V	Normal operation
		12.2	12.5	12.8	V	PROM mode
Low-level input voltage	V_{IL}	−0.3		0.8	V	
High-level input voltage	V_{IH}	2.2		V_{DD} + 0.3	V	
Low-level X1 input voltage	V_{ILX}	−0.3		0.5	V	
High-level X1 input voltage	V_{IHX}	3.9		V_{DD} + 0.3	V	
Input voltage for PROM mode	V_{PROG}	11.5	12.0	12.5	V	
Operating temperature	T_{OPT}	−10	+25	+70	°C	Normal operation
		+20	+25	+30	°C	PROM mode

DC Characteristics

T_A = −10 to +70°C; V_{DD} = 5 V ±5%

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Low-level output voltage	V_{OL}			0.45	V	I_{OL} = 2.0 mA
High-level output voltage	V_{OH}	0.7 V_{DD}			V	I_{OH} = −400 μA
Low-level input current	I_{IL}			−400	μA	$\overline{RESET}$, SICK, SOCK, V_{IN} = 0 V
High-level input current	I_{IH}			400	μA	$\overline{M}$/S V_{IN} = V_{DD}
Low-level input leak current	I_{LIL}			−10	μA	Except $\overline{RESET}$, SICK, SOCK, V_{IN} = 0 V
High-level input leak current	I_{LIH}			10	μA	Except $\overline{M}$/S, V_{IN} = V_{DD}
Low-level output leak current	I_{LOL}			−10	μA	V_{OUT} = 0 V
High-level output leak current	I_{LOH}			10	μA	V_{OUT} = V_{DD}
X1 input current	I_{IX1}			400	μA	X1 pin, external clock input
Input leak current	I_{PROG}			30	μA	V_{PROG} = 12.0
Power supply current	I_{DD}		140	200	mA	f_{CYX} = 16.384 MHz (Normal operation)
				100	mA	PROM programming mode
	I_{PP}			1	mA	Normal operation
				30	mA	PROM programming mode

Crystal Oscillator Connection Conditions

T_A = −10 to +70°C; V_{DD} = 5 V ±5%

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Oscillation frequency	f_{CYX}					Figure 1
8-MHz version		1.0	16.384	16.667	MHz	
10-MHz version		1.0	—	20.000	MHz	
C1, C2 capacitance			15		pF	

Timing Requirements (Figure 4)

T_A = −10 to +70°C; V_{DD} = 5 V ±5%

		8-MHz Version			10-MHz Version				
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit	Conditions
X1 cycle time	t_{CYX}	60	61	1000	50		1000	ns	Figures 2 and 3. Voltage threshold for timing measurements are 1.0 and 3.0 volts.
X1 high pulse width	t_{XXH}	25			20			ns	
X1 low pulse width	t_{XXL}	25			20			ns	
X1 rise time	t_{XR}			5			5	ns	
X1 fall time	t_{XF}			5			5	ns	
SICK, SOCK cycle time	t_{CYS}	240	244		240	244		ns	
SICK, SOCK high pulse width	t_{SSH}	100			100			ns	
SICK, SOCK low pulse width	t_{SSL}	100			100			ns	
SICK, SOCK rise time	t_{SR}			20			20	ns	
SICK, SOCK fall time	t_{SF}			20			20	ns	

Switching Characteristics (Figure 4)

T_A = −10 to +70°C; V_{DD} = 5 V ±5%; C_L = 100 pF

Parameter	Symbol	Min	Max	Unit
X1 ↑ to $\overline{RD}$ delay time	t_{DXC}		50	ns
X1 ↑ to CLKOUT hold time	t_{HXC}	0		ns
SCK cycle time	t_{CYS}	$8t_{CYX}$		ns
SCK high pulse width	t_{SSH}	$4t_{CYX} - 65$		ns
SCK low pulse width	t_{SSL}	$4t_{CYX} - 65$		ns
SCK rise time	t_{SR}		20	ns
SCK fall time	t_{SF}		20	ns
X1 ↑ to SCK ↑ delay time	t_{DXS}	10	120	ns

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External Memory Access Timing (Figures 5, 6)

T_A = −10 to +70°C; V_{DD} = 5 V ±5%

Parameter	Symbol	8-MHz Version		10-MHz Version		Unit	Conditions
		Min	Max	Min	Max		
Data set time (for address)	t_{SADI}		$2t_{CYX}$ − 85		$2t_{CYX}$ − 75	ns	When an instruction is read
Data set time (for $\overline{RD}$ ↓)	t_{SRDI}		t_{CYX} − 25		t_{CYX} − 25	ns	
Data hold time (for $\overline{RD}$ ↑)	t_{HRDI}	0		0		ns	
Data set time (for address)	t_{SAD1}		$4t_{CYX}$ − 135		$4t_{CYX}$ − 115	ns	Applies to high-speed access area
	t_{SAD2}		$8t_{CYX}$ − 135		$8t_{CYX}$ − 115	ns	Applies to low-speed access area
Data set time (for $\overline{RD}$ ↓)	t_{SRD1}		$3t_{CYX}$ − 75		$3t_{CYX}$ − 65	ns	Applies to high-speed access area
	t_{SRD2}		$7t_{CYX}$ − 75		$7t_{CYX}$ − 65	ns	Applies to low-speed access area
Data hold time (for $\overline{RD}$ ↑)	t_{HRD}	0		0		ns	

Switching Characteristics (Figures 5 - 8)

T_A = −10 to +70°C; V_{DD} = 5 V ±5%; C_L = 100 pF

Parameter	Symbol	Min	Max	Unit	Conditions
X1 ↑ to $\overline{RD}$ delay time	t_{DXRD}		55	ns	
X1 ↑ to $\overline{WR}$ delay time	t_{DXWR}		55	ns	
Address set time (for $\overline{RD}$ ↓)	t_{SAR}	t_{CYX} − 50		ns	
Address hold time (for $\overline{RD}$ ↑)	t_{HRA}	5		ns	
$\overline{RD}$ low-level width	t_{WR1}	t_{CYX} − 20		ns	When an instruction is read
	t_{WR2}	$3t_{CYX}$ − 30		ns	Applies to high-speed access area
	t_{WR3}	$7t_{CYX}$ − 30		ns	Applies to low-speed access area
Address set time (For $\overline{WR}$ ↓)	t_{SAW}	t_{CYX} − 45		ns	
Address hold time (for $\overline{WR}$ ↑)	t_{HWA}	5		ns	
$\overline{WR}$ low-level width	t_{WW1}	$3t_{CYX}$ − 50		ns	Applies to high-speed access area
	t_{WW2}	$7t_{CYX}$ − 50		ns	Applies to low-speed access area
Data set time (for $\overline{WR}$ ↑)	t_{SDW1}	$3t_{CYX}$ − 100		ns	Applies to high-speed access area
	t_{SDW2}	$7t_{CYX}$ − 100		ns	Applies to low-speed access area
$\overline{WR}$ ↓ to data delay time	t_{DWD}	0		ns	
Data float time (for $\overline{WR}$ ↑)	t_{FWD}	10	50	ns	
$\overline{RD}$, $\overline{WR}$ recovery time	t_{RV}	t_{CYX} − 30		ns	At time of continuous operation

Host Interface Timing, Slave Mode (Figures 9, 10)

T_A = −10 to +70°C; V_{DD} = 5 V ±5%

Parameter	Symbol	Min	Unit
$\overline{CS}$ set time (for $\overline{HRD}$ ↓)	t_{SCR}	0	ns
$\overline{CS}$ hold time (for $\overline{HRD}$ ↑)	t_{HRC}	0	ns
$\overline{HRD}$ low-level width	t_{WHRD}	150	ns
$\overline{CS}$ set time (for $\overline{HWR}$ ↓)	t_{SCW}	0	ns
$\overline{CS}$ hold time (for $\overline{HWR}$ ↑)	t_{HWC}	0	ns
$\overline{HWR}$ low-level width	t_{WHWR}	150	ns
Data set time (for $\overline{HWR}$ ↓)	t_{SIHW}	100	ns
Data hold time (for $\overline{HHR}$ ↑)	t_{HHWI}	0	ns
$\overline{HRD}$, $\overline{HWR}$ recovery time	t_{HRV}	100	ns
$\overline{HRD}$, $\overline{HWR}$ hold time (for RQM ↑)	t_{HRH}	t_{CYX}	ns
P0, P1 set time (for X1 ↑)	t_{SPX}	t_{CYX}	ns
P0, P1 hold time (for X1 ↑)	t_{HXP}	t_{CYX}	ns

Switching Characteristics (Figures 9, 11)

T_A = −10 to +70°C; V_{DD} = 5 V ±5%; C_L = 100 pF

Parameter	Symbol	Min	Max	Unit
$\overline{HRD}$ ↓ to data delay time	t_{DHRI}		100	ns
$\overline{HRD}$ ↓ to data float time	t_{FHRI}	10	65	ns
X1 ↑ to RQM ↑ delay time	t_{DXRH}		100	ns
X1 ↑ to RQM ↓ delay time	t_{DXRL}		100	ns
$\overline{HRD}$, $\overline{HWR}$ ↑ to RQM ↓ delay time	t_{DHR}		$2t_{CYX}$ + 100	ns
X1 ↑ to P2, P3 delay time	t_{DXP}		100	ns

Interrupt Reset Timing (Figure 12)

T_A = −10 to +70°C; V_{DD} = 5 V ±5%

Parameter	Symbol	Min	Unit
$\overline{RESET}$ low-level width	t_{RST}	$6t_{CYX}$	ns
$\overline{NMI}$, $\overline{INT}$ hold time (for $\overline{RESET}$ ↑)	t_{HRNI}	$6t_{CYX}$	ns
$\overline{NMI}$, $\overline{INT}$ low-level width	t_{INT}	$6t_{CYX}$	ns
$\overline{NMI}$, $\overline{INT}$ recovery time	t_{RINT}	$6t_{CYX}$	ns

Serial Interface Timing (Figure 13)

T_A = −10 to +70°C; V_{DD} = 5 V ±5%

Parameter	Symbol	Min	Unit
$\overline{SIEN}$, SI set time (for SCK ↓)	t_{SSIS}	55	ns
$\overline{SIEN}$, SI hold time (for SCK ↓)	t_{HSSI}	30	ns
$\overline{SOEN}$ set time (for SCK ↑)	t_{SSES}	50	ns
$\overline{SOEN}$ hold time (for SCK ↑)	t_{HSSE}	30	ns
$\overline{SIEN}$, $\overline{SOEN}$ recovery time	t_{SRV}	t_{CYS}	ns

Switching Characteristics (Figures 14 - 16)

T_A = −10 to +70°C; V_{DD} = 5 V ±5%; C_L = 100 pF

Parameter	Symbol	Min	Max	Unit
SCK ↓ to SORQ ↑ delay time	t_{DSSQ}	30	150	ns
$\overline{SOEN}$ ↓ to SO delay time	t_{DSESO}		60	ns
$\overline{SOEN}$ ↑ to SO float time	t_{FSESO}	10	100	ns
SCK ↑ to SO delay time	t_{DSHSO}		60	ns
SCK ↓ to SO hold time	t_{HSHSO}	0		ns
SCK ↓ to SO delay time	t_{DSLSO}		60	ns
Switching Characteristics				
SCK ↓ to SO float time (at time of SORQ ↓)	t_{FSSO}	10	100	ns

Figure 1. Oscillation Circuit Diagram

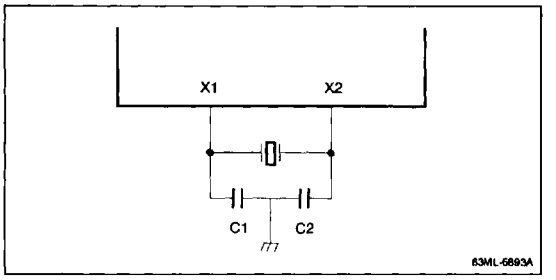


Figure 2. External Clock Connection Diagram

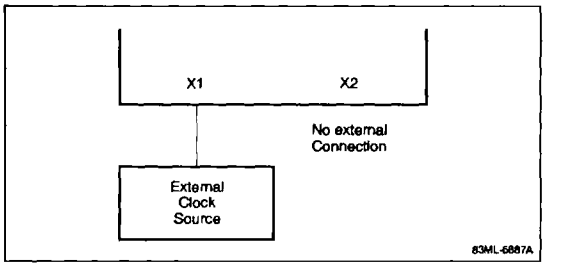


Figure 3. Switching Characteristics

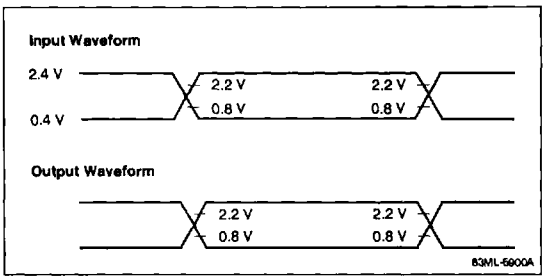


Figure 4. Clock Input/Output

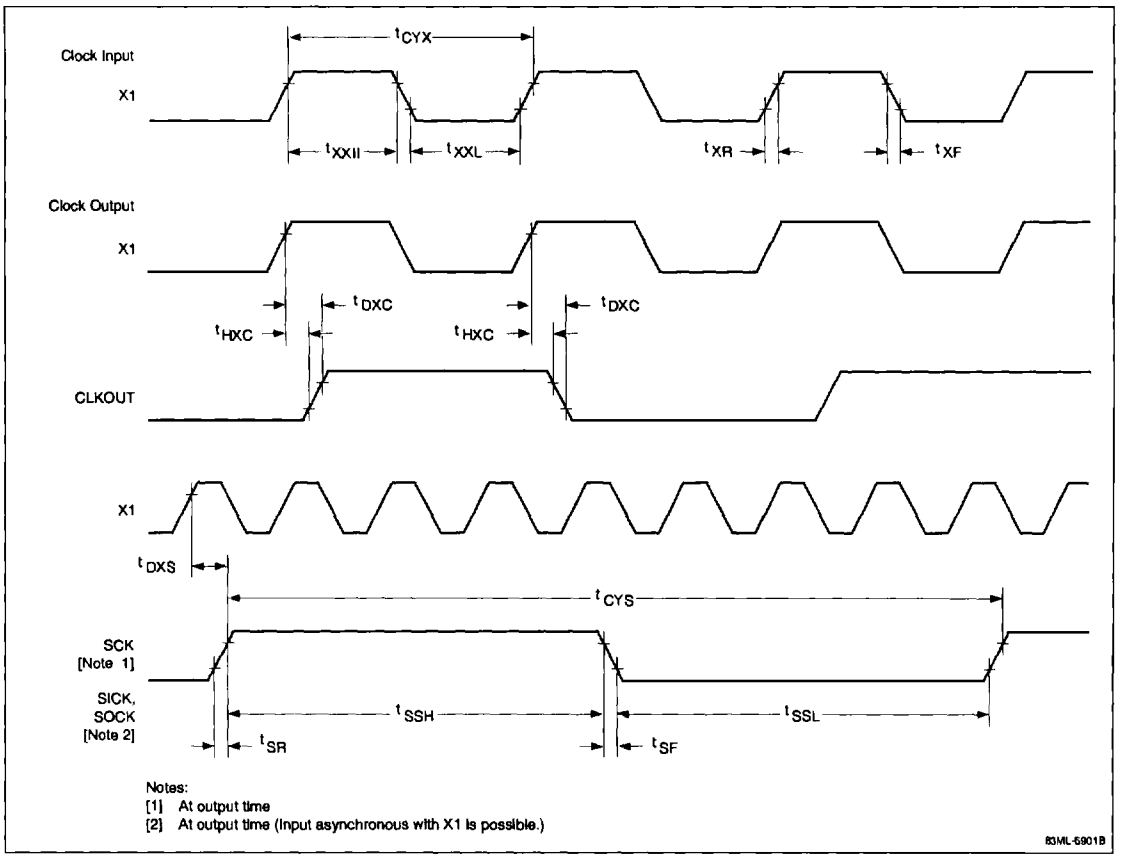


Figure 5. Instruction Read Operation (Master Mode Only)

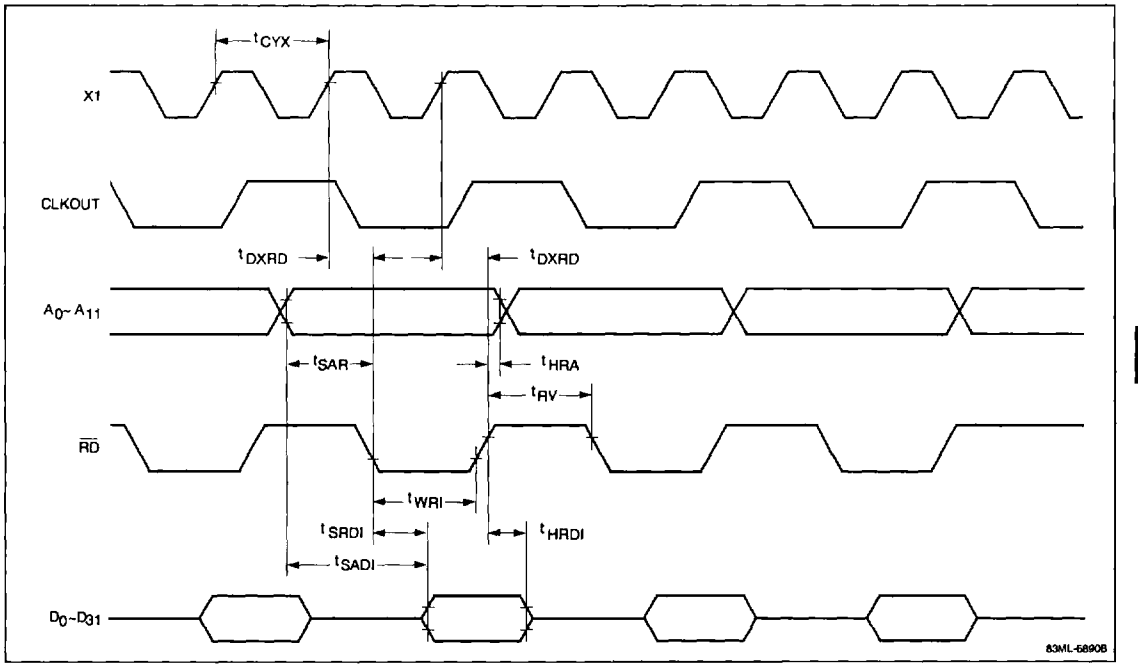


Figure 6. Data Read Operation

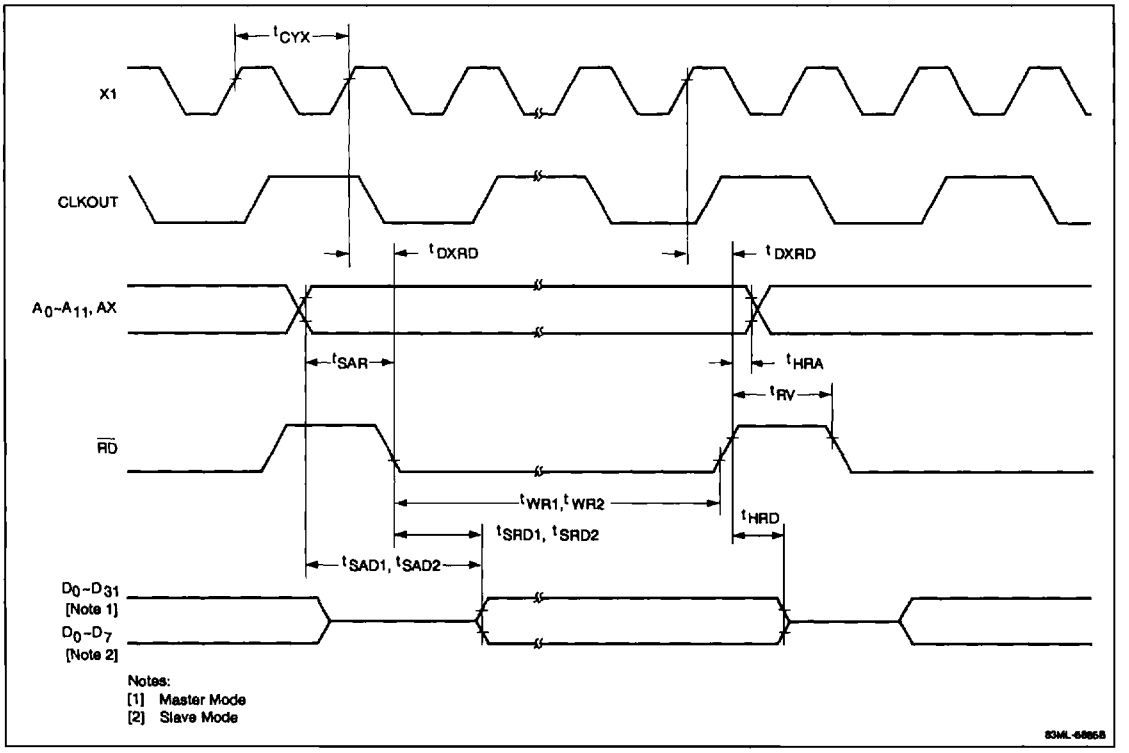


Figure 7. Data Write Operation

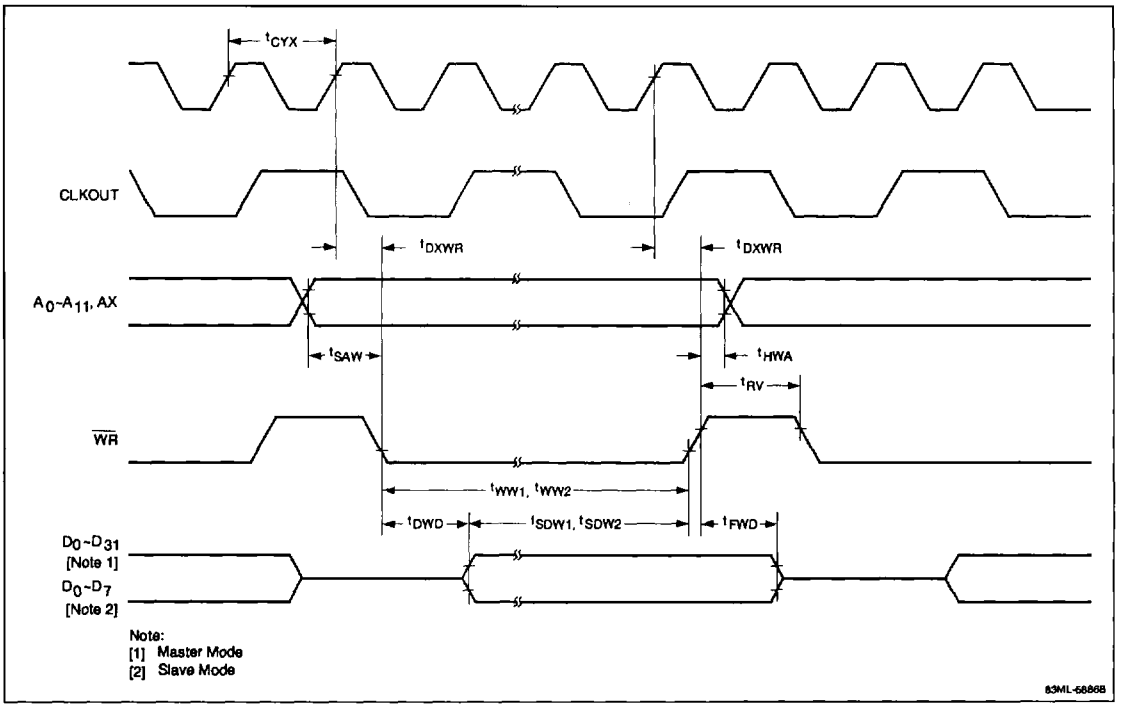
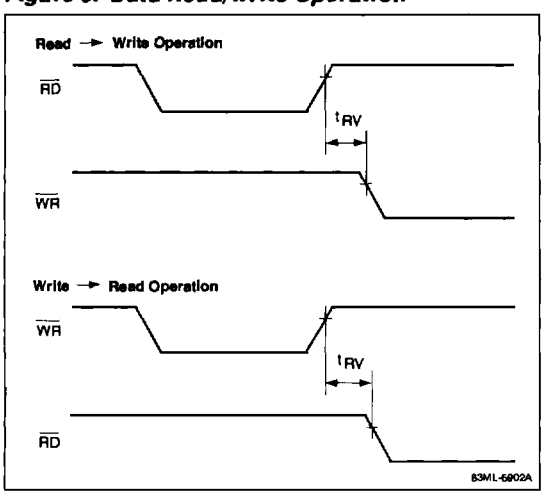


Figure 8. Data Read/Write Operation



3c

Figure 9. Host Read Operation

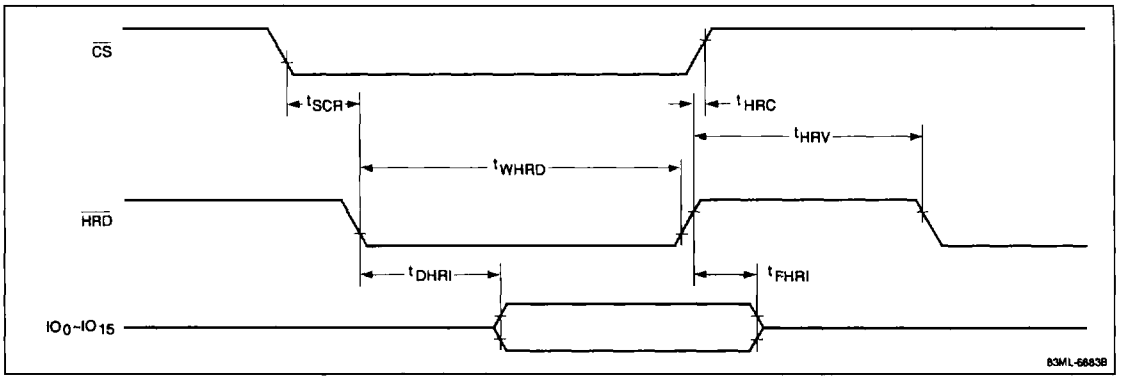


Figure 10. Host Write Operation

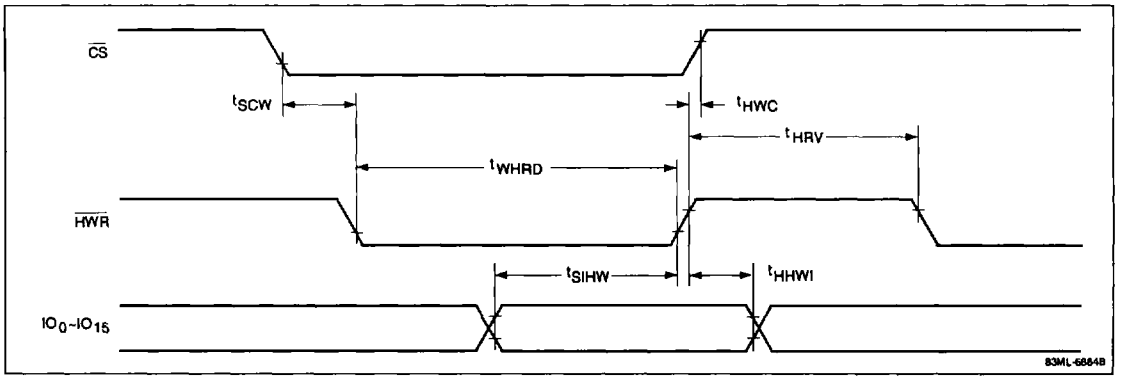


Figure 11. RQM Port

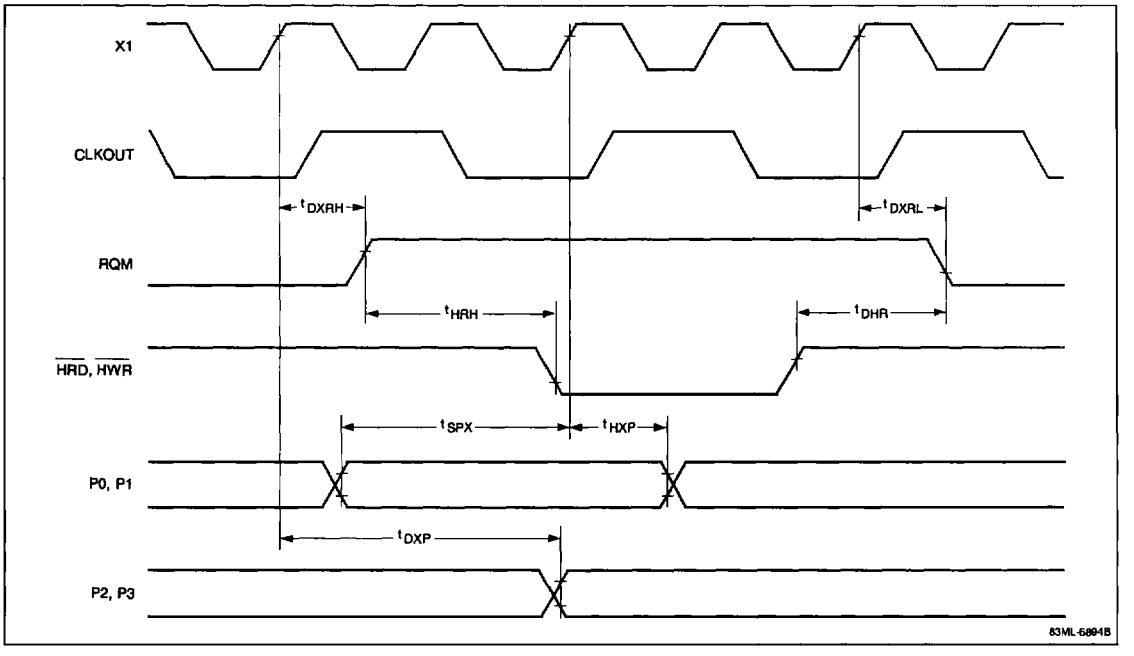
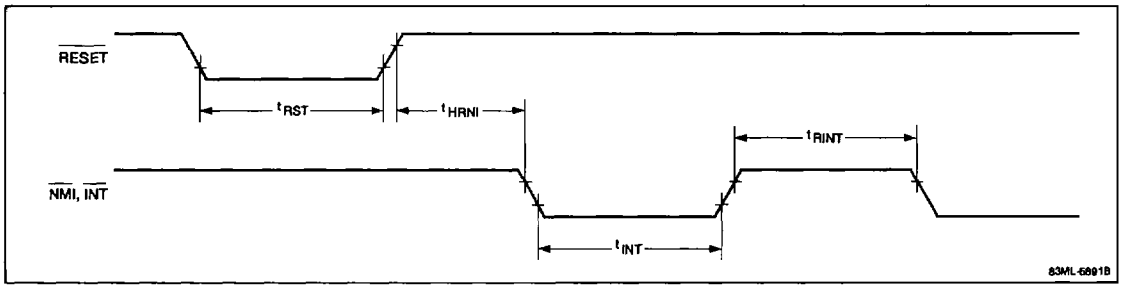


Figure 12. Interrupt Reset Timing Chart



3c

Figure 13. Serial In

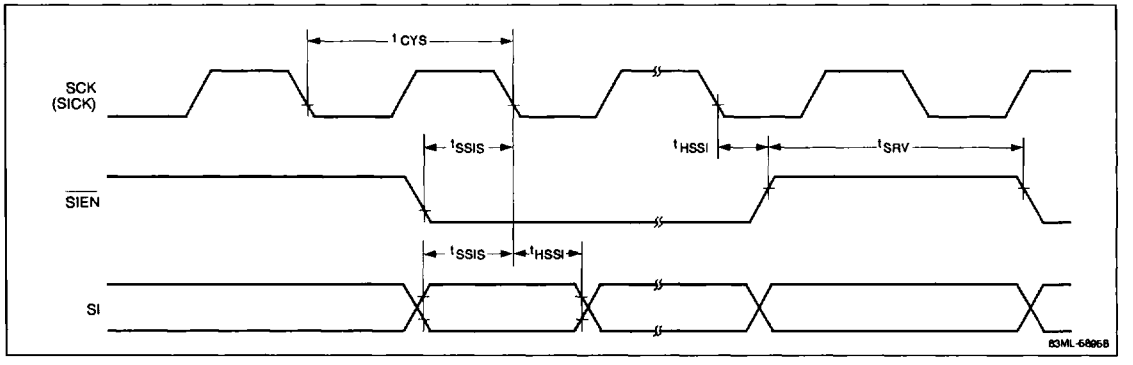


Figure 14. Serial OUT 1 (SOEN Interrupt Control)

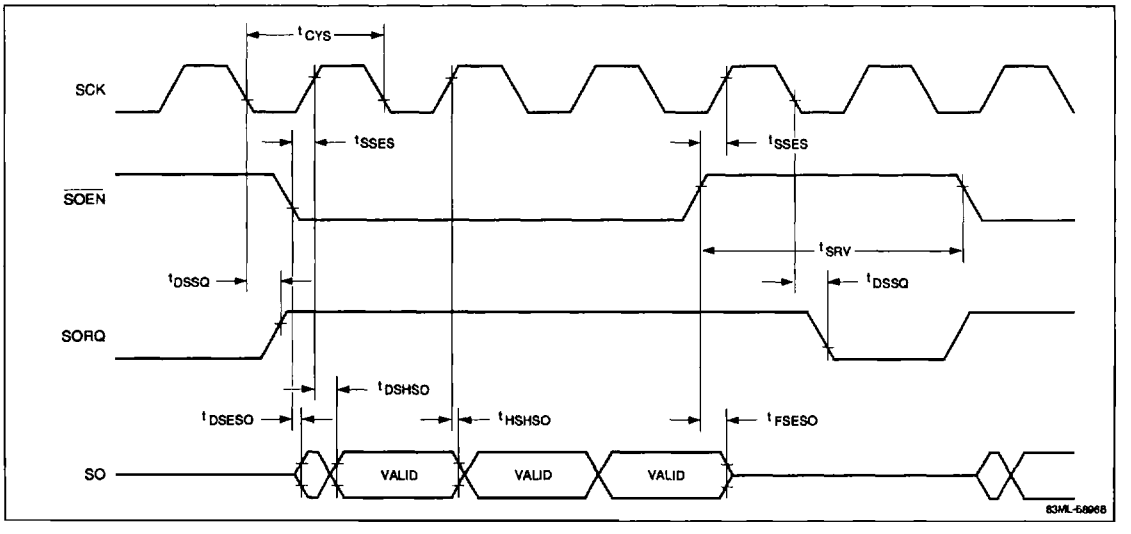


Figure 15. Serial OUT 2 (SOEN Control: SOEN Low AT SCK is Low Level

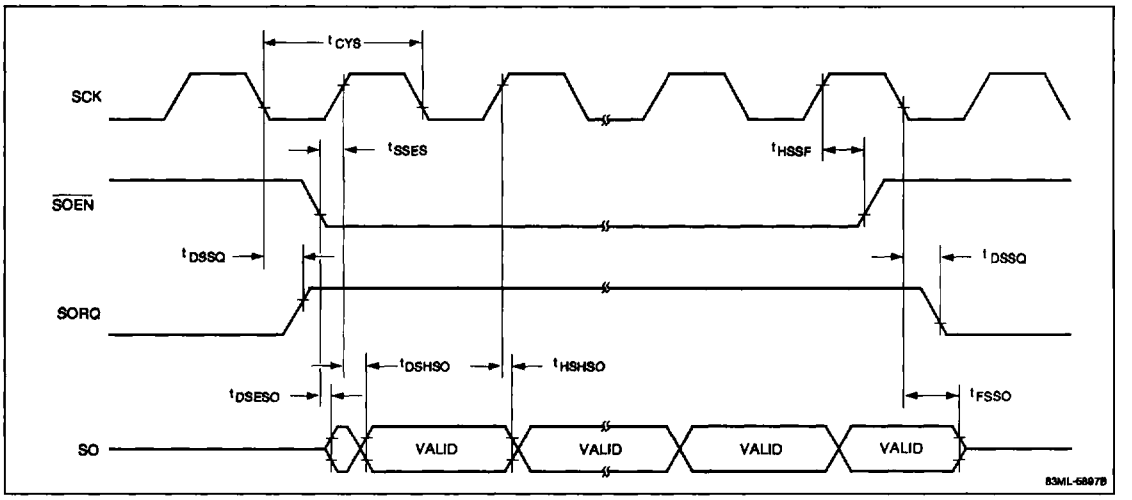
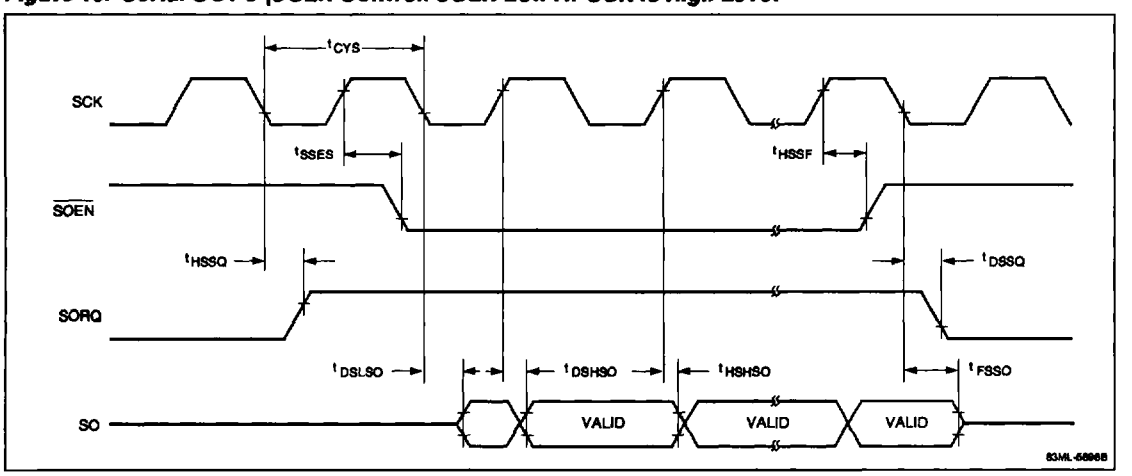


Figure 16. Serial OUT 3 (SOEN Control: SOEN Low AT SCK is High Level



3c

DATA FORMAT

The μPD77220 can process fixed-point data. Data is represented by a 2's complement, and the highest-order bit of fixed-point data indicates the sign. See figure 4. Table 3 shows the 24-bit fixed-point data format. Table 4 shows the 47-bit fixed point data.

Numeric data is processed in fixed-point data format, and the decimal point is positioned between the sign bit and the following bit.

Figure 17. Fixed-Point Data Format

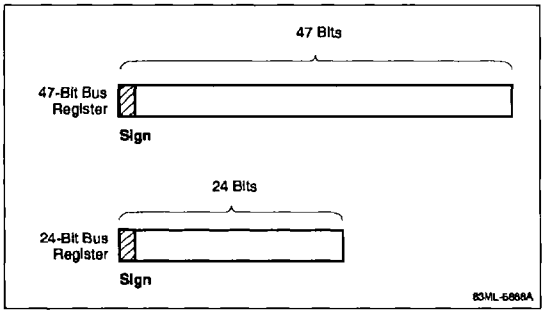


Table 3. 24-Bit Fixed-Point Internal Data Format

Value	Binary Notation	Hexadecimal Notation	Conversion to Decimal Number
Maximum Positive Value	0111 1111	$7FFFFF_H$	$1.0 - 2^{-23} \approx 1.0$
	0111 1110	$7FFFFF_H$	$1.0 - 2^{-22}$
	:	:	:
	0100 0000	400000_H	$1.0 - 2^{-1} = 0.5$
	:	:	:
Minimum Positive Value	0000 0001	000001_H	$2^{-23} \approx 1.2 \times 10^{-7}$
Zero	0000 0000	000000_H	0.0
Maximum Negative Value	1111 1111	$FFFFFF_H$	$-(2^{-23}) \approx -1.2 \times 10^{-7}$
	:	:	:
	1100 0000	$C00000_H$	$-(2^{-1}) = -0.5$
	:	:	:
	1000 0001	800001_H	$-1.0 + 2^{-23}$
Minimum Negative Value	1000 0000	800000_H	-1.0

Table 4. 47-Bit Fixed-Point Internal Data Format

Value	Binary Notation	Hexadecimal Notation	Conversion to Decimal Number
Maximum Positive Value	0111 1111	$7FFFFFFFFFFE_H$	$1.0 - 2^{-46} \approx 1.0$
	0111 1110	$7FFFFFFFFFFC_H$	$1.0 - 2^{-45}$
	:	:	:
	0100 0000	400000000000_H	$1.0 - 2^{-1} = 0.5$
	:	:	:
Minimum Positive Value	0000 0001	000000000002_H	$2^{-46} \approx 1.4 \times 10^{-14}$
Zero	0000 0000	000000000000_H	0.0
Maximum Negative Value	1111 1111	$FFFFFFFFFFFE_H$	$-(2^{-46}) \approx -1.4 \times 10^{-14}$
	:	:	:
	1100 0000	$C00000000000_H$	$-(2^{-1}) = -0.5$
	:	:	:
	1000 0001	800000000002_H	$-1.0 + 2^{-46}$
Minimum Negative Value	1000 0000	800000000000_H	-1.0

Conversion of data (47 bits) into hexadecimal format ranges from the highest-order bit (sign bit) to the lowest-order bit sequentially.

INSTRUCTIONS

All μPD77220 instructions consist of a 32-bit word. The instructions fall into three categories:

- Operation instructions
- Branch instructions
- Load instructions

Operation Instructions

An operation (OP) instruction is an ALU operation instruction where 22 different operations may be specified in the upper five bits. Figure 5 shows the bit format.

Pointer modifications may be specified in the CNT field. Transfers may also be specified within the SRC and DST fields of an OP instruction. When all fields are specified in an OP instruction, several different tasks are performed simultaneously.

OP Field. The 5-bit OP field specifies the operation type in the ALU. Table 5 lists the 22 types of operations it may contain.

CNT (Control) Field. The CNT field is 12 bits long and specifies a pointer, flag operation, register switch-over, data transfer format, and loop counter decrement.

The control field bit configuration is shown in figure 6. The field has 22 types of subfields. Table 6 describes the subfields.

Figure 18. Operation Instruction Format

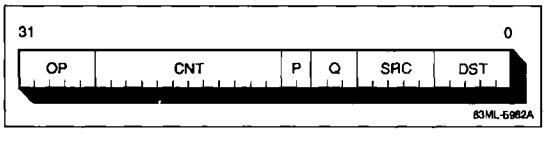


Table 5. OP Field Specifications

Symbol	OP Field (31-27)	Operation
NOP	00000	No operation
INC	00001	Increment
DEC	00010	Decrement
ABS	00011	Absolute
NOT	00100	Not
NEG	00101	Negate
SHLC	00110	Shift left with carry for double precision
SHRC	00111	Shift right with carry for double precision
ROL	01000	Rotate left

Table 5. OP Field Specifications

Symbol	OP Field (31-27)	Operation
ROR	01001	Rotate right
SHLM	01010	Shift left multiple (see note)
SHRM	01011	Shift right multiple (see note)
SHRAM	01100	Shift right arithmetic multiple see note)
CLR	01101	Clear
ADD	10000	Add fixed-point data
SUB	10001	Subtract fixed-point data
ADDC	10010	Add fixed-point data with carry
SUBC	10011	Subtract fixed-point data with carry
CMP	10100	Compare
AND	10101	AND
OR	10110	OR
XOR	10111	Exclusive OR

Multiple value is in SVR or specification value of SHV bit.

Table 6. Control Field Specifications

Group	Field	Function	Effective
Interrupt	EM	Enables/disables maskable interrupt	→
	BM	Sets and clears maskable interrupt input flag	→
PSW	FIS	PSW control	*/→
	FC	Switches over PSW0, PSW1	*
ROM pointer	RP	Rules ROM pointer count operations	→
	RPC	Specifies n value in ROM pointer operation	→
	RPS	Specifies low-order nine bits of data ROM address	→
RAM0/RAM1 pointers	M0	Specifies base pointer 0 and index register 0	→
	M1	Specifies base pointer 1 and index register 1	→
	DP0	Rules count operations of base pointer 0 and index register 0	→
	DP1	Rules count operations of base pointer 1 and index register 1	→
	BASE0	Specifies counter length of modulo counter base pointer 0	→
	BASE1	Specifies counter length of modulo counter counter base pointer 1	→
Data format conversion	WI	Specifies transfer format when working register is specified in the DST field	→
	WT	Specifies transfer format when working register is specified in the SRC field	→
Shift specification	SHV	Specifies amount of shift for 47-bit fixed-point data	*
Data memory access	RW	Specifies input/output operation for external memory	*
	EA	Address register increment and decrement	*/→
General-purpose output port	P2	Controls signal output of pins with the same name	→
	P3	Controls signal output of pins with the same name	→
Loop counter	L	Loop counter decrement	*
Jump	NAL	Specifies unconditional jump address	*

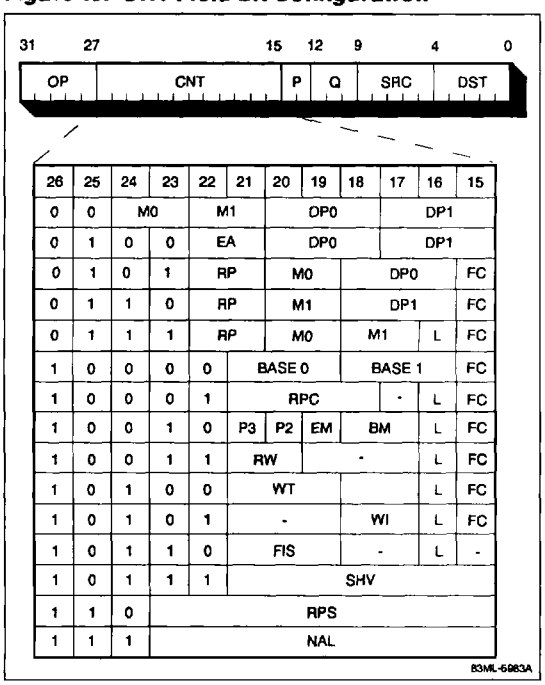
* Effective starting with current instruction.
→ Effective starting with the next instruction.

P Field. The 2-bit P field (bits 14, 13) specifies the source of input to the register, which is used as an input to the ALU for operations requiring two operands. The internal data bus, MPY output, RAM0, or RAM1 can be specified. Table 7 shows the field specifications.

Table 7. P Field Specifications

Symbol	Bit 14	Bit 13	Input of P Register
IB	0	0	PU bus
M4	0	1	Multiplier output register (MPY output)
RAM0	1	0	RAM block 0
RAM1	1	1	RAM block 1

Figure 19. CNT Field Bit Configuration



Q Field. The 3-bit Q field (bits 12-10) specifies the source of input to the Q register, which is the second of two ALU input registers.

One of the working registers, WR0 to WR7, must be specified in the Q field. The result of the operation is placed in the working register specified in the Q field. Table 8 provides the Q field specifications.

Table 8. Q Field Specifications

Symbol	Bit 12	Bit 11	Bit 10	Register
WR0	0	0	0	Working register 0
WR1	0	0	1	Working register 1
WR2	0	1	0	Working register 2
WR3	0	1	1	Working register 3
WR4	1	0	0	Working register 4
WR5	1	0	1	Working register 5
WR6	1	1	0	Working register 6
WR7	1	1	1	Working register 7

SRC (Source) Field. The 5-bit SRC field (bits 9-5) holds the source register for a transfer instruction. Table 9 lists the 32 types of registers that may be specified in this field.

Table 9. SRC Field Specifications

Symbol	SRC Field (9-5)	Selected Source Register
NON	00000	Non-selection
RP	00001	ROM pointer
PSW0	00010	Program status word 0
PSW1	00011	Program status word 1
SVR	00100	SVR (shift value register)
SR	00101	Status register
LC	00110	Loop counter
STK	00111	Stack
M	01000	M register
ML	01001	Low 24 bits of M register
ROM	01010	Data ROM
TR	01011	Temporary register
AR	01100	Address register
SI	01101	Serial input register
DR	01110	Data register
DRS	01111	Data register for slave
WR0	10000	Working register 0
WR1	10001	Working register 1
WR2	10010	Working register 2
WR3	10011	Working register 3
WR4	10100	Working register 4
WR5	10101	Working resister 5
WR6	10110	Working register 6
WR7	10111	Working register 7
RAM0	11000	RAM 0
RAM1	11001	RAM 1
BP0	11010	Base pointer 0
BP1	11011	Base pointer 1
IX0	11100	Index register 0
IX1	11101	Index register 1
K	11110	K register
L	11111	L register

DST (Destination) Field. The DST field (bits 4-0) is 5 bits long and specifies the destination register for a transfer instruction. Table 10 lists the 31 destinations that may be specified in the DST field.

Table 10. DST Field Specifications

Symbol	DST Field (4-0)	Selected Destination Register
NON	00000	Non-selection
RP	00001	ROM pointer
PSW0	00010	Program status word 0
PSW1	00011	Program status word 1
SVR	00100	SVR (shift value register)
SR	00101	Status register
LC	00110	Loop counter
STK	00111	Stack
LKR0	01000	L register (RAM 0 to K register)
KLR1	01001	K register (RAM 1 to L register)
TR	01011	Temporary register
AR	01100	Address register
SO	01101	Serial output register
DR	01110	Data register
DRS	01111	Data register for slave
WR0	10000	Working register 0
WR1	10001	Working register 1
WR2	10010	Working register 2
WR3	10011	Working register 3
WR4	10100	Working register 4
WR5	10101	Working resister 5
WR6	10110	Working register 6
WR7	10111	Working register 7
RAM0	11000	RAM 0
RAM1	11001	RAM 1
BP0	11010	Base pointer 0
BP1	11011	Base pointer 1
IX0	11100	Index register 0
IX1	11101	Index register 1
K	11110	K register
L	11111	L register

Branch Instructions

Branch instructions specify a conditional jump, an unconditional jump, subroutine call, or return. The format of the branch instruction, consisting of five fields, is shown in figure 7.

Note that the SRC and DST fields may be included as part of the branch instruction. This data transfer will take place regardless of any condition upon which a jump may be dependent.

B Field. This field (bits 31-28) indicates a branch instruction. The value of this field is always 1101.

C Field. This 5-bit field (bits 14-10) indicates the nature of the branch instruction. Table 11 summaries the branch conditions that can be specified.

NA Field. The destination address of the branch is contained in the 13-bit NA field (bits 27-15). Note that the most significant bit of the NA field is used to determine whether the destination address is in internal or external instruction memory.

SRC Field. The SRC field (bits 9-5) specifies a type of source register for a transfer instruction. There are 32 possible types.

DST Field. The DST field (bits 4-0) indicates the type of destination register to be used for a transfer instruction. There are 31 possible types.

Load Instructions

The load instruction consists of three fields as shown in figure 8. This instruction loads 24-bit data specified in the IM field into the register specified in the DST field. The data is input to each register through the main bus.

The value of the LDI field is always 111.

Figure 20. Branch Instruction Format

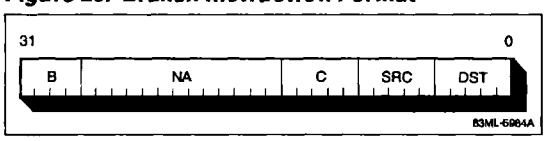


Figure 21. Load Instruction Format

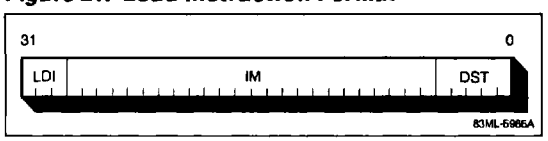


Table 11. Branch Condition Summary

Symbol	C Field (14-10)	Jump with Condition
JMP	00000	Jump with no condition
CALL	00001	Subroutine call
RET	00010	Return
JNZRP	00011	Jump if ROM pointer is not zero
JZ0	00100	Jump if zero flag 0 is set
JNZ0	00101	Jump if zero flag 0 is reset
JZ1	00110	Jump if zero flag 1 is set
JNZ1	00111	Jump if zero flag 1 is reset
JC0	01000	Jump if carry flag 0 is set
JNC0	01001	Jump if carry flag 0 is reset
JC1	01010	Jump if carry flag 1 is set
JNC1	01011	Jump if carry flag 1 is reset
JS0	01100	Jump if sign flag 0 is set
JNS0	01101	Jump if sign flag 0 is reset
JS1	01110	Jump if sign flag 1 is set
JNS1	01111	Jump if sign flag 1 is reset
JV0	10000	Jump if overflow flag 0 is set
JNV0	10001	Jump if overflow flag 0 is reset
JV1	10010	Jump if overflow flag 1 is set
JNV1	10011	Jump if overflow flag 1 is reset
JNFSI	10110	Jump if SI register is not full
JNESO	10111	Jump if SO register is not empty
JIP0*	11000	Jump if input port 0 is on
JIP1*	11001	Jump if input port 1 is on
JNZIX0	11010	Jump if index register 0 is nonzero
JNZIX1	11011	Jump if index register 1 is nonzero
JNZBP0	11100	Jump if base pointer 0 is nonzero
JNZBP1	11101	Jump if base pointer 1 is nonzero
JRDY	11110	Jump if ready is on
JRQM*	11111	Jump if request for master is on

* Valid for slave mode only.

3c

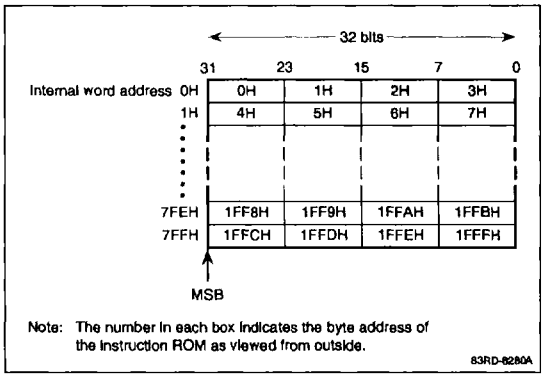
PROM INTERFACE

The μPD77P220 has a PROM—one-time programmable (OTP) or ultraviolet erasable (UVE)—consisting of a 2K-word x 32-bit instruction ROM and a 1K-word x 24-bit data ROM.

The 32-bit instruction words and 24-bit data words require special byte addresses because data is written to and read from the PROM in 8-bit bytes. Figure 22 shows the special byte addresses assigned to the data ROM (2000H to 2003H).

Each internal word address for the data ROM is equivalent to three byte addresses used by external devices plus one dummy byte address. For example, in figure 23, the internal word address OH corresponds to 3 byte addresses (2001H to 2003H) plus one dummy byte address (2000H)

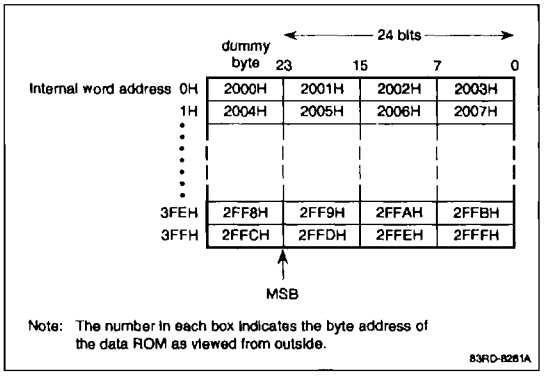
Figure 22. Instruction ROM Memory Map



Note: The number in each box indicates the byte address of the instruction ROM as viewed from outside.

83RD-8280A

Figure 23. Data ROM Memory Map



Note: The number in each box indicates the byte address of the data ROM as viewed from outside.

83RD-8281A

UVEPROM Erasure

Data in the UVEPROM can be erased by exposure to light with a wavelength shorter than 400 nm. Usually, ultraviolet light with a 254-nm wavelength is used. The erasure process, which sets all data bits to 1's, must take place before data is programmed to a UVEPROM.

The total light quantity required to completely erase the written data is 15Ws/cm^2, equivalent to exposure to a UV lamp with a rating of 12,000 μW/cm^2 for about 20 minutes. A longer time may be necessary due to factors such as the age of the UV lamp and stains on the package window. The window must be positioned within 1 inch of the UV lamp.

If the UVEPROM is exposed to direct sunlight or fluorescent light for a long time, the data might be destroyed. To prevent this, mask the window with a cover of film after the erasure process.

Data Programming Procedure

This section describes how to program the PROM. Table 12 shows the reassigned pin functions when in PROM program/read mode. Figure 24 shows the on-chip PROM program timing.

Since no PROM cell exists for the data ROM dummy byte addresses, set the dummy byte addresses to FFH, the default data for normal programming. The data programming procedure is as follows:

(1) Enter PROM program mode by applying +12.5 ±0.5 V to the $\overline{SIEN}$/PROG PIN, +6 V to the V_{DD} pin, and +12.5 ±0.3 V to the V_{PP} pin.
(2) Specify the desired ROM byte address from the address input pins A_0 - A_{13}.
(3) Program the data on the data bus (D_0 - D_7) by applying 0 to the $\overline{CE}$ pin and 1 to the $\overline{OE}$ pin. (Program mode.)
(4) Output programmed data to the data bus (D_0 - D_7) by applying 0 to the $\overline{OE}$ pin and 1 to the $\overline{CE}$ pin. (Program verify mode.)
(5) Repeat steps 2 through 4 to a maximum of 25 times until the data is properly written to the specified address.
(6) After verifying that the data has been properly programmed, apply an additional overprogram pulse by setting $\overline{OE}$ to 1 (clear $\overline{CE}$ to 0). The overprogram pulse width is determined by multiplying the initial pulse width by 3X ms, where X equals the number of times steps 3 and 4 were repeated.

The above procedure completes writing one byte of data. If steps 2 to 4 have been repeated more than 25 times and the data has not programmed properly, the μPD77P220 is defective.

Table 12. Pin Functions for PROM

Program Mode	Normal M/S Mode	Function
A_0 - A_8	A_0 - A_8	Input address pins (viewed from external device) for programming/ reading PROM (instruction ROM and data ROM).
A_9	$\overline{INT}$	
A_{10}	A_{10}	
A_{11}	A_{11}	
A_{12}	AX	
A_{13}	A_9	
D_0 - D_7	D_0 - D_7	Input/output data pins for PROM (instruction ROM and data ROM).
$\overline{CE}$	$D_{25}/\overline{HWR}$	PROM program strobe signal (active low)
$\overline{OE}$	$D_{24}/\overline{HRD}$	PROM read strobe signal (active low)
V_{PP}	V_{PP}	Power pin to read or program PROM; apply + 12.5 V for programming and + 5 V for reading.
V_{DD}	V_{DD}	Power pin; apply + 6 V for programming and + 5 V for reading.
GND	GND	Ground terminals
PROG	$\overline{SIEN}$	Sets PROM program or read mode; apply + 12.5 V to set PROM program/ read mode.

Data Reading Procedure

This section describes the data reading procedure. Figure 25 shows the on-chip PROM read timing. The programming procedure is as follows:

(1) Enter the PROM read mode by applying + 12.5 ± 0.5 V to $\overline{SIEN}$/PROG pin, + 5 V to the V_{DD} pin, and + 5 V to the V_{PP} pin.
(2) Specify the desired ROM byte address from the address input pins A_0 - A_{13}.
(3) Output data to the data bus (D_0 - D_7) by clearing $\overline{OE}$ and $\overline{CE}$ to 0.

3c

PROM ELECTRICAL SPECIFICATIONS

This section lists the electrical specifications of the μPD77P220 while in PROM program/read mode.

Data Program Timing Requirements

T_A = 25 ±5°C; V_{DD} = 6 ±0.25 V; V_{PP} = 12.5 ±0.3 V; V_{PROG} = 12.0 ±0.5 V

Parameter	Symbol	Min	Typ	Max	Unit
$\overline{CE}$ setup time for $\overline{SIEN}$/PROG	t_{SRSCE}	2			μs
$\overline{CE}$ setup time for address	t_{SAC}	2			μs
$\overline{CE}$ setup time for data	t_{SDC}	2			μs
$\overline{CE}$ setup time for V_{PP}	t_{SVPC}	2			μs
$\overline{CE}$ setup time for V_{DD}	t_{SVDC}	2			μs
$\overline{OE}$ setup time for data	t_{SDO}	2			μs
Address hold time	t_{HCA}	2			μs
Data hold time	t_{HCD}	2			μs
Initial program pulse width	t_{WCD}	0.95	1.0	1.05	ms
Overprogram pulse width	t_{WC1}*	2.85		78.75	ms

*t_{WC1} = $3nt_{WCO}$ assuming initial program pulse is applied n times.

Data Program Switching Characteristics

T_A = 25 ±5°C; V_{DD} = 6 ±0.25 V; V_{PP} = 12.5 ±0.3 V; V_{PROG} = 12.0 ±0.5 V

Parameter	Symbol	Min	Typ	Max	Unit
$\overline{OE}$ to output float time	t_{FOD}	0		130	ns
$\overline{OE}$ to output delay	t_{DODW}			250	ns

Data Program Read Timing Requirements

T_A = 25 ±5°C; V_{DD} = V_{PP} = 5 ±0.5 V; V_{PROG} = 12.0 ±0.5 V

Parameter	Symbol	Min	Typ	Max	Unit
$\overline{CE}$ setup time for $\overline{SIEN}$/PROG	t_{SRSCE}	2			μs
$\overline{OE}$ setup time for $\overline{SIEN}$/PROG	t_{SRSOE}	2			μs

Data Read Switching Characteristics

T_A = 25 ±5°C; V_{DD} = V_{PP} = 5 ±0.5 V; V_{PROG} = 12.0 ±0.5 V

Parameter	Symbol	Min	Typ	Max	Unit
Address to output delay	t_{DAD}			200	ns
$\overline{CE}$ to output delay	t_{DCD}			200	ns
$\overline{OE}$ to output delay	t_{DODR}			100	ns
$\overline{OE}$ to high to output float	t_{FCD}	0		65	ns
Address to output hold	t_{HAD}	0			ns

Figure 24. On-Chip PROM Program Timing

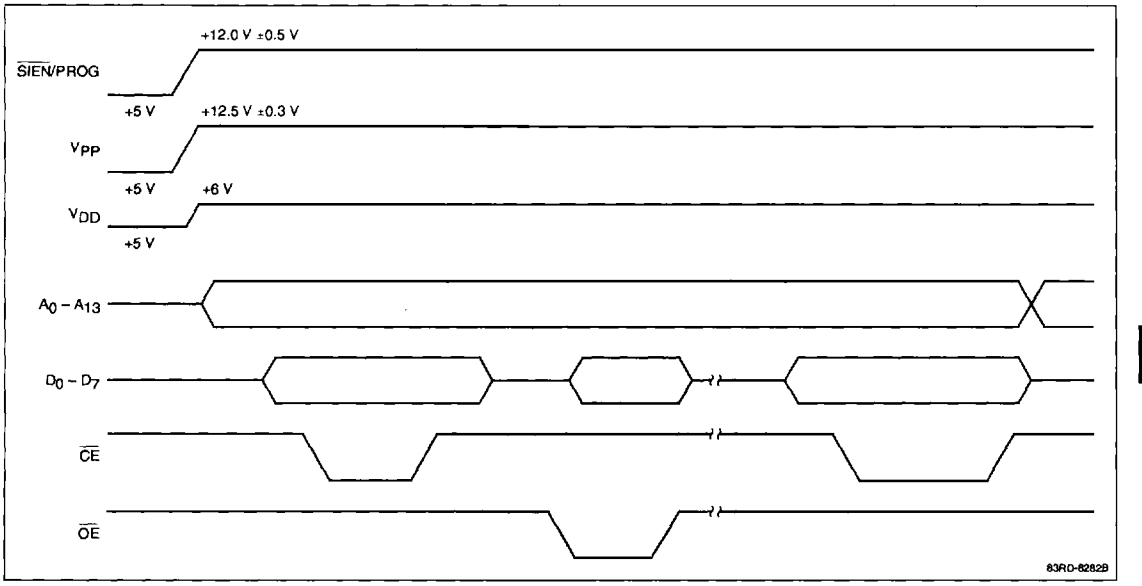


Figure 25. On-Chip PROM Read Timing