SIEMENS

4M × 4-Bit Dynamic RAM
2k & 4k Refresh
(Hyper Page Mode - EDO)

HYB 5116405BJ-50/-60
HYB 5117405BJ-50/-60
HYB 3116405BJ/BT(L)-50/-60
HYB 3117405BJ/BT-50/-60

Advanced Information

- 4 194 304 words by 4-bit organization
- 0 to 70 °C operating temperature
- Hyper Page Mode - EDO - operation
- Performance:

		-50	-60	
t_{RAC}	$\overline{\text{RAS}}$ access time	50	60	ns
t_{CAC}	$\overline{\text{CAS}}$ access time	13	15	ns
t_{AA}	Access time from address	25	30	ns
t_{RC}	Read/Write cycle time	84	104	ns
t_{HPC}	Hyper page mode (EDO) cycle time	20	25	ns

- Power dissipation, refresh & addressing:

	HYB 5116405		**HYB 3116405**		**HYB 5117405**		**HYB 3117405**		
	-50	-60	-50	-60	-50	-60	-50	-60	
Power supply	5 V ± 10%		3.3 V ± 0.3 V		5 V ± 10%		3.3 V ± 0.3 V		
Addressing	12/10		12/10		11/11		11/11		
Refresh	4096 cycles / 64 ms				2048 cycles / 32 ms				
L-version	4096 cycles / 128 ms				–				
Active	275	220	180	144	440	385	288	252	mW
TTL Standby	11		7.2		11		7.2		mW
CMOS Standby	5.5		3.6		5.5		3.6		mW
CMOS Standby (L-version)	–		0.72		–		–		mW

- Read, write, read-modify-write, $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$-only refresh, hidden refresh, test mode and Self Refresh (on L-versions only)
- All inputs, outputs and clocks fully TTL (5 V versions) and LV-TTL (3.3 V version)-compatible
- Plastic Package: P-SOJ-26/24-1 300 mil
  P-TSOPII-26/24-1 300 mil

HYB 5116(7)405BJ-50/-60
HYB 3116(7)405BJ/BT(L)-50/-60
4M × 4 EDO-DRAM

The HYB 5(3)116(7)405 are 16 MBit dynamic RAMs based on die revisions “G” & “F” and organized as 4 194 304 words by 4-bits. The HYB 5(3)116(7)405BJ/BT(L) utilizes a submicron CMOS silicon gate process technology, as well as advanced circuit techniques to provide wide operating margins, both internally and for the system user. Multiplexed address inputs permit the HYB 5(3)116(7)405 to be packaged in a standard SOJ-26/24 and TSOPII-26/24 plastic package with 300 mil width. These packages provide high system bit densities and are compatible with commonly used automatic testing and insertion equipment. The HYB 3116(7)405BTL have a very low power “sleep mode” supported by Self Refresh.

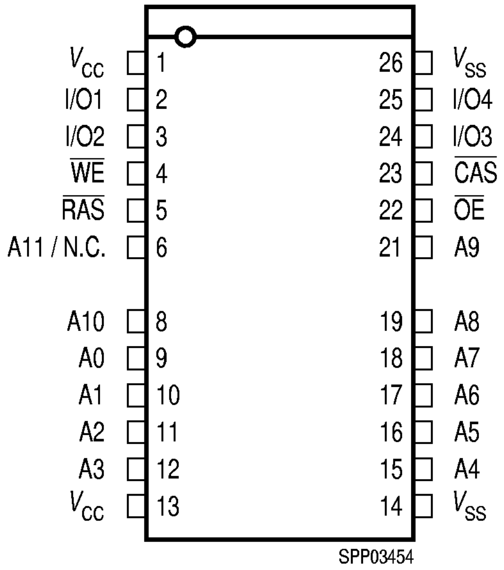
Ordering Information

Type	Ordering Code	Package	Descriptions
2k-Refresh Versions:			
HYB 5117405BJ-50	Q67100-Q1101	P-SOJ-26/24-1 300 mil	5 V 50 ns EDO-DRAM
HYB 5117405BJ-60	Q67100-Q1102	P-SOJ-26/24-1 300 mil	5 V 60 ns EDO-DRAM
HYB 3117405BJ-50	on request	P-SOJ-26/24-1 300 mil	3.3 V 50 ns EDO-DRAM
HYB 3117405BJ-60	on request	P-SOJ-26/24-1 300 mil	3.3 V 60 ns EDO-DRAM
HYB 3117405BT-50	on request	P-TSOPII-26/24-1 300 mil	3.3 V 50 ns EDO-DRAM
HYB 3117405BT-60	on request	P-TSOPII-26/24-1 300 mil	3.3 V 60 ns EDO-DRAM
4k-Refresh Versions:			
HYB 5116405BJ-50	Q67100-Q1098	P-SOJ-26/24-1 300 mil	5 V 50 ns EDO-DRAM
HYB 5116405BJ-60	Q67100-Q1099	P-SOJ-26/24-1 300 mil	5 V 60 ns EDO-DRAM
HYB 3116405BJ-50	on request	P-SOJ-26/24-1 300 mil	3.3 V 50 ns EDO-DRAM
HYB 3116405BJ-60	on request	P-SOJ-26/24-1 300 mil	3.3 V 60 ns EDO-DRAM
HYB 3116405BT-50	on request	P-TSOPII-26/24-1 300 mil	3.3 V 50 ns EDO-DRAM
HYB 3116405BT-60	on request	P-TSOPII-26/24-1 300 mil	3.3 V 60 ns EDO-DRAM
HYB 3116405BTL-50	on request	P-TSOPII-26/24-1 300 mil	3.3 V 50 ns LP-EDO-DRAM
HYB 3116405BTL-60	on request	P-TSOPII-26/24-1 300 mil	3.3 V 60 ns LP-EDO-DRAM

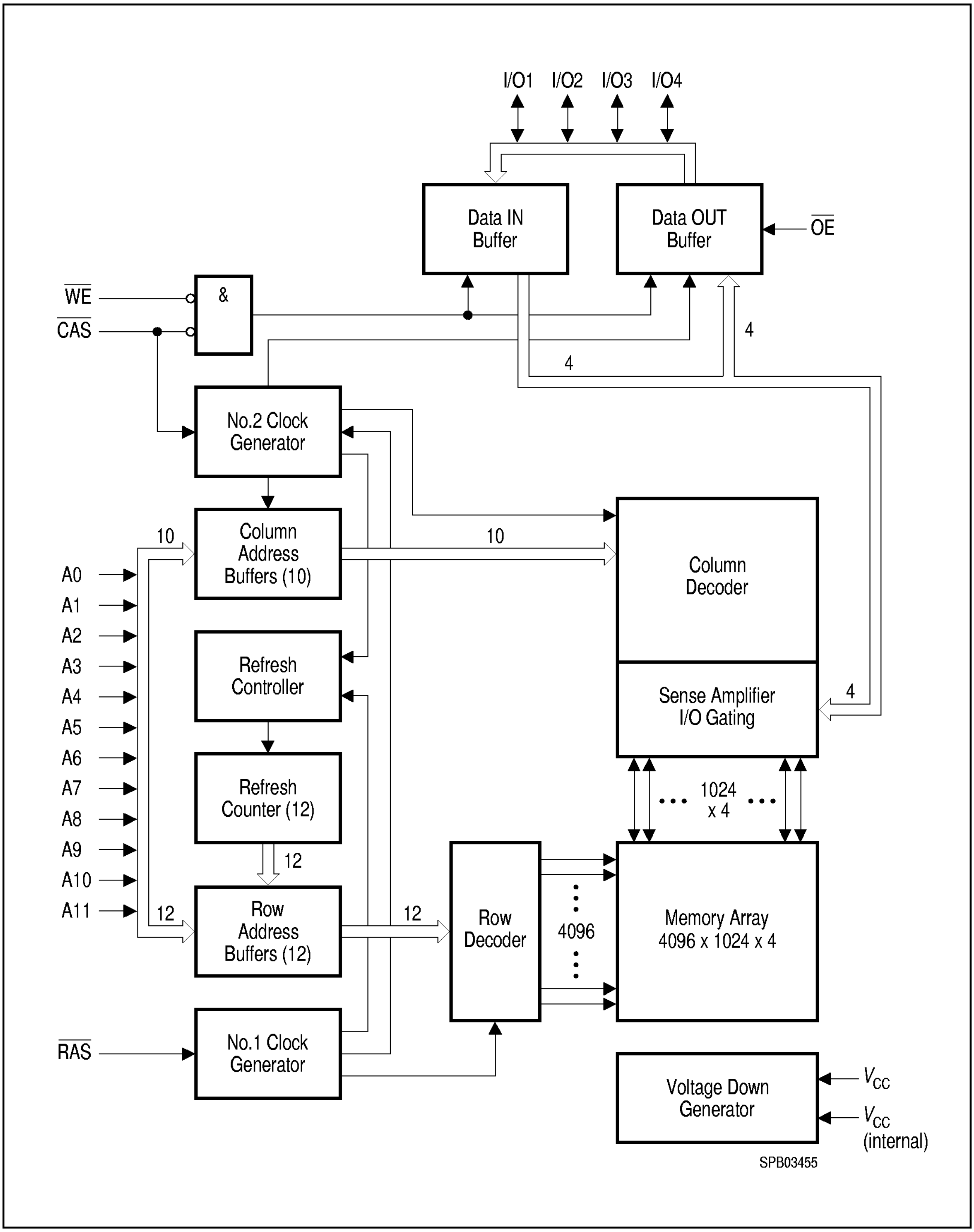
Pin Names

	HYB 5(3)16405 4k-Refresh	HYB 5(3)17405 2k-Refresh
Row Address Inputs	A0 - A11	A0 - A10
Column Address Inputs	A0 - A9	A0 - A10
Row Address Strobe	$\overline{\text{RAS}}$	
Column Address Strobe	$\overline{\text{CAS}}$	
Output Enable	$\overline{\text{OE}}$	
Data Input/Output	I/O1 - I/O4	
Read/Write Input	$\overline{\text{WE}}$	
Power Supply	V_{CC}	
Ground (0 V)	V_{SS}	
Not Connected	–	N.C.

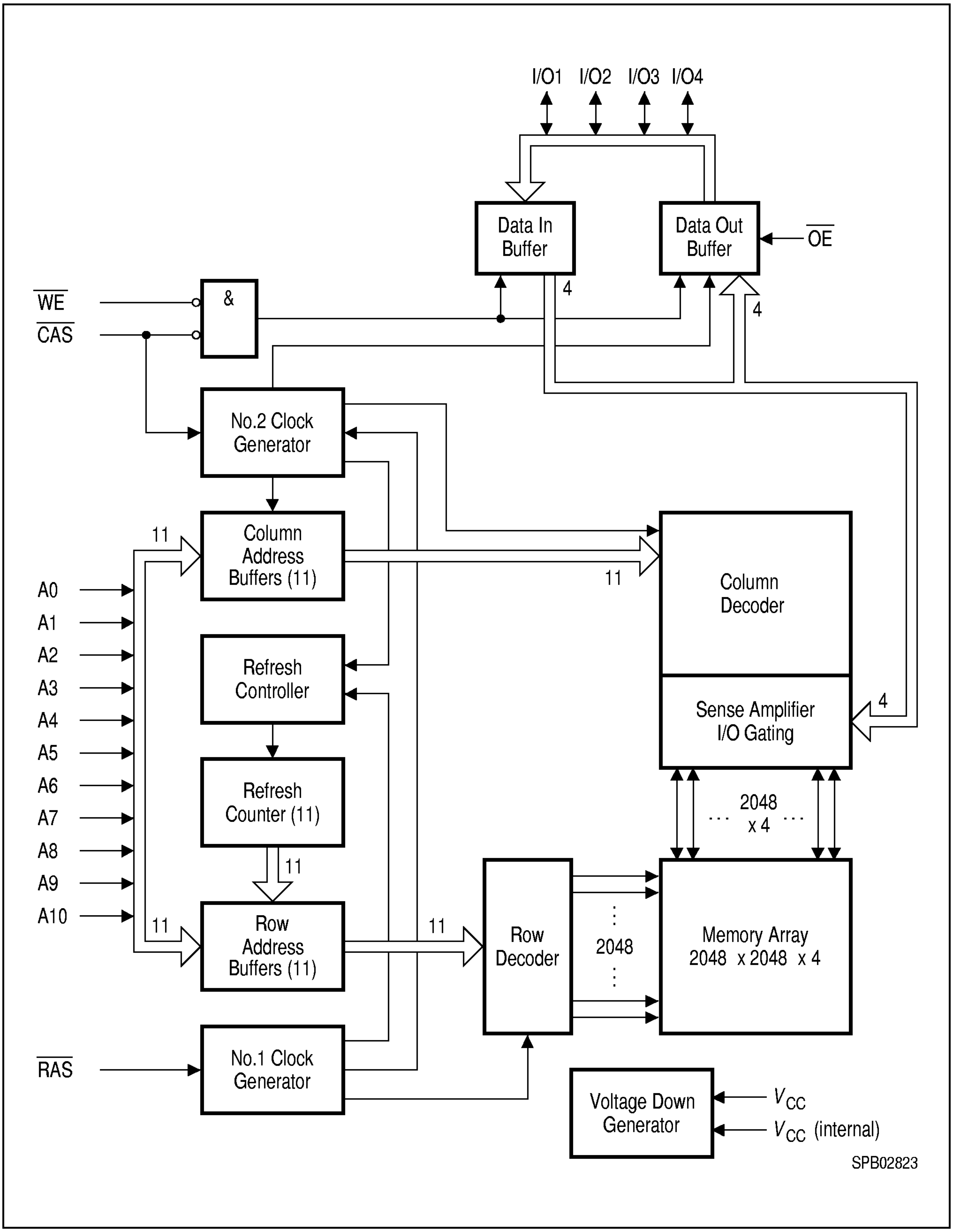
P-SOJ-26/24-1 300 mil
P-TSOPII-26/24-1 300 mil



Pin Configuration
(top view)



Block Diagram for HYB 5(3)116405 (4k-refresh)



Block Diagram for HYB 5(3)117405 (2k-refresh)

Absolute Maximum Ratings

Operating temperature range	0 to 70 ˚C
Storage temperature range	– 55 to 150 ˚C
Input/output voltage (5 V versions)	– 0.5 to min (V_{CC} + 0.5, 7.0) V
Input/output voltage (3.3 V versions)	– 0.5 to min (V_{CC} + 0.5, 4.6) V
Power supply voltage (5 V versions)	– 1.0 V to 7.0 V
Power supply voltage (3.3 V versions)	– 1.0 V to 4.6 V
Power dissipation (5 V versions)	1.0 W
Power dissipation (3.3 V versions)	0.5 W
Data out current (short circuit)	50 mA

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = 0 to 70 °C, V_{SS} = 0 V, t_T = 2 ns

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
5 V Versions					
Power supply voltage	V_{CC}	4.5	5.5	V	
Input high voltage	V_{IH}	2.4	V_{CC} + 0.5	V	1
Input low voltage	V_{IL}	– 0.5	0.8	V	1
Output high voltage (I_{OUT} = – 5 mA)	V_{OH}	2.4	–	V	1
Output low voltage (I_{OUT} = 4.2 mA)	V_{OL}	–	0.4	V	1
3.3 V Versions					
Power supply voltage	V_{CC}	3.0	3.6	V	
Input high voltage	V_{IH}	2.0	V_{CC} + 0.5	V	1
Input low voltage	V_{IL}	– 0.5	0.8	V	1
TTL Output high voltage (I_{OUT} = – 2 mA)	V_{OH}	2.4	–	V	1
TTL Output low voltage (I_{OUT} = 2 mA)	V_{OL}	–	0.4	V	1
CMOS Output high voltage (I_{OUT} = – 100 µA)	V_{OH}	V_{CC} – 0.2	–	V	
CMOS Output low voltage (I_{OUT} = 100 µA)	V_{OL}	–	0.2	V	

DC Characteristics (cont'd)
T_A = 0 to 70 °C, V_{SS} = 0 V, t_T = 2 ns

Parameter	Symbol	Limit Values			Unit	Notes
		min.	max.			
			2k	4k		
Common Parameters						
Input leakage current (0 V ≤ V_{IH} ≤ V_{CC} + 0.3 V, all other pins = 0 V)	$I_{I(L)}$	– 10	10		µA	1
Output leakage current (DO is disabled, 0 V ≤ V_{OUT} ≤ V_{CC} + 0.3 V)	$I_{O(L)}$	– 10	10		µA	1
Average V_{CC} supply current	I_{CC1}					
-50 version		–	80	50	mA	2, 3, 4
-60 version		–	70	40	mA	2, 3, 4
($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, address cycling: $t_{RC} = t_{RC\ MIN.}$)						
Standby V_{CC} supply current ($\overline{\text{RAS}}$ = $\overline{\text{CAS}}$ = V_{IH})	I_{CC2}	–	2		mA	–
Average V_{CC} supply current, during $\overline{\text{RAS}}$-only refresh cycles	I_{CC3}					
-50 version		–	80	50	mA	2, 4
-60 version		–	70	40	mA	2, 4
($\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}}$ = V_{IH}, $t_{RC} = t_{RC\ MIN.}$)						
Average V_{CC} supply current,during hyper page mode (EDO)	I_{CC4}					
-50 version		–	35		mA	2, 3, 4
-60 version		–	30		mA	2, 3, 4
($\overline{\text{RAS}}$ = V_{IL}, $\overline{\text{CAS}}$, address cycling: $t_{PC} = t_{PC\ MIN.}$)						
Standby V_{CC} supply current ($\overline{\text{RAS}}$ = $\overline{\text{CAS}}$ = V_{CC} – 0.2 V)	I_{CC5}	–	1 200		mA µA	1 L-version
Average V_{CC} supply current, during $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh mode	I_{CC6}					
-50 version		–	80	50	mA	2, 4
-60 version		–	70	40	mA	2, 4
($\overline{\text{RAS}}$, $\overline{\text{CAS}}$ cycling: $t_{RC} = t_{RC\ MIN.}$)						
Average Self Refresh current (CBR cycle with $t_{RAS} > t_{RASS\ MIN.}$, $\overline{\text{CAS}}$ held low, $\overline{\text{WE}}$ = V_{CC} – 0.2 V, Address and Din = V_{CC} – 0.2 V or 0.2 V)	I_{CC7}	–	250		µA	L-version only

Capacitance

T_A = 0 to 70 °C, f = 1 MHz

Parameter	Symbol	Limit Values		Unit
		min.	**max.**	
Input capacitance (A0 to A11)	C_{I1}	–	5	pF
Input capacitance ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$)	C_{I2}	–	7	pF
I/O capacitance (I/O1 to I/O4)	C_{IO}	–	7	pF

AC Characteristics [5, 6]

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 % / V_{CC} = 3.3 V ± 0.3 V, t_T = 2 ns

Parameter	Symbol	Limit Values				Unit	Note
		-50		**-60**			
		min.	**max.**	**min.**	**max.**		
Common Parameters							
Random read or write cycle time	t_{RC}	84	–	104	–	ns	
$\overline{\text{RAS}}$ precharge time	t_{RP}	30	–	40	–	ns	
$\overline{\text{RAS}}$ pulse width	t_{RAS}	50	10k	60	10k	ns	
$\overline{\text{CAS}}$ pulse width	t_{CAS}	8	10k	10	10k	ns	
Row address setup time	t_{ASR}	0	–	0	–	ns	
Row address hold time	t_{RAH}	8	–	10	–	ns	
Column address setup time	t_{ASC}	0	–	0	–	ns	
Column address hold time	t_{CAH}	8	–	10	–	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	t_{RCD}	12	37	14	45	ns	
$\overline{\text{RAS}}$ to column address delay	t_{RAD}	10	25	12	30	ns	
$\overline{\text{RAS}}$ hold time	t_{RSH}	13	–	15	–	ns	
$\overline{\text{CAS}}$ hold time	t_{CSH}	40	–	50	–	ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	t_{CRP}	5	–	5	–	ns	
Transition time (rise and fall)	t_T	1	50	1	50	ns	7
Refresh period for 2k-refresh version	t_{REF}	–	32	–	32	ms	
Refresh period for 4k-refresh version	t_{REF}	–	64	–	64	ms	
Refresh period for Low Power Version	t_{REF}	–	128	–	128	ms	
Read Cycle							
Access time from $\overline{\text{RAS}}$	t_{RAC}	–	50	–	60	ns	8, 9
Access time from $\overline{\text{CAS}}$	t_{CAC}	–	13	–	15	ns	8, 9

AC Characteristics (cont'd) [5, 6]
T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 % / V_{CC} = 3.3 V ± 0.3 V, t_T = 2 ns

Parameter	Symbol	Limit Values				Unit	Note
		-50		-60			
		min.	max.	min.	max.		
Access time from column address	t_{AA}	–	25	–	30	ns	8, 10
$\overline{\text{OE}}$ access time	t_{OEA}	–	13	–	15	ns	
Column address to $\overline{\text{RAS}}$ lead time	t_{RAL}	25	–	30	–	ns	
Read command setup time	t_{RCS}	0	–	0	–	ns	
Read command hold time	t_{RCH}	0	–	0	–	ns	11
Read command hold time referenced to $\overline{\text{RAS}}$	t_{RRH}	0	–	0	–	ns	11
$\overline{\text{CAS}}$ to output in low-Z	t_{CLZ}	0	–	0	–	ns	8
Output buffer turn-off delay	t_{OFF}	0	13	0	15	ns	12
Output turn-off delay from $\overline{\text{OE}}$	t_{OEZ}	0	13	0	15	ns	12
Data to $\overline{\text{CAS}}$ low delay	t_{DZC}	0	–	0	–	ns	13
Data to $\overline{\text{OE}}$ low delay	t_{DZO}	0	–	0	–	ns	13
$\overline{\text{CAS}}$ high to data delay	t_{CDD}	10	–	13	–	ns	14
$\overline{\text{OE}}$ high to data delay	t_{ODD}	10	–	13	–	ns	14

Write Cycle

Write command hold time	t_{WCH}	8	–	10	–	ns	
Write command pulse width	t_{WP}	8	–	10	–	ns	
Write command setup time	t_{WCS}	0	–	0	–	ns	15
Write command to $\overline{\text{RAS}}$ lead time	t_{RWL}	8	–	10	–	ns	
Write command to $\overline{\text{CAS}}$ lead time	t_{CWL}	8	–	10	–	ns	
Data setup time	t_{DS}	0	–	0	–	ns	16
Data hold time	t_{DH}	8	–	10	–	ns	16

Read-Modify-Write Cycle

Read-write cycle time	t_{RWC}	113	–	138	–	ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ delay time	t_{RWD}	64	–	77	–	ns	15
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ delay time	t_{CWD}	27	–	32	–	ns	15
Column address to $\overline{\text{WE}}$ delay time	t_{AWD}	39	–	47	–	ns	15
$\overline{\text{OE}}$ command hold time	t_{OEH}	10	–	13	–	ns	

AC Characteristics (cont'd) [5, 6]

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 % / V_{CC} = 3.3 V ± 0.3 V, t_T = 2 ns

Parameter	Symbol	Limit Values				Unit	Note
		-50		-60			
		min.	max.	min.	max.		
Hyper Page Mode (EDO) Cycle							
Hyper page mode (EDO) cycle time	t_{HPC}	20	–	25	–	ns	
$\overline{\text{CAS}}$ precharge time	t_{CP}	8	–	10	–	ns	
Access time from $\overline{\text{CAS}}$ precharge	t_{CPA}	–	27	–	32	ns	7
Output data hold time	t_{COH}	5	–	5	–	ns	
$\overline{\text{RAS}}$ pulse width in EDO mode	t_{RAS}	50	200k	60	200k	ns	
$\overline{\text{CAS}}$ precharge to $\overline{\text{RAS}}$ delay	t_{RHCP}	27	–	32	–	ns	
$\overline{\text{OE}}$ setup time prior to $\overline{\text{CAS}}$	t_{OES}	5	–	5	–	ns	
Hyper Page Mode (EDO) Read-Modify-Write Cycle							
Hyper page mode (EDO) read-write cycle time	t_{PRWC}	58	–	68	–	ns	
$\overline{\text{CAS}}$ precharge to $\overline{\text{WE}}$	t_{CPWD}	41	–	49	–	ns	
$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ Refresh Cycle							
$\overline{\text{CAS}}$ setup time	t_{CSR}	10	–	10	–	ns	
$\overline{\text{CAS}}$ hold time	t_{CHR}	10	–	10	–	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	t_{RPC}	5	–	5	–	ns	
Write to $\overline{\text{RAS}}$ precharge time	t_{WRP}	10	–	10	–	ns	
Write hold time referenced to $\overline{\text{RAS}}$	t_{WRH}	10	–	10	–	ns	
$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ Counter Test Cycle							
$\overline{\text{CAS}}$ precharge time ($\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ counter test cycle)	t_{CPT}	35	–	40	–	ns	
Self Refresh Cycle (L-Version only)							
$\overline{\text{RAS}}$ pulse width	t_{RASS}	100k	–	100k	–	ns	17
$\overline{\text{RAS}}$ precharge time	t_{RPS}	95	–	110	–	ns	17
$\overline{\text{CAS}}$ hold time	t_{CHS}	– 50	–	– 50	–	ns	17

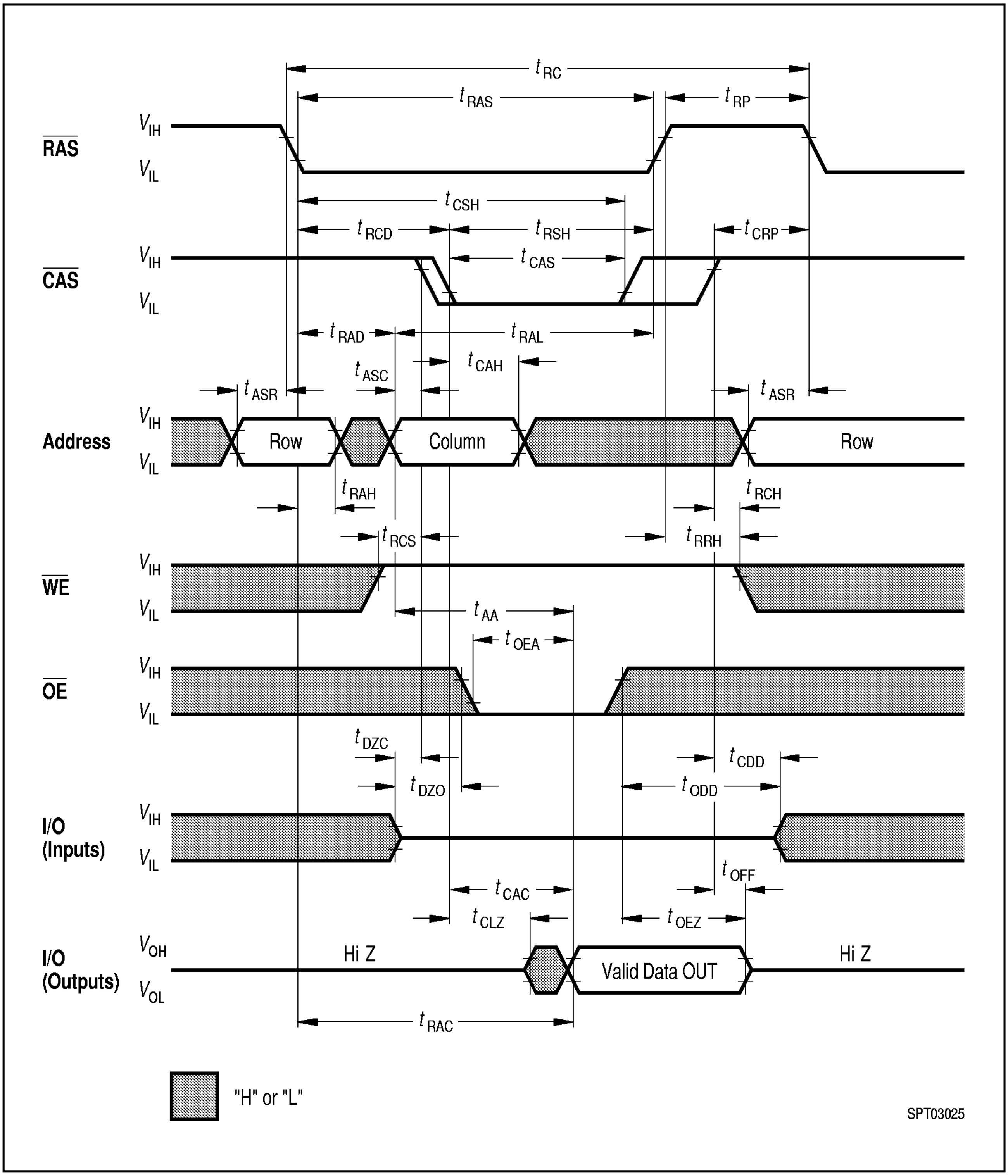
AC Characteristics (cont'd) [5, 6]

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 % / V_{CC} = 3.3 V ± 0.3 V, t_T = 2 ns

Parameter	Symbol	Limit Values				Unit	Note
		-50		-60			
		min.	max.	min.	max.		
Test Mode							
Write command setup time	t_{WTS}	10	–	10	–	ns	
Write command hold time	t_{WTH}	10	–	10	–	ns	
$\overline{\text{CAS}}$ hold time	t_{CHRT}	30	–	30	–	ns	
$\overline{\text{RAS}}$ hold time in test mode	t_{RAHT}	30	–	30	–	ns	

Notes

1. All voltages are referenced to V_{SS}.
2. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
3. I_{CC1} and I_{CC4} depend on output loading. Specified values are obtained with the output open.
4. Address can be changed once or less while $\overline{\text{RAS}}$ = V_{IL}. In case of I_{CC4} it can be changed once or less during a hyper page mode (EDO) cycle
5. An initial pause of 200 µs is required after power-up followed by 8 $\overline{\text{RAS}}$ cycles of which at least one cycle has to be a refresh cycle, before proper device operation is achieved. In case of using the internal refresh counter, a minimum of 8 $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ initialization cycles instead of 8 $\overline{\text{RAS}}$ cycles are required.
6. AC measurements assume t_{T} = 2 ns.
7. $V_{\text{IH (MIN.)}}$ and $V_{\text{IL (MAX.)}}$ are reference levels for measuring timing of input signals. Transition times are also measured between V_{IH} and V_{IL}.
8. Measured with the specified current load and 100 pF at V_{OL} = 0.8 V and V_{OH} = 2.0 V. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{AA}, t_{CPA}, t_{OEA} . t_{CAC} is measured from tristate.
9. Operation within the $t_{\text{RCD (MAX.)}}$ limit ensures that $t_{\text{RAC (MAX.)}}$ can be met. $t_{\text{RCD (MAX.)}}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{\text{RCD (MAX.)}}$ limit, then access time is controlled by t_{CAC}.
10. Operation within the $t_{\text{RAD (MAX.)}}$ limit ensures that $t_{\text{RAC (MAX.)}}$ can be met. $t_{\text{RAD (MAX.)}}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{\text{RAD (MAX.)}}$ limit, then access time is controlled by t_{AA}.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. $t_{\text{OFF (MAX.)}}$, $t_{\text{OEZ (MAX.)}}$ define the time at which the output achieves the open-circuit conditions and are not referenced to output voltage levels. t_{OFF} is referenced from the rising edge of $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$, whichever occurs last.
13. Either t_{DZC} or t_{DZO} must be satisfied.
14. Either t_{CDD} or t_{ODD} must be satisfied.
15. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{\text{WCS}} > t_{\text{WCS (MIN.)}}$, the cycle is an early write cycle and data out pin will remain open-circuit (high impedance) through the entire cycle; if $t_{\text{RWD}} > t_{\text{RWD (MIN.)}}$, $t_{\text{CWD}} > t_{\text{CWD (MIN.)}}$ and $t_{\text{AWD}} > t_{\text{AWD (MIN.)}}$, the cycle is a read-write cycle and I/O will contain data read from the selected cells. If neither of the above sets of conditions is satisfied, the condition of I/O (at access time) is indeterminate.
16. These parameters are referenced to the $\overline{\text{CAS}}$ leading edge in early write cycles and to the $\overline{\text{WE}}$ leading edge in read-write cycles.
17. When using Self Refresh mode, the following refresh operations must be performed to ensure proper DRAM operation:
    If row addresses are being refreshed on an evenly distributed manner over the refresh interval using CBR refresh cycles, then only one CBR cycle must be performed immediately after exit from Self Refresh.
    If row addresses are being refreshed in any other manner (ROR - Distributed/Burst; or CBR-Burst) over the refresh interval, then a full set of row refreshes must be performed immediately before entry to and immediately after exit from Self Refresh.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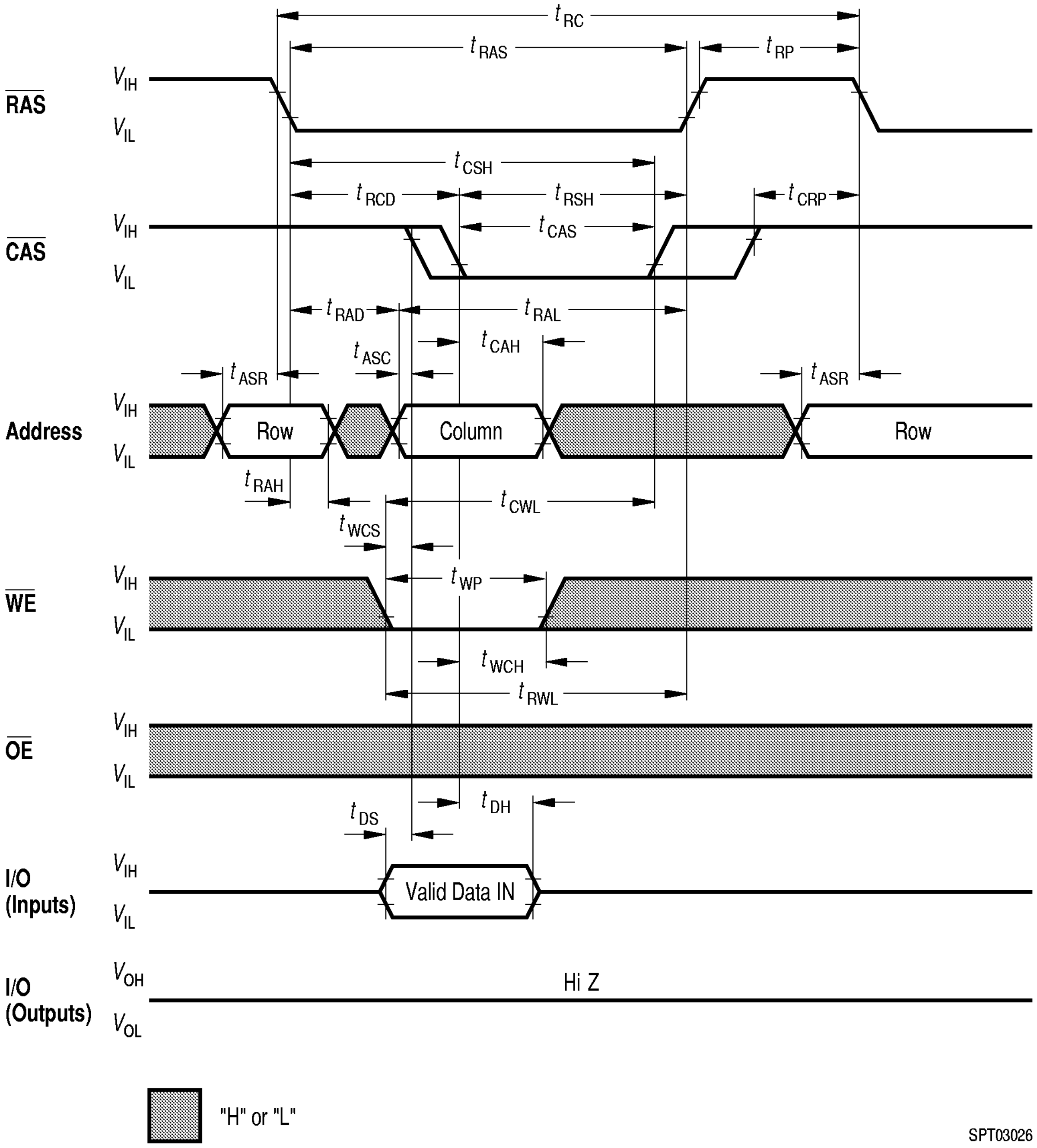
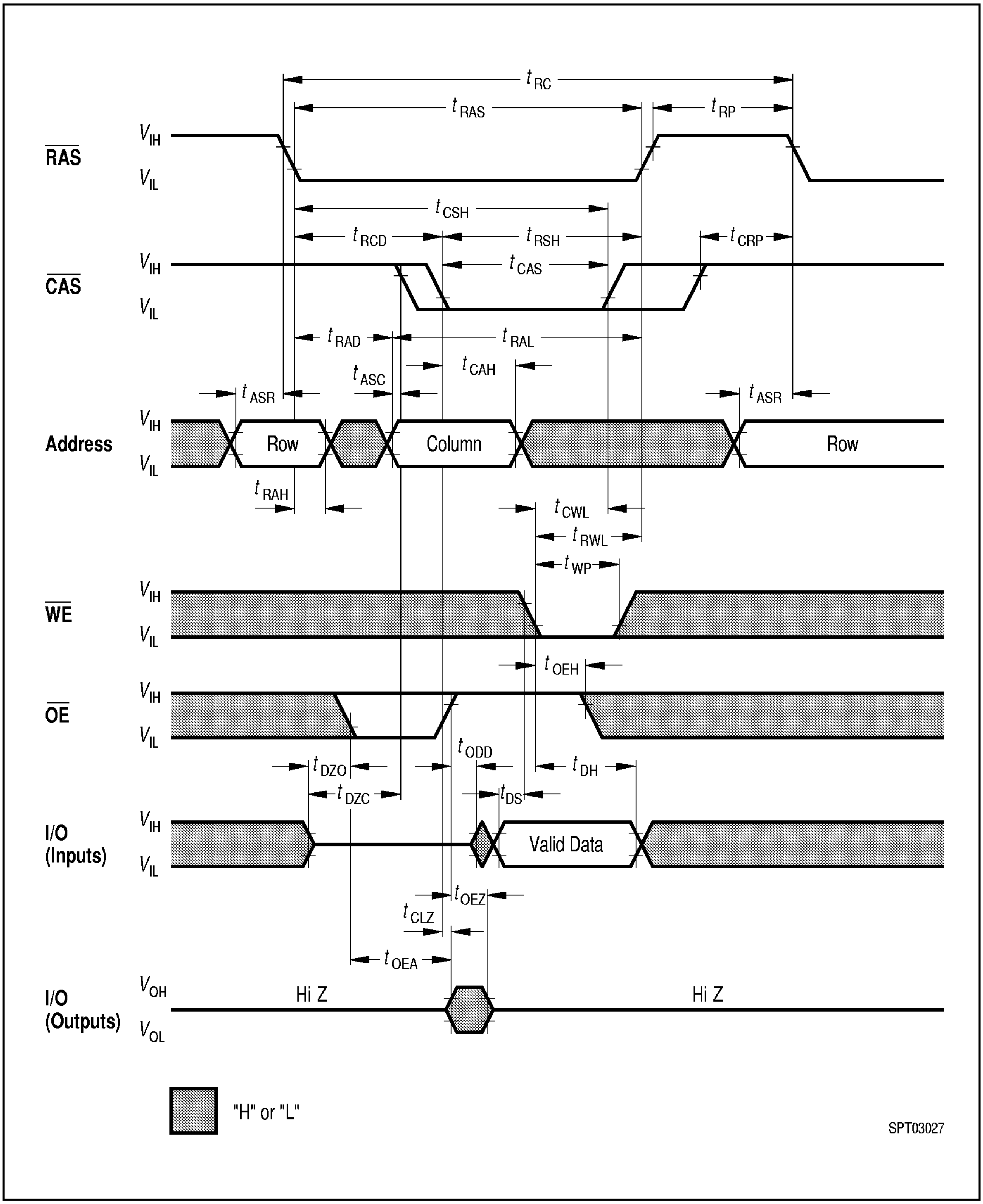
t RAH
t RCH
t RCS
t RRH
WE
t AA
t OEA
OE
t DZC
t CDD
t DZO
t ODD
I/O
(Inputs)
t OFF
t CAC
t CLZ
t OEZ
I/O
(Outputs)
V OH
V OL
Hi Z
Valid Data OUT
Hi Z
t RAC
"H" or "L"
SPT03025

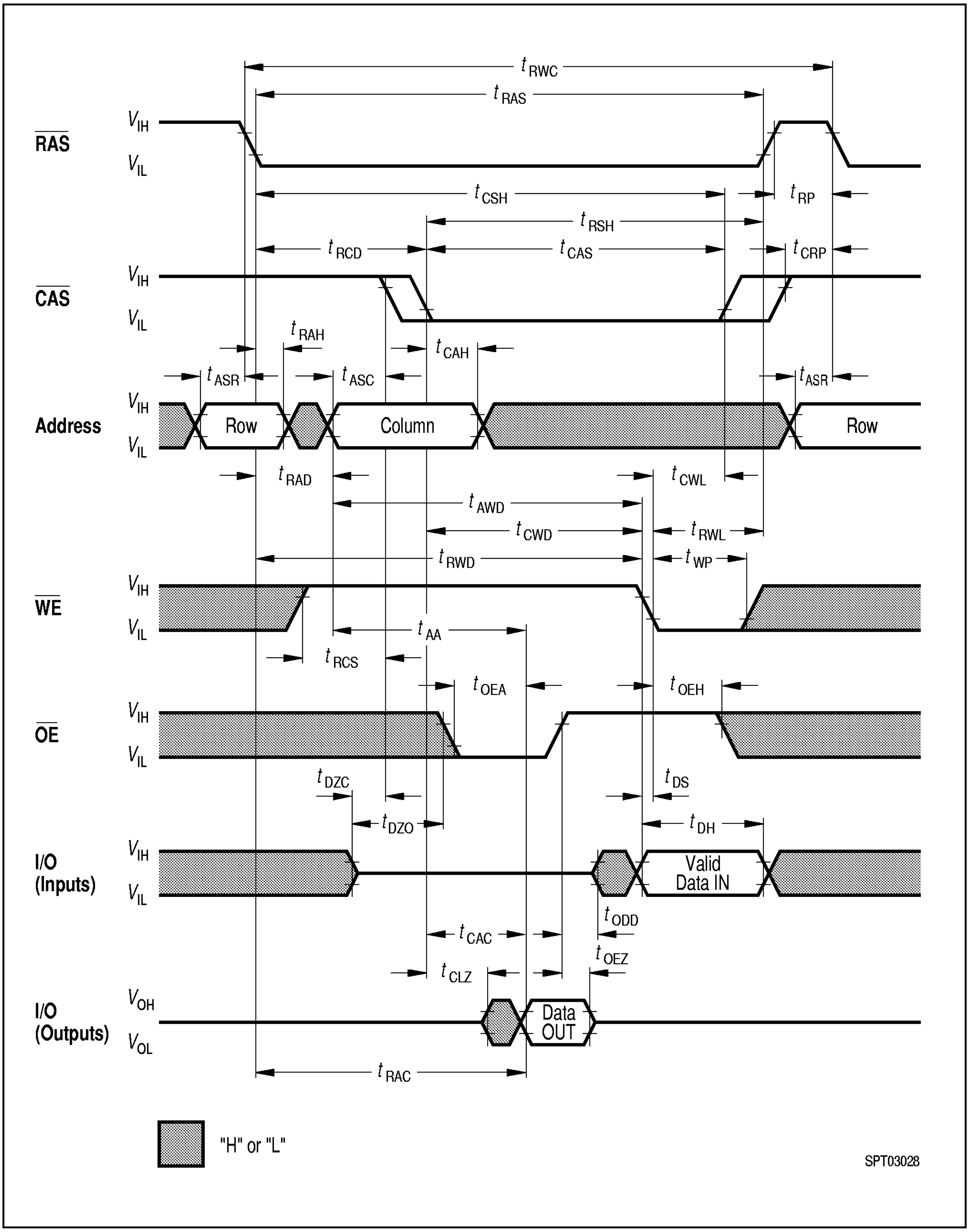
Read Cycle



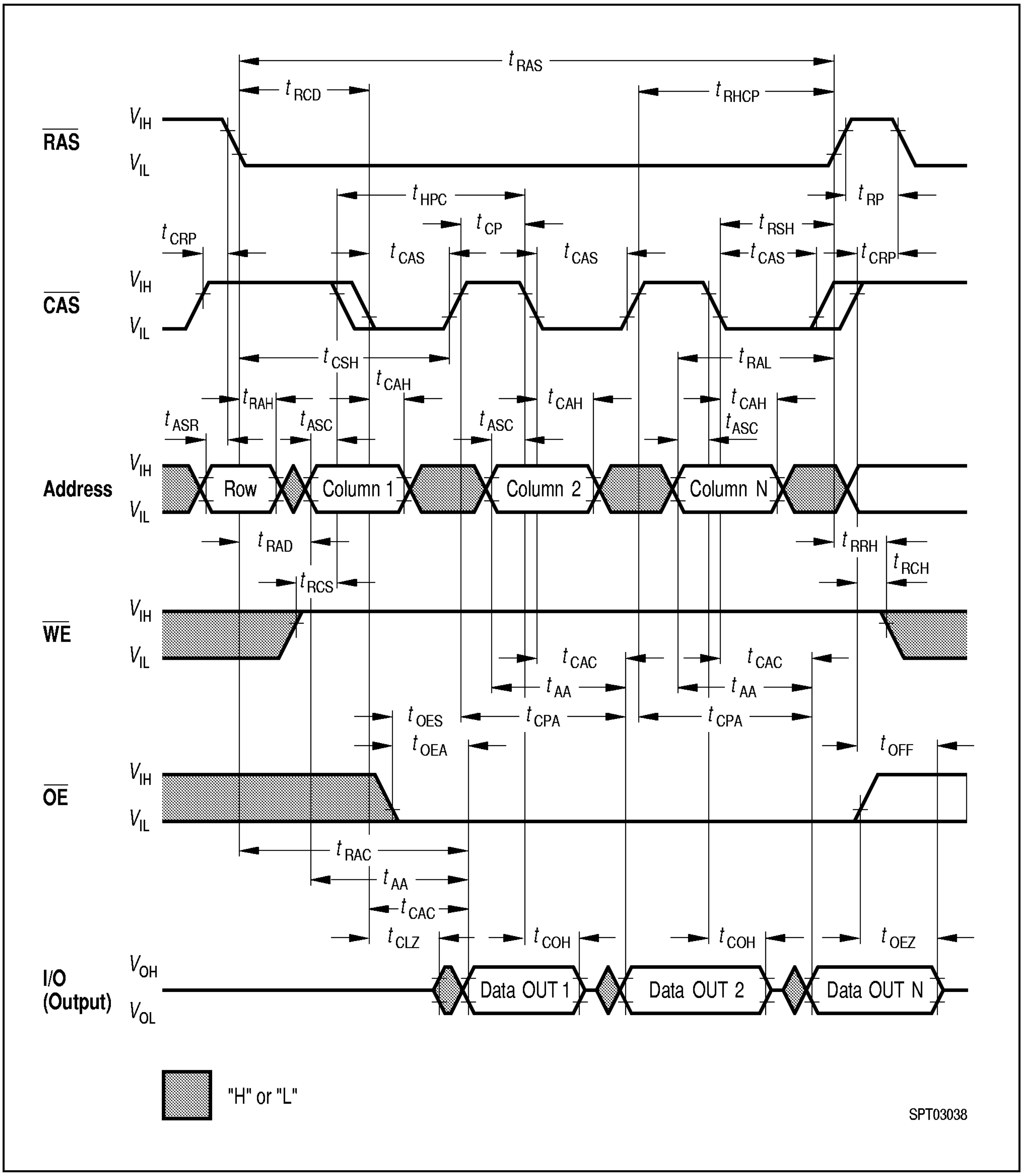
Write Cycle (Early Write)



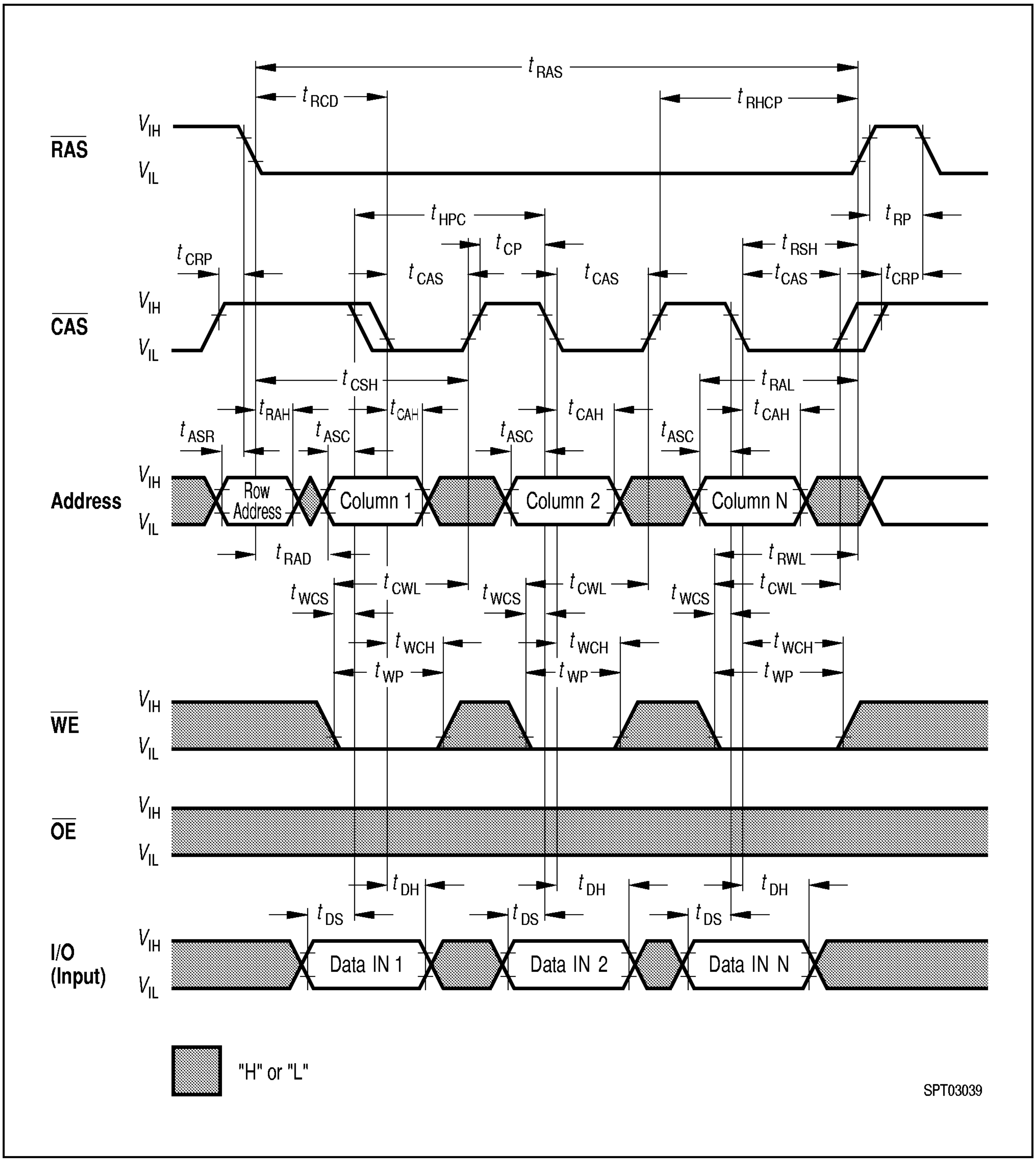
Write Cycle (OE Controlled Write)



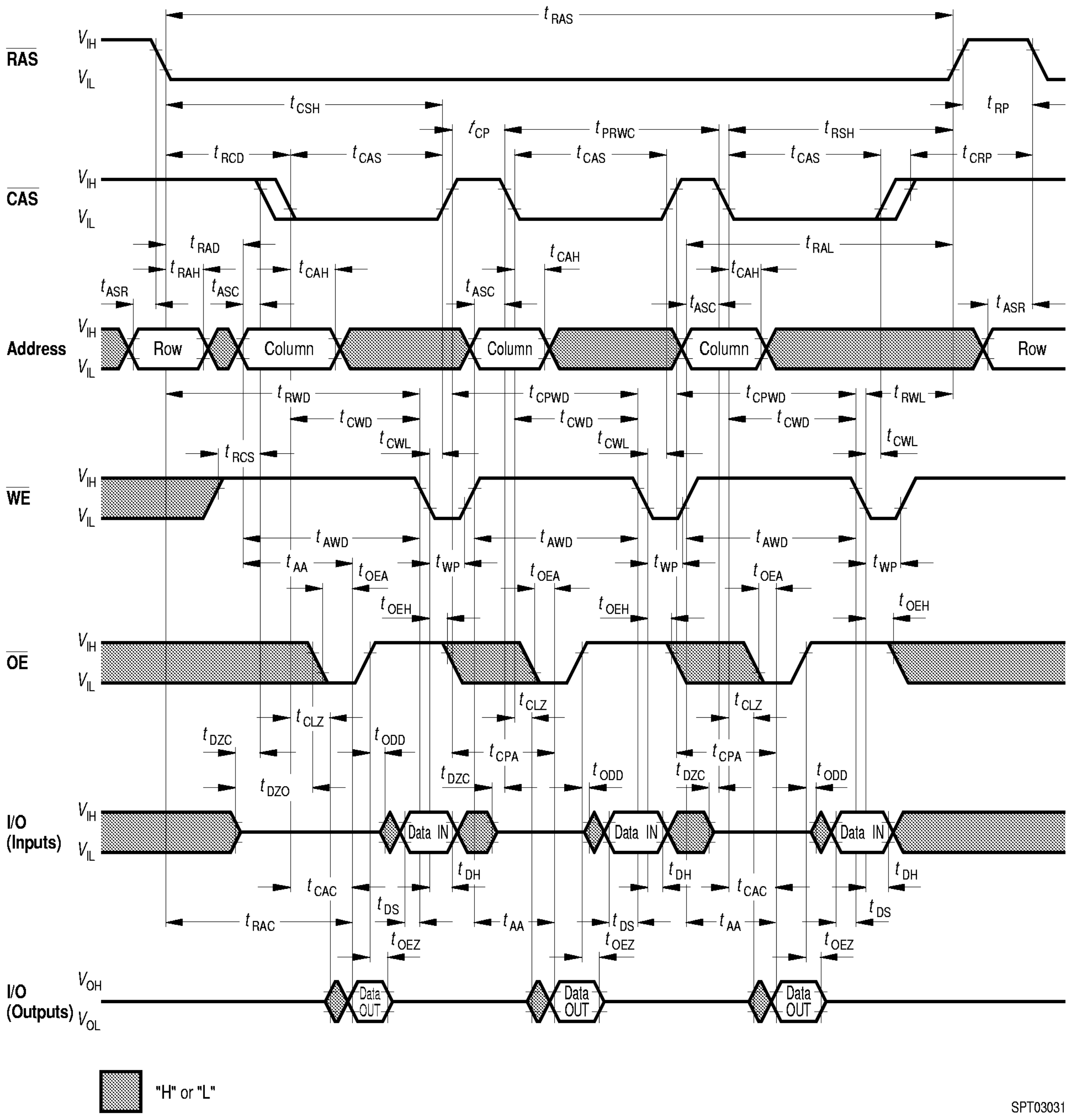
Read-Write (Read-Modify-Write) Cycle



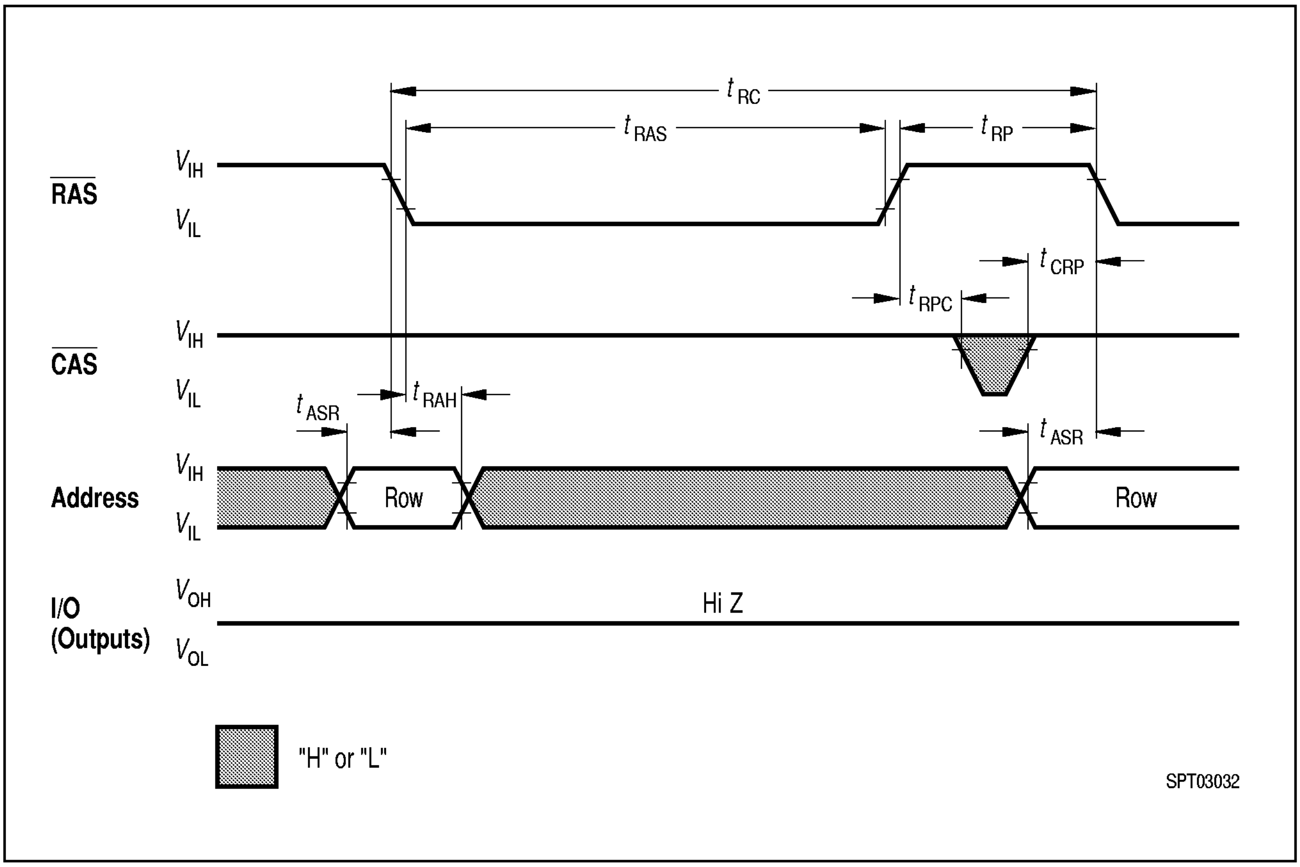
Hyper Page Mode (EDO) Read Cycle



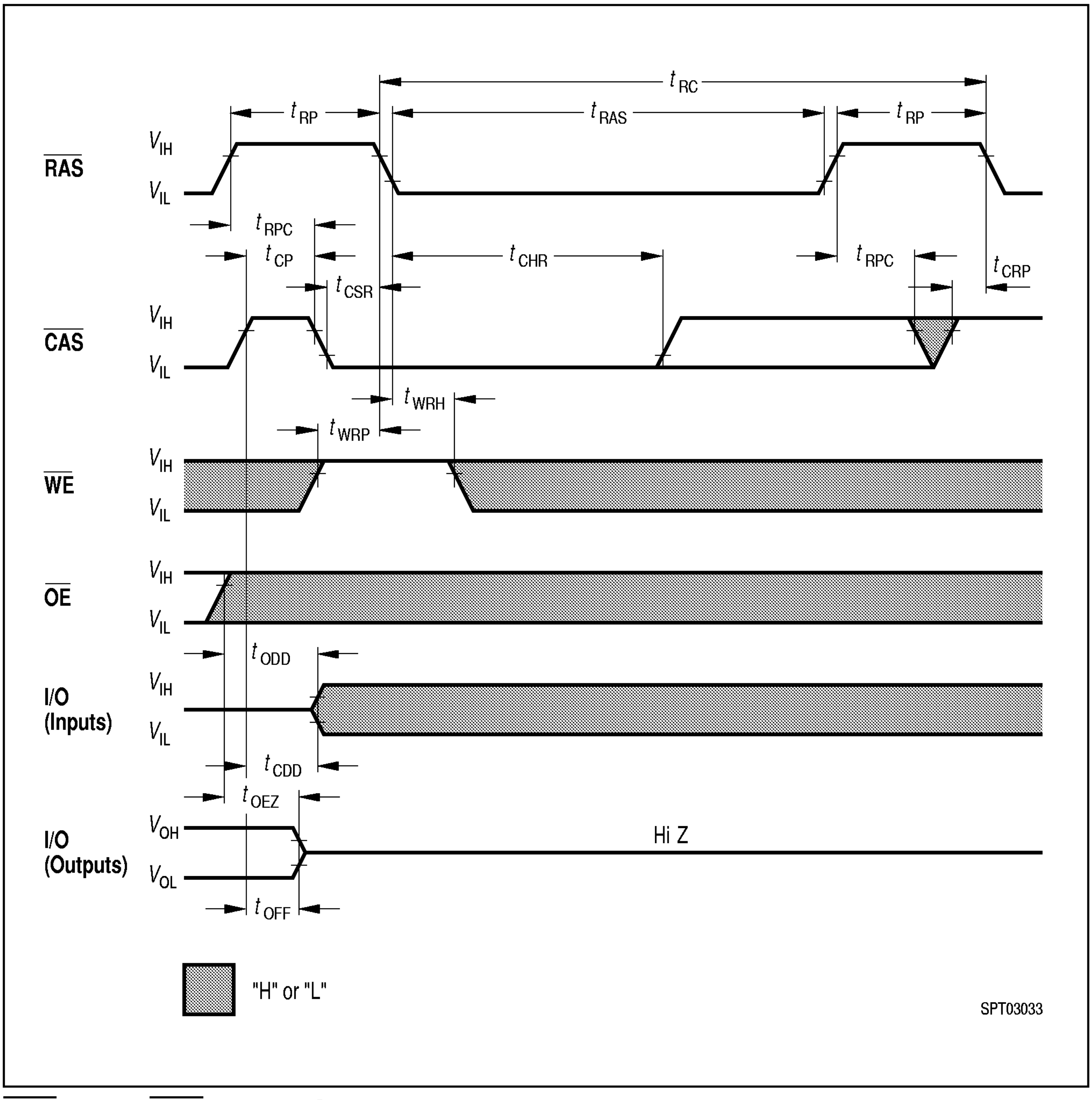
Hyper Page Mode (EDO) Early Write Cycle



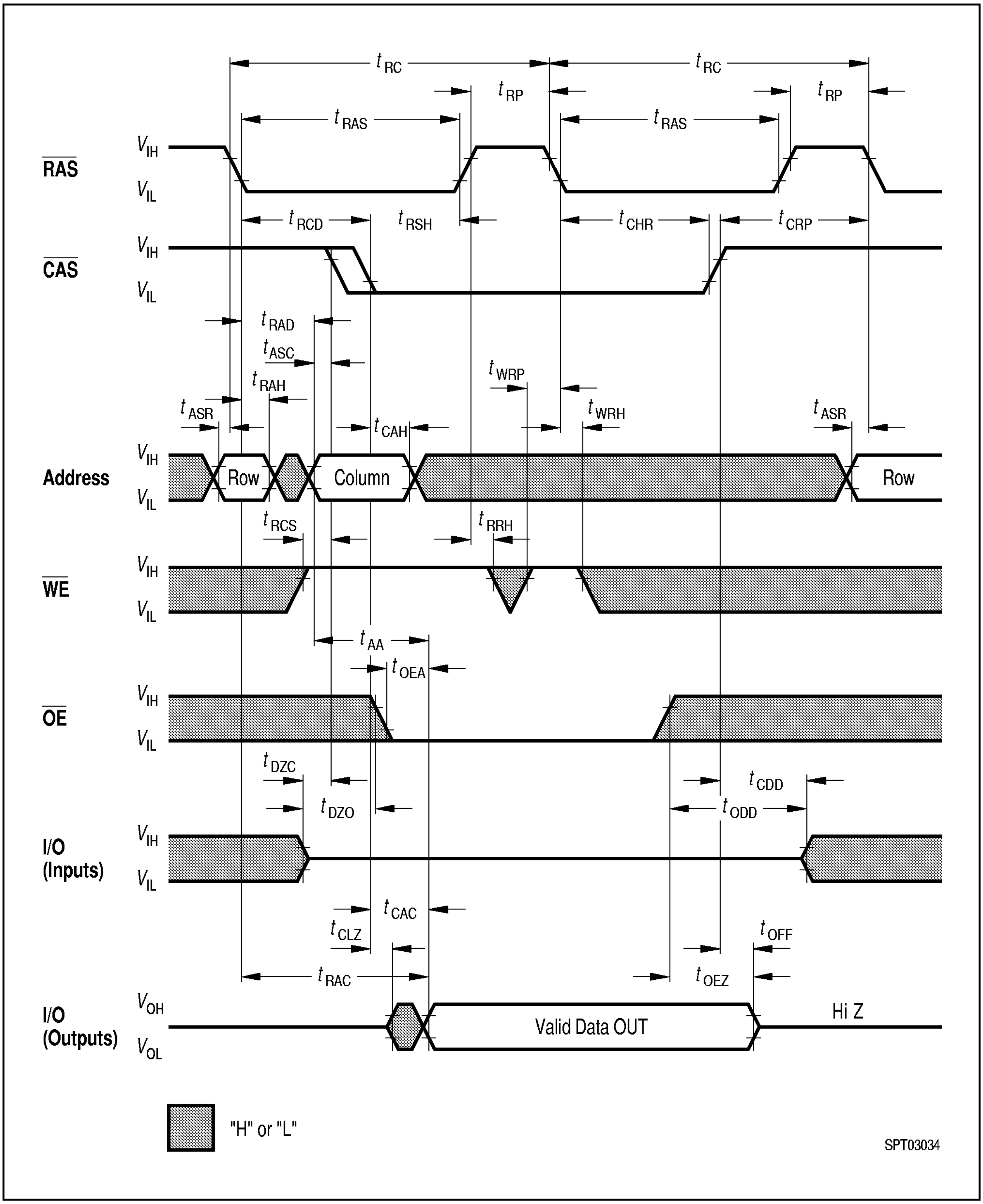
Hyper Page Mode (EDO) Late Write and Read-Modify Write Cycle



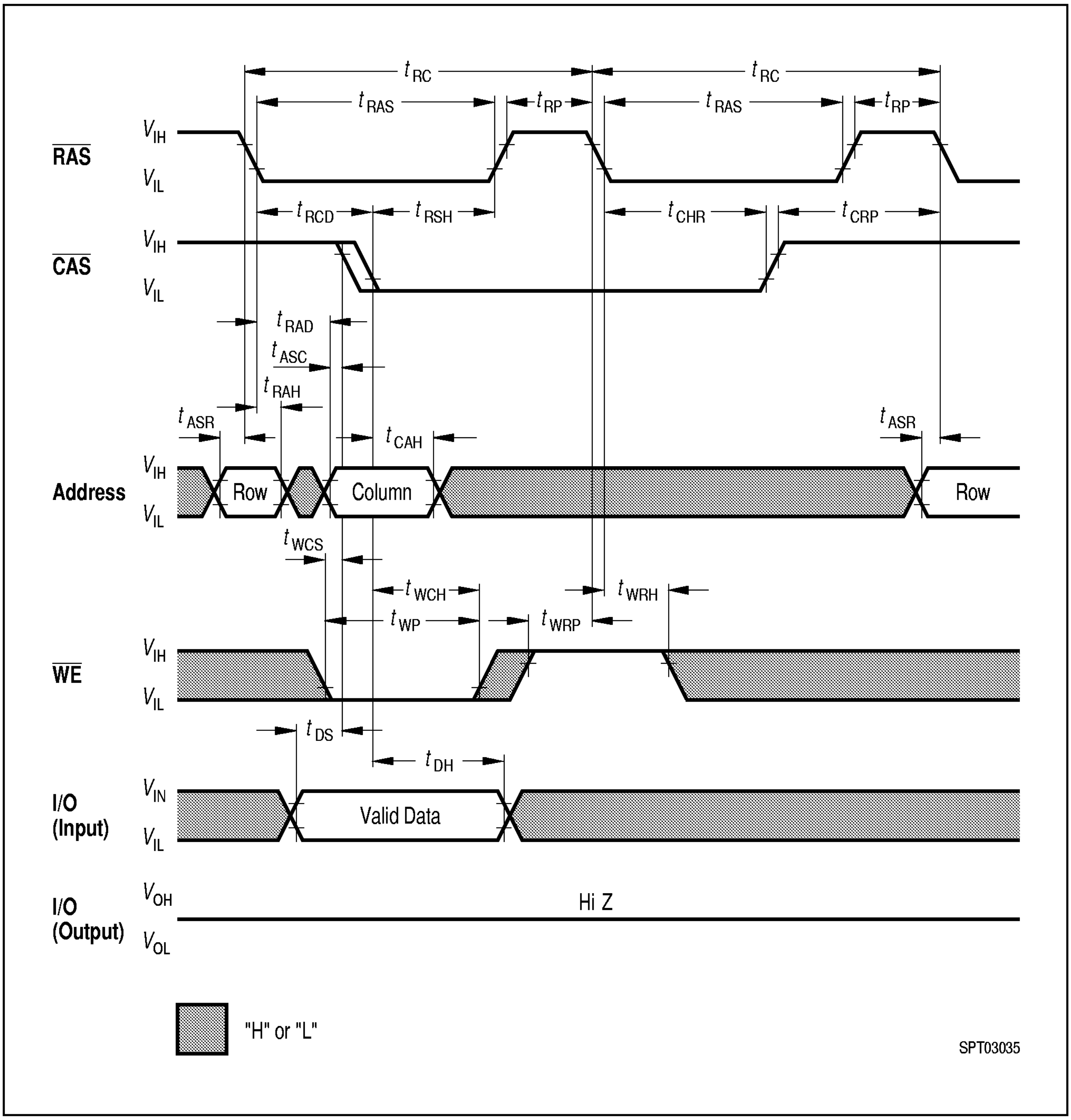
$\overline{\text{RAS}}$-only Refresh Cycle



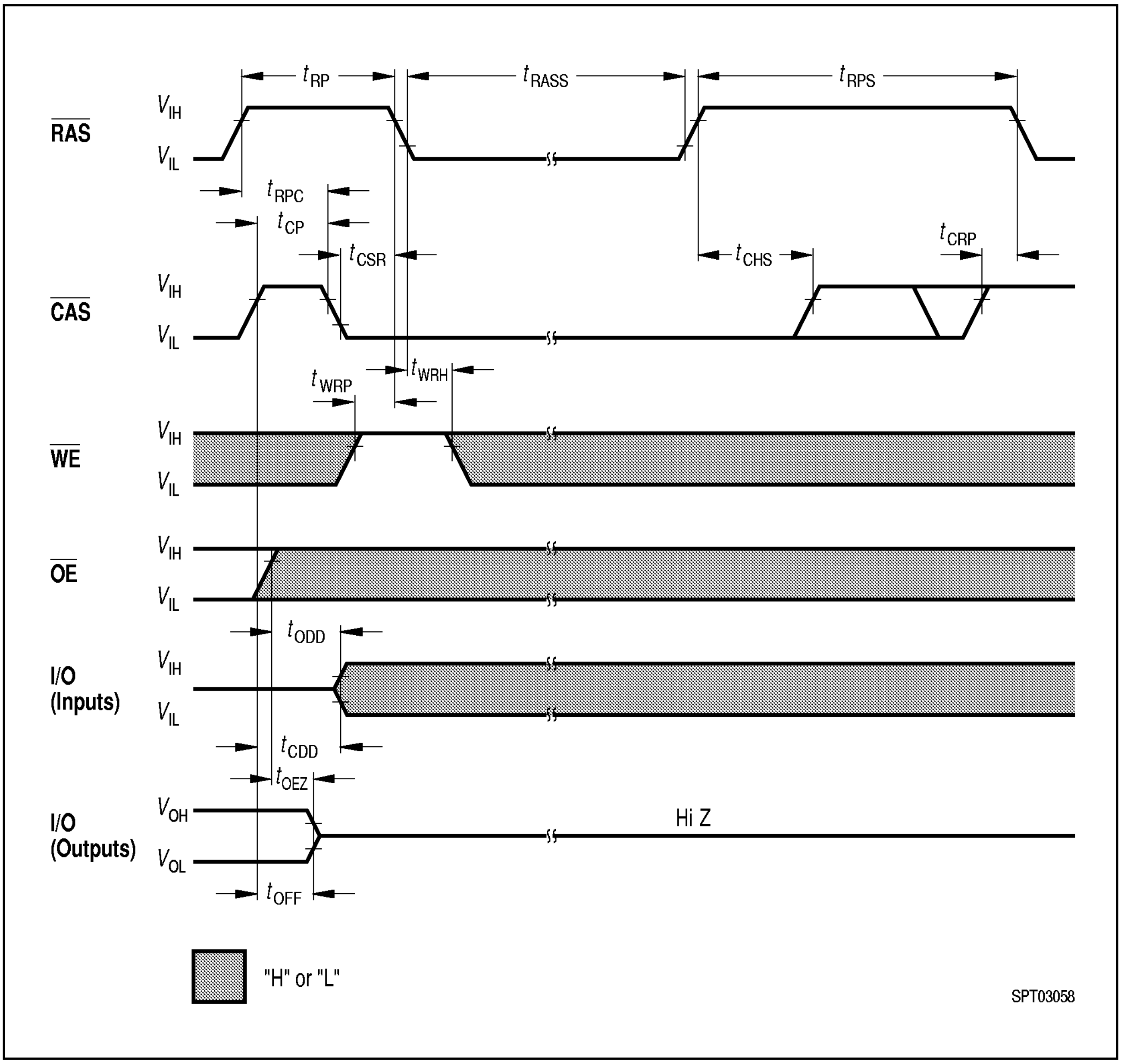
$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ Refresh Cycle



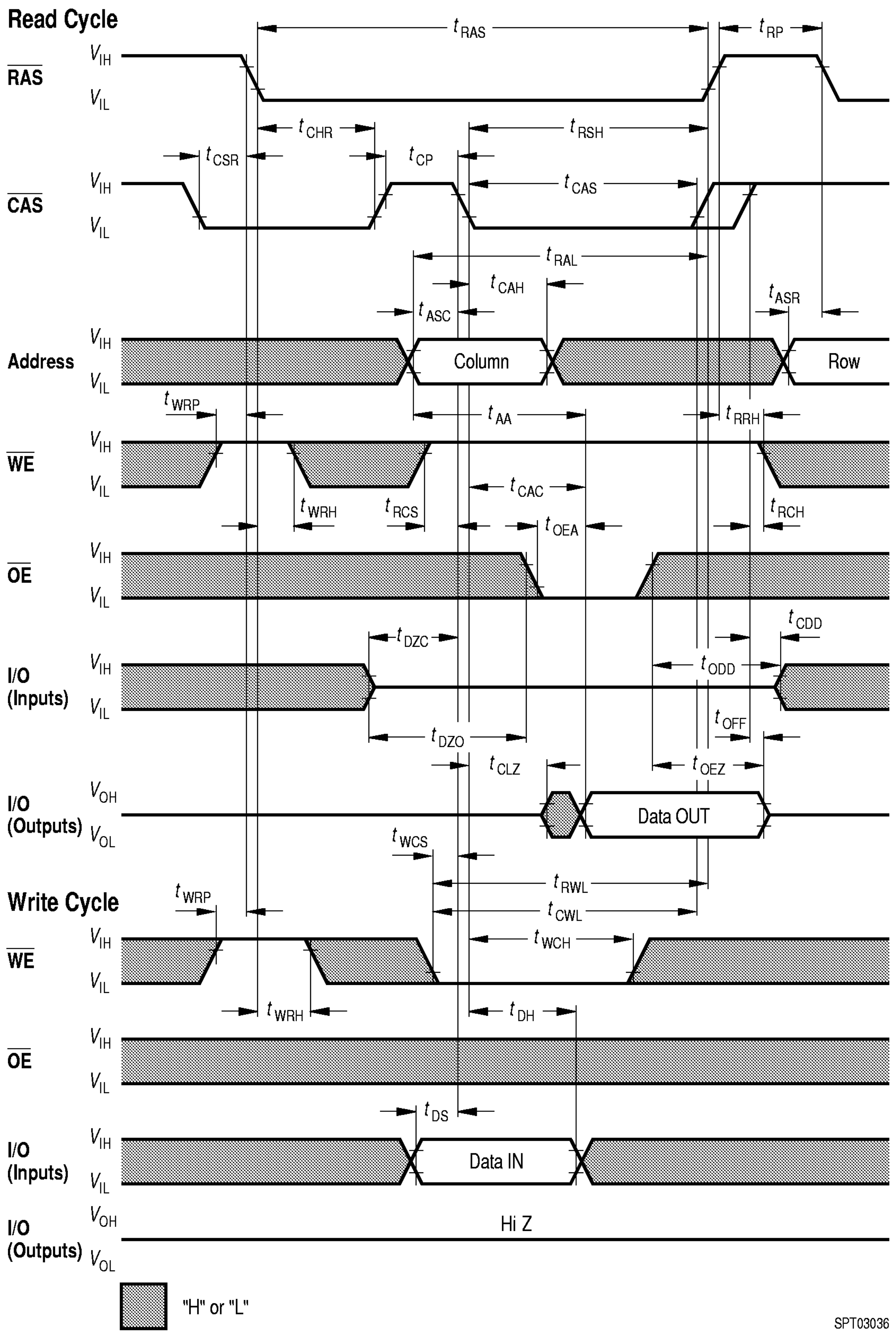
Hidden Refresh Cycle (Read) Cycle



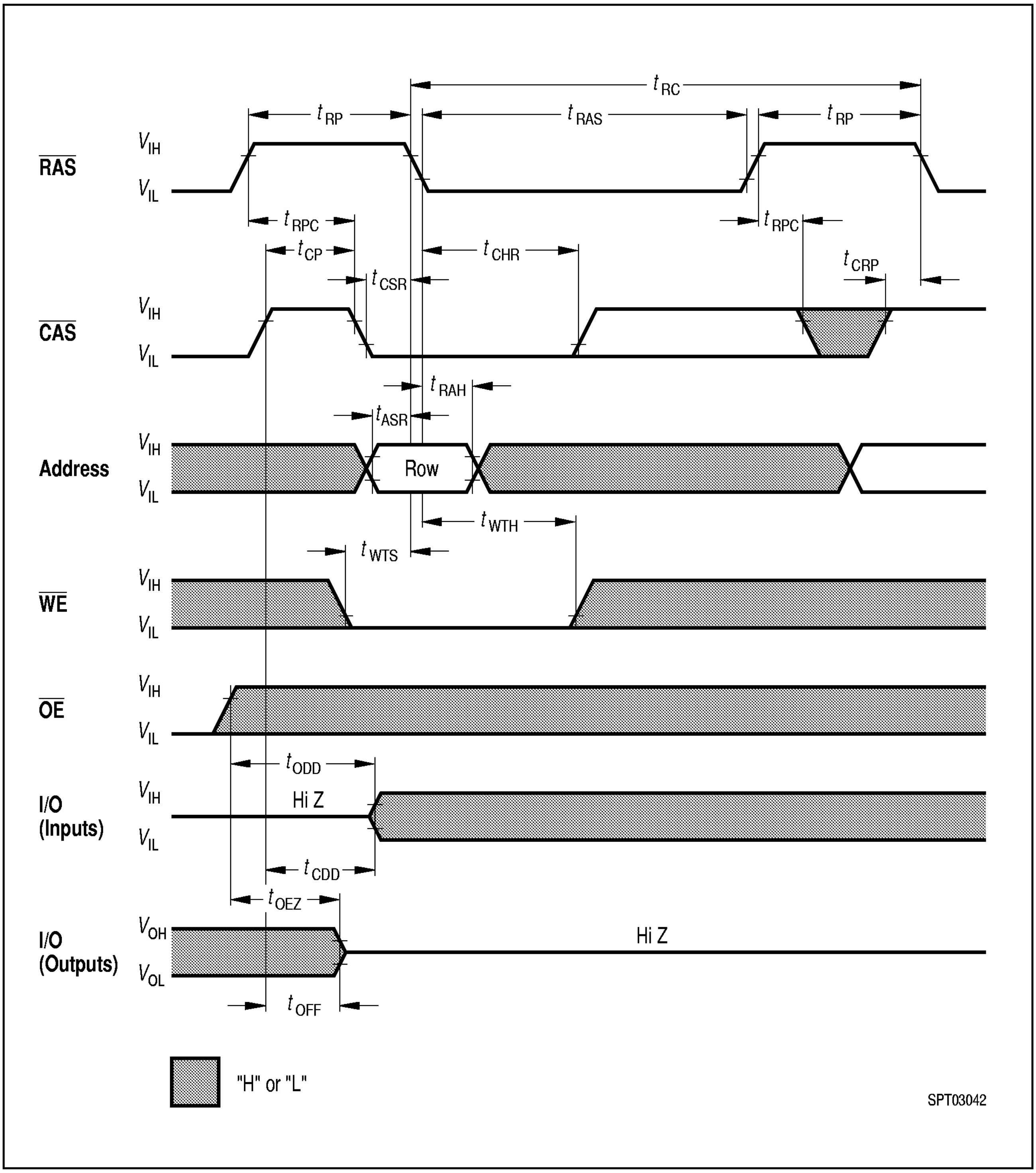
Hidden Refresh Early Write Cycle



Self Refresh



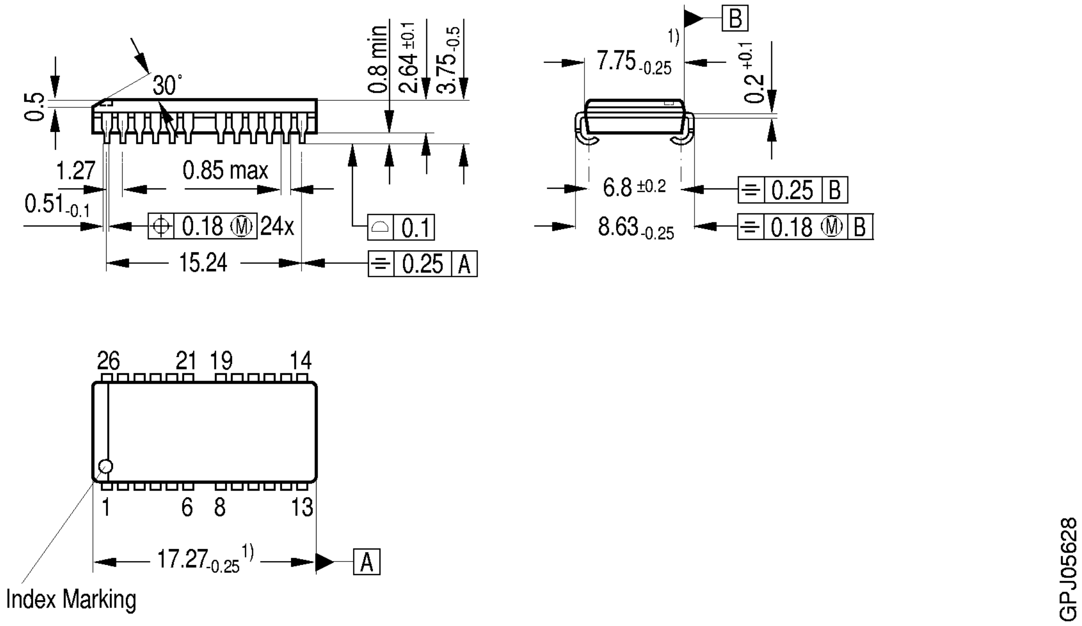
$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ Refresh Counter Test Cycle



Test Mode Entry

Package Outlines

Plastic Package P-SOJ-26/24-1 (SMD) (300mil)
(Plastic small outline J-leaded)



1) Does not include plastic or metal protrusions of 0.15 max per side

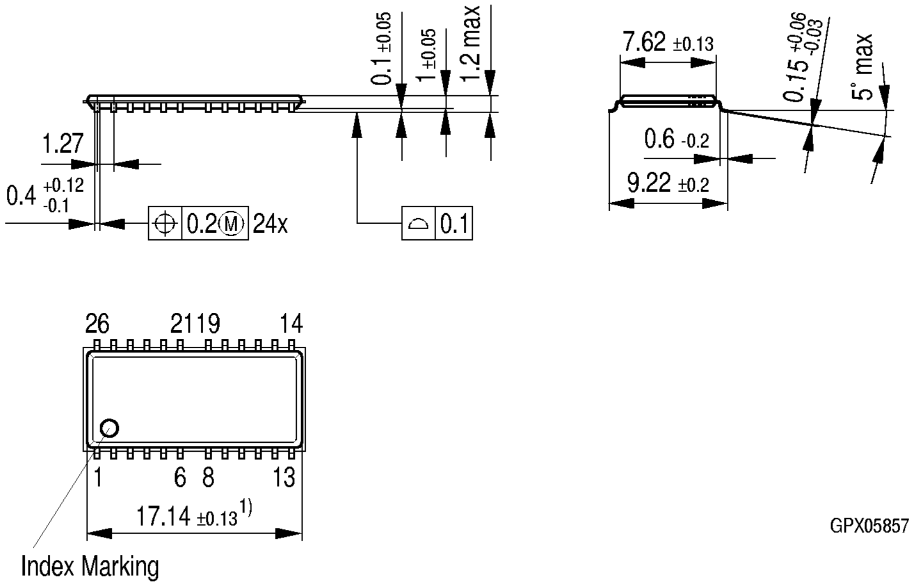
Sorts of Packing

Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm

Plastic Package P-TSOPII-26/24-1 (400 mil) (SMD)
(Plastic Thin Small Outline Package (Type II))



[1] Does not include plastic or metal protrusion of 0.15 max per side

Sorts of Packing

Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

SMD = Surface Mounted Device

Dimensions in mm