

FEATURES

- 9-bit ideal for byte-parity applications
- Flow-through configuration
- Extra TTL and ECL power/ground pins to minimize switching noise
- ECL and TTL enable inputs
- Dual supply
- 3.5ns max. D to Q
- PNP TTL inputs for low loading
- Choice of ECL compatibility: MECL 10KH (10Hxxx) or 100K (100Hxxx)
- Fully compatible with Motorola MC10H/100H600
- ESD protection of 2000V
- Available in 28-pin PLCC package

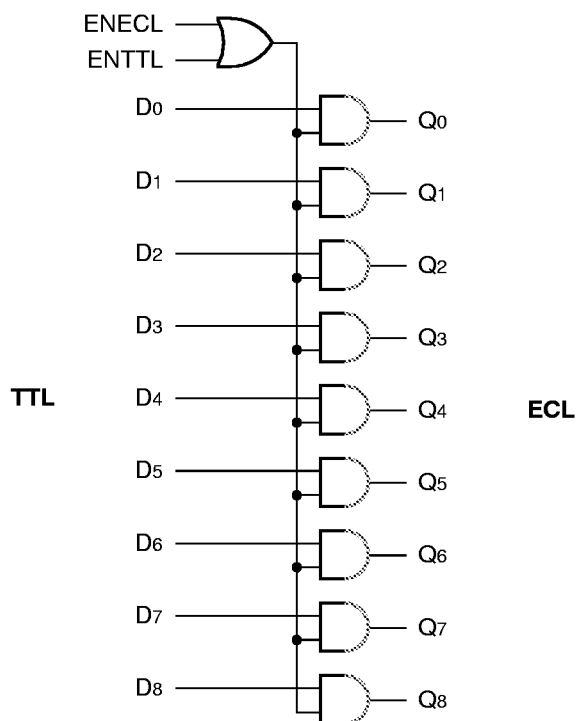
DESCRIPTION

The SY10/100H600 are 9-bit, dual supply TTL-to-ECL translators. Devices in the Synergy 9-bit translator series utilize the 28-lead PLCC for optimal power pinning, signal flow-through and electrical performance.

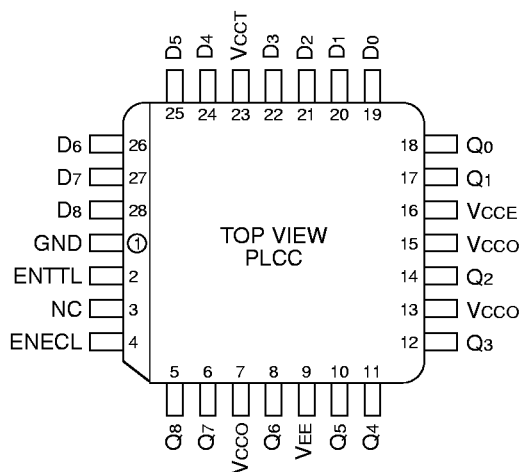
The H600 features both ECL and TTL logic enable controls for maximum flexibility.

The 10H version is compatible with MECL 10KH ECL logic levels. The 100H version is compatible with 100K levels.

BLOCK DIAGRAM



PIN CONFIGURATION



PIN NAMES

Pin	Function
GND	TTL Ground (0V)
VcCe	ECL Vcc (0V)
Vcco	ECL Vcc (0V) — Outputs
Vcct	TTL Supply (+5.0V)
VEE	ECL Supply (-5.2/-4.5V)
D0-D8	Data Inputs (TTL)
Q0-Q8	Data Outputs (ECL)
ENECL	Enable Control (ECL)
ENTTL	Enable Control (TTL)

TRUTH TABLE

ENECL	ENTTL	D	Q
H	X	H	H
H	X	L	L
X	H	H	H
X	H	L	L
L	L	X	L

DC ELECTRICAL CHARACTERISTICS
 $V_{CC} = 5.0V \pm 10\%$; $V_{EE} = -4.75V$ to $-5.5V$ (10H Version); $V_{EE} = -4.2V$ to $-5.5V$ (100H Version)

Symbol	Parameter	TA = 0°C		TA = +25°C		TA = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
IEE	Power Supply Current, ECL 10H 100H	—	125	—	125	—	125	mA	—
		—	122	—	123	—	132		
ICCH ICCL	Power Supply Current, TTL	—	48	—	48	—	48	mA	—
		—	50	—	50	—	50		

AC ELECTRICAL CHARACTERISTICS
 $V_{CC} = 5.0V \pm 10\%$; $V_{EE} = -4.75V$ to $-5.5V$ (10H Version); $V_{EE} = -4.2V$ to $-5.5V$ (100H Version)

Symbol	Parameter	TA = 0°C		TA = +25°C		TA = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
tPLH tPHL	Propagation Delay to Output D ENECL/ENTTL	1.4 1.8	3.0 3.7	1.5 1.9	3.2 3.9	1.7 2.0	3.5 4.1	ns	50Ω to -2.0V
tr tf	Output Rise/Fall Time 20% to 80%, 80% to 20%	0.5	1.5	0.5	1.5	0.5	1.5		

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10H600JC	J28-1	Commercial
SY10H600JCTR	J28-1	Commercial
SY100H600JC	J28-1	Commercial
SY100H600JCTR	J28-1	Commercial

28 LEAD PLASTIC LEADED CHIP CARRIER (J28-1)

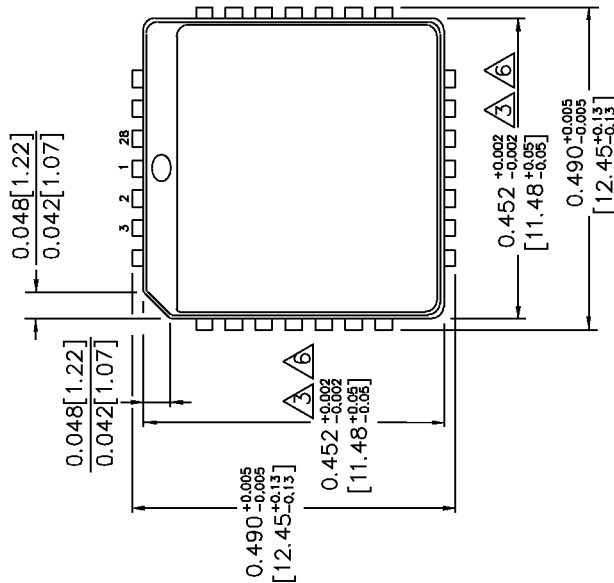
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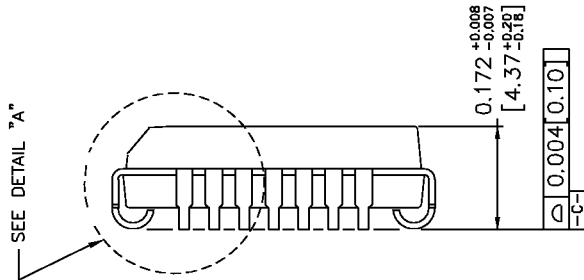
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REV	REVISION DESCRIPTION	DATE
01	CONVERT TO DESIGNER VERSION 4.0 FORMAT. ADD COVER PAGE TO SPEC. CHANGE BODY WIDTH DIMENSION FROM 0.450(11.43) TO 0.443(11.25). TYPOGRAPHICAL ERROR.	08/18/94
02	CONVERT DWG FROM DESIGNER TO AUTOCAD REL. 12. REFERENCE AMKOR DWG. NO. 34855 REV. 00.	02/22/96
03	CONVERT DWG TO REL. 13 AND ONE PAGE DOCUMENT.	02/18/98

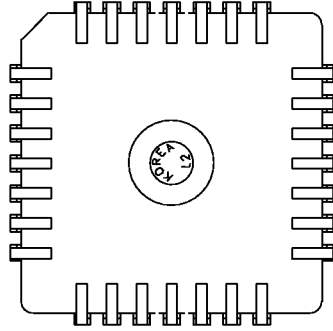
TOP VIEW



SIDE VIEW



BOTTOM VIEW



NOTES:

1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008[0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.



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APPROVALS	DATE	APPROVALS	DATE	SIZE	SCALE
ORIGINATOR: ERMIN G. LIRRUTIA	02/23/98	QUALITY: MARSHALL WILDER		A	28 LEAD PLCC
CHK'D: RON CHANG		DOCUMENT CONTROL: BRIAN SANFILIPPO			PACKAGE OUTLINE
RELEASE DATE:					THESE SPECIFICATIONS ARE THE PROPERTY OF SYNERGY SEMICONDUCTOR. ARE ISSUED IN STRICT CONFIDENCE AND SHALL NOT BE REPRODUCED, COPIED, OR USED AS THE BASIS FOR THE MANUFACTURE OR SALE OF APPARATUS WITHOUT WRITTEN PERMISSION.
					N/A
					REVISION
					03