T-79-15

TELEDYNE COMPONENTS

1430

FAST SETTLING, FET INPUT OPERATIONAL AMPLIFIER

FEATURES

- **Settling Time to ±0.01% (10V step)........200 ns Max**
- **Operating Temperature...................-55°C to +125°C**
- **Gain Bandwidth Product............................100 MHz**
- **Slew Rate..750V/µs**
- **Output...±11V, ±55 mA**

APPLICATIONS

- **Digital-to-Analog Converters**
- **Sample/Hold Circuits**
- **Pulse Amplifiers**
- **Wideband Amplifiers**

GENERAL DESCRIPTION

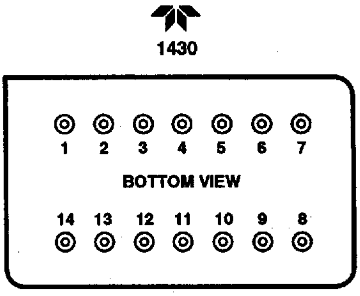
The 1430 is a high speed, precision, FET input hybrid op amp that features fast settling time, low bias current, high slew rate, wide bandwidth, and good phase margin. Guaranteed settling time of 200nsec (10V step to 0.01%) and a design that is tailored for inverting applications make the 1430 an ideal output amplifier for fast 12 bit D/A converters and other applications such as sample-hold amplifiers and radar pulse amplifiers.

The 1430 was carefully designed so that output settling time would not vary appreciably with closed loop gain (Figure 1). This is particularly important for current to voltage converter applications as with high speed current-output DACs (see Figure 2). The 1430 requires only a feedback capacitor for stability at closed-loop gains of unity and above.

The 1430 is packaged in a 14-pin metal platform package. Both the standard 1430 and the High Reliability (HR) 1430 are specified to operate over the -55°C to +125°C temperature range.

PIN CONFIGURATION

Pin No.	Designation
1	NC
2	TRIM
3	TRIM
4	-IN
5	+IN
6	$-V_{cc}$
7	NC
8	COM
9	NC
10	OUTPUT
11	$+V_{cc}$
12	TRIM
13	NC
14	NC



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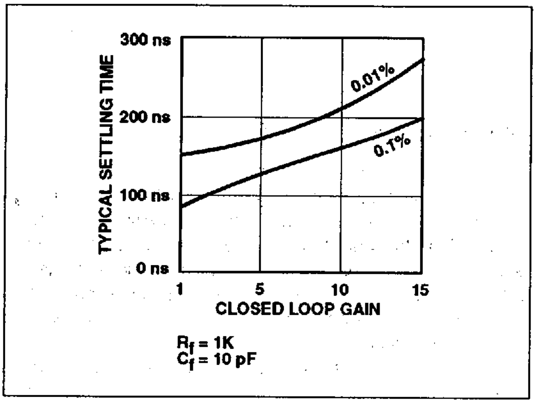

Figure 1. Settling Time vs Closed Loop Gain

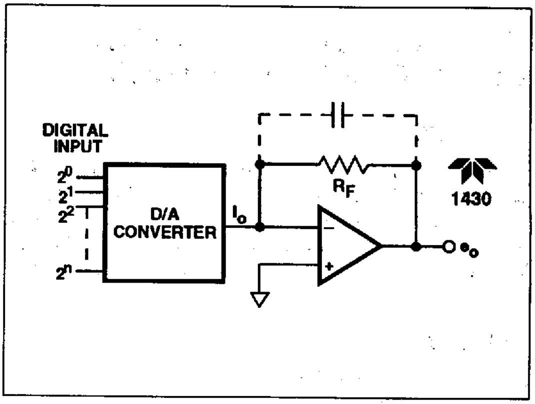

Figure 2. Output Amplifier for D/A Converter

ABSOLUTE MAXIMUM RATINGS

V_{CC} Supply Voltage ....±18V

V_{ID} Differential Input Voltage ....±V_{CC}

V_{ICM} Common Mode Input Voltage ....±V_{CC}

T_C Operating Temperature Range (Case)

1430 ....-55°C to +125°C

1430-HR ....-55°C to +125°C (1)

T_{STG} Storage Temperature Range ......–65°C to +150°C

(1) Operation above 85°C requires a 20°C/W heat sink.

DC CHARACTERISTICS: (Note 1) V_{CC} = ±15V, R_L = 1 kΩ, inverting circuits only, T_C = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	1430			1430-HR			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage		—	±0.5	**±2**	—	±0.5	**±2**	mV
V_{OS} TC	Input Offset Voltage Drift vs Temperature	Average, T_{MIN} to T_{MAX}	—	±40	—	—	±40	**±100**	µV/°C
I_B	Input Bias Current		—	±10	**±100**	—	±10	**±100**	pA
I_B TC	Input Bias Current Drift vs Temperature	Average, T_{MIN} to T_{MAX}	Doubles every 11°C			Doubles every 11°C			—
I_{OS}	Input Offset Current		—	±2	—	—	±2	—	pA
I_{OS} TC	Input Offset Current Drift vs Temperature	Average, T_{MIN} to T_{MAX}	Doubles every 11°C			Doubles every 11°C			—
A_{VOL}	Open-Loop Voltage Gain	R_L = 200Ω	**106**	120	—	**106**	120	—	dB
PSRR	Power Supply Rejection Ratio		—	80	—	—	80	—	dB
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±2V	—	65	—	—	65	—	dB
CMR	Common-Mode Range (DC Linear Operation)		—	+3/-10	—	—	+3/-10	—	V
Z_{ID}	Differential Input Impedance		—	$10^{11}\|\|3$	—	—	$10^{11}\|\|3$	—	Ω||pF
Z_{ICM}	Common-Mode Input Impedance		—	$10^{11}\|\|3$	—	—	$10^{11}\|\|3$	—	Ω||pF
V_O	Output Voltage Swing	R_L = 200Ω	**±10**	±11	—	**±10**	±11	—	V
I_O	Output Current	R_L = 200Ω	**±50**	±55	—	**±50**	±55	—	mA
I_{SC}	Output Short-Circuit Current		—	±110	—	—	±110	—	mA
R_O	Output Resistance (DC Open-Loop)		—	1000	—	—	1000	—	Ω
V_{CC}	Supply Voltage Range (Operating)		±10	±15	±18	±10	±15	±18	V
I_{CC}	Quiescent Supply Current		—	±20	**±25**	—	±20	**±25**	mA

NOTES: 1. Limits printed in **boldface** type are guaranteed and 100% production tested. Limits in normal font are guaranteed but not 100% production tested.

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AC CHARACTERISTICS: (Note 1) $V_{CC} = \pm 15V$, $R_L = 1\ k\Omega$, inverting circuits only, $T_C = 25°C$, unless otherwise noted.

Symbol	Parameter	Test Conditions	1430			1430-HR			Unit
			Min	Typ	Max	Min	Typ	Max	
S_R	Slew Rate		—	750	—	—	750	—	V/µs
GBWP	Gain-Bandwidth Product	f = 1 MHz	80	100	—	80	100	—	MHz
UGBW	Unity-Gain Bandwidth		—	60	—	—	60	—	MHz
t_s	Settling Time ($A_{CL} = -1$)	10V step/1%	—	70	—	—	70	—	ns
		10V step/0.1%	—	85	—	—	85	—	ns
		10V step/0.01%	—	175	200	—	175	200	ns
		5V step/1%	—	70	—	—	70	—	ns
		5V step/0.1%	—	100	—	—	100	—	ns
		5V step/0.01%	—	180	—	—	180	—	ns
		2V step/1%	—	80	—	—	80	—	ns
		2V step/0.1%	—	100	—	—	100	—	ns
		2V step/0.01%	—	240	—	—	240	—	ns
e_n	Input Voltage Noise Density	f = 1 kHz	—	16	—	—	16	—	nV/√Hz
i_n	Input Current Noise Density	f = 1 kHz	—	0.2	—	—	0.2	—	pA/√Hz
C_L	Capacitive Load (maximum w/o oscillation)		100	—	—	100	—	—	pF

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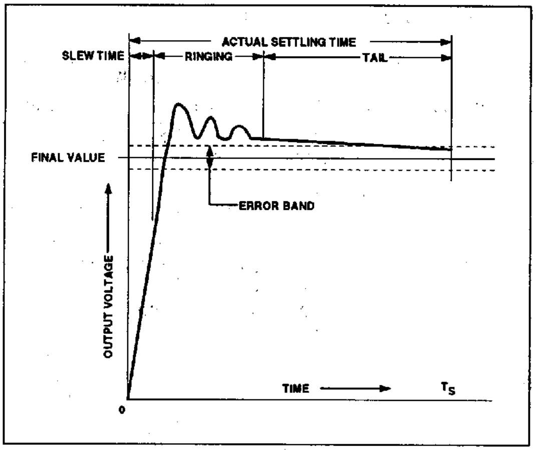

Figure 3. The Composition of Settling Time

Defining Settling Time

Settling time is the important specification when handling fast (sub-microsecond rise time), precision (0.1% or better amplitude accuracy) pulses. Settling time is the total time required, after the application of an input step (voltage or current), for a circuit's output to reach and stay within an error band specified in relation to the output's final value (see Figure 3).

Settling time cannot be predicted from bandwidth or slew rate. A step input to the amplifier will cause the output to slew at its maximum rate toward the final value. When this value is reached the output will usually overshoot slightly and "ring" as it settles toward the final value. Settling time includes not only the slew rate but also that portion of the ringing time in which the peaks exceed the settling time error band.

The error band is generally expressed as a percentage of the op-amps full scale output (i.e. 0.01% or 1 mV for a 10V amplifier). When observing settling time on an oscilloscope the amplifier may appear to have settled because the ringing has ceased but the observed value is outside the error band for a few seconds until it drifts within the error band. This "long tail" phenomenon is often a source of error. The long tail makes it virtually impossible to calculate settling time by using slew rate, and ringing characteristics as the sole factors. Also, knowing the settling time to a given accuracy (i.e. 0.1%) is not helpful in extrapolating the settling time to a higher accuracy, such as 0.01% and vice versa.

If settling time cannot be extrapolated, calculated, guessed or ignored, it must be measured. This can be difficult and misleading if the proper procedures are not followed precisely. (Figure 4 illustrates the 1430's settling characteristics using the test circuit shown in Figure 5A).

Measuring Settling Time

It is not possible to obtain 0.1% or 0.01% accurate measurements directly from an oscilloscope looking at the output waveform. Measuring a 10V signal, at high sensitivity for proper resolution, will overdrive the scope's input amplifier such that it's own recovery time will be much longer than the settling time being measured. Measuring settling time to 0.01% requires a clipping amplifier to prevent overloading the oscilloscope's input (Figure 5B).

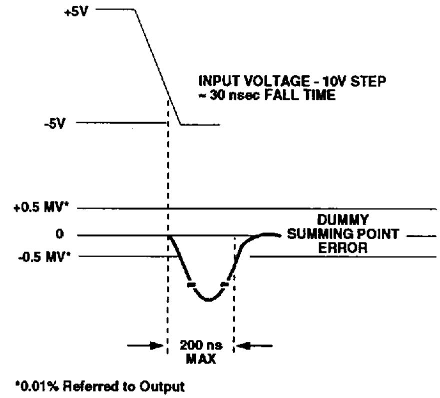

Figure 4. 1430/1430-HR Settling Time

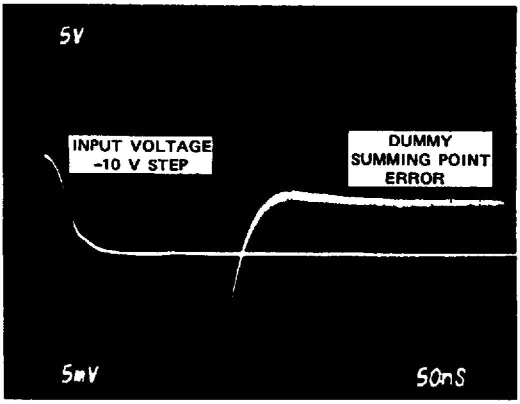

Figure 5. Test Circuit and Clipping Amplifier

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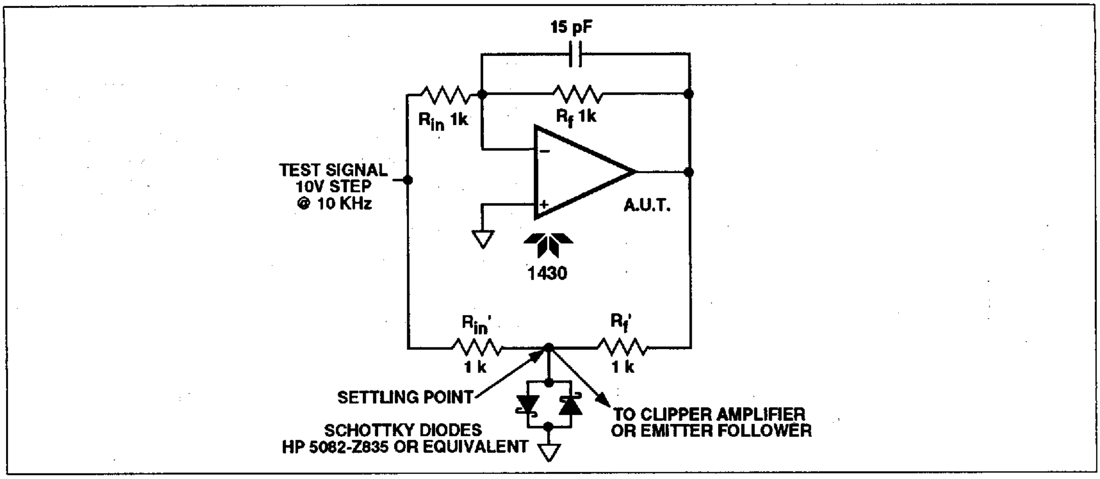

Figure 5A. Test Circuit

The test circuit (Figure 5A) is an excellent method for fast-settling time measurements. In this circuit R_{in} and R_f are matched to R_{in}' and R_f'. When the Amplifier Under Test (AUT) settles to ±0.01% of a 20V step (±2 mV) the settling point settles to ±1 mV. A FET follower with less than 1 pF input capacitance (3N128) is used in the clipper amp to buffer the settling point. The two schottky diodes acting as limiters on the settling point do not store a charge nor present much capacitive loading. Therefore, the lag due to capacitance, ≈3 pF, in combination with $R_f' = R_i' = 1\ k\Omega$ can be as low as 1.5 ns. Be sure to use an ideal square wave source for testing, since a square wave with significant ripple can unfairly cause an amplifier to look bad.

This method allows you to look directly at the true AUT output, yet avoids most drawbacks due to the output signal subtraction from the input signal.

Why not connect the 3N128 buffer directly to the summing point? Because of feedback capacitance, C_f, and the (A.U.T.) input capacitance, C_{in}. Many fast-settling amplifiers give best results when some finite amount of feedback capacitance is used. The effect of changing C_f can be seen at the settling point but not at the summing point. In addition, some good amplifiers have significant input capacitance due to "Miller capacitance" or feedforward capacitors. In this case, it is possible to see the true settling only at the settling point. You can test at the summing point if the result is the same as at the settling point; but if there is a difference measure at the settling point.

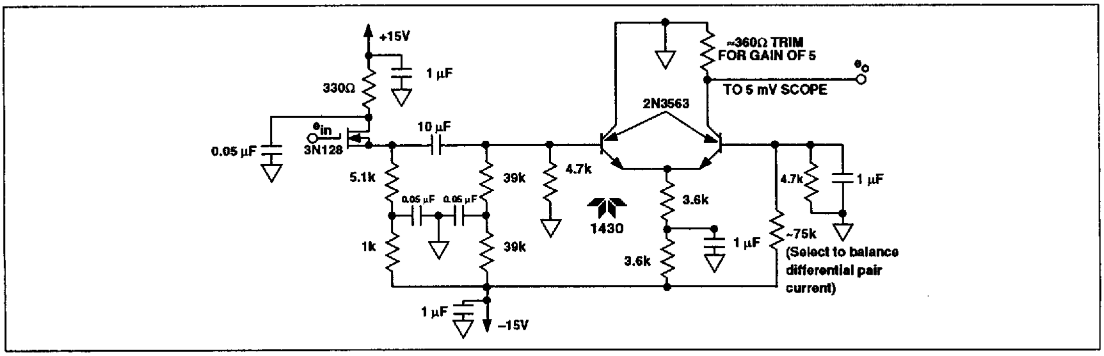

Figure 5B. Clipping Amplifier

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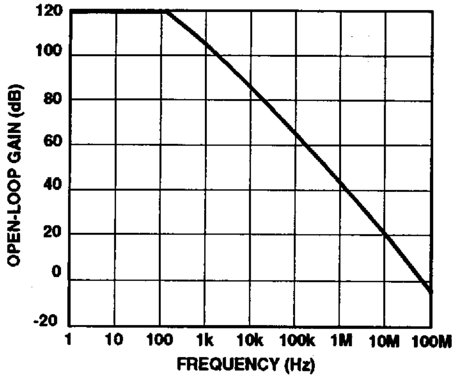
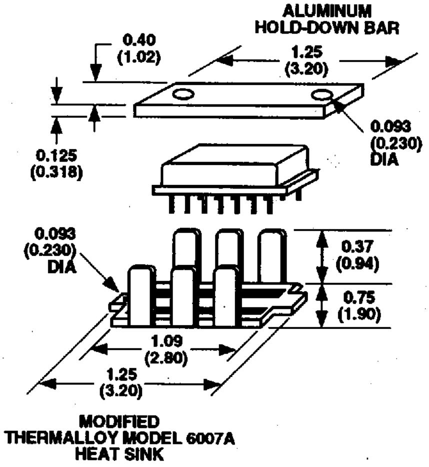


Figure 6. Open-Loop Gain vs Frequency

An amplifier is of little use in precision work if it's output for a 400ns pulse rises in 10ns, overshoots 20%, rings for 100ns, and, due to a tail does not arrive at and remain within 0.01% of the final value for another 600ns. A 1430 will be within 0.01% of final value within 200ns.

To operate the 1430 or 1430-HR from +85°C to +125°C, a 20°C per watt heat sink must be attached. A suggested device is the Thermalloy Model 6007A* modified by removing the two fins at each end and adding an aluminum "hold down bar" (Figure 7). Heat sink compound must be used between the 1430 and the heat sink.

*Thermalloy
2021 West Valley View Lane
Dallas, TX 75234



NOTE: Dimensions: in. (cm)

Figure 7. Heat Sink Assembly