HIGH-SPEED A/D CONVERTER

The Samsung KSV3208, VLSI circuit in CI (Collector Implanted) technology, consists of a high-speed flash-type 8-bit A/D converter. Also, the various auxiliary circuits such as reference voltage sources, pre-amplifier and input clamping circuits are integrated on the single chip.

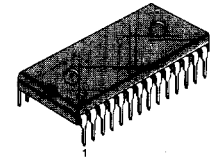
The KSV3208 has been developed for use in all applications which call for a high-speed A/D converter.

For instance, this VLSI circuit can be used to advantage to decode television signals in Pay-TV converters or for MAC converters used in direct satellite broadcasts.

Other promising applications can be seen in industrial electronics, e.g. in conjunction with signal processing.

Although the KSV3208 was initially designed as high-speed converter for the video frequency range, it can be used with equal benefits for lower frequencies, even down to zero.

28 DIP



ORDERING INFORMATION

Device	Package	Temperature Range	Diff. Nonlinearity
KSV3208CN	28 DIP	0 ~ + 70°C	± 1/2 LSB

BLOCK DIAGRAM

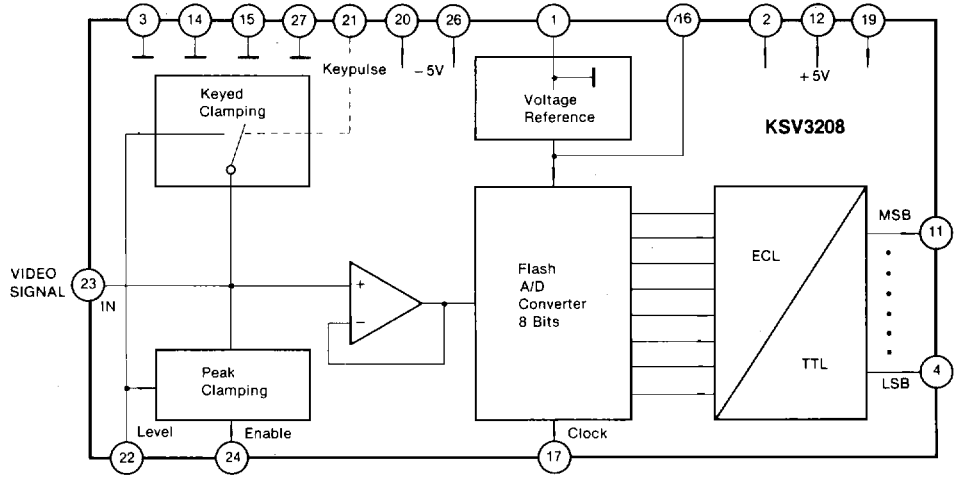


Fig. 1

The auxiliary circuits contained on-chip provide versatile potential applications needing a minimum of external components. For example, an impedance converter is connected upstream of the A/D converter to provide a high-impedance signal input in spite of the high input capacitance of the A/D converter. The reference voltage for the A/D converter is generated on-chip, but both the ground of the circuit and the reference voltage are fed to pins, so that an external filter capacitor may be connected.

Further, the input is equipped with switches which optionally provide operation with keyed clamping of peak clamping or without clamping.

All inputs and outputs are TTL compatible.

PIN DESCRIPTION

Pin No.	Description
1	GND of Reference Resistor String
2	+5V Supply of ECL Logic Part, Digital
3	GND of ECL to TTL Translator Part, Digital
4	Digital Output Bit 0 (LSB)
5	Digital Output Bit 1
6	Digital Output Bit 2
7	Digital Output Bit 3
8	Digital Output Bit 4
9	Digital Output Bit 5
10	Digital Output Bit 6
11	Digital Output Bit 7 (MSB)
12	+5V Supply of TTL Output Part, Digital
13	No Connection
14	GND of ECL Logic Part, Digital
15	GND of Input Stage, Analog
16	$+V_{REF}$, Reference Voltage Point of Resistor String
17	Clock Input
18	No Connection
19	+5V Supply of Input Stage, Analog
20	−5V Input Stage, Analog
21	Clamping Pulse Input
22	Clamping Level Input
23	Analog Signal Input
24	Peak Clamp Enable Input
25	No Connection
26	No Connection
27	GND of ECL Clock Part, Digital
28	−5V Supply of ECL Logic Part, Digital

RECOMMENDED OPERATING CIRCUIT

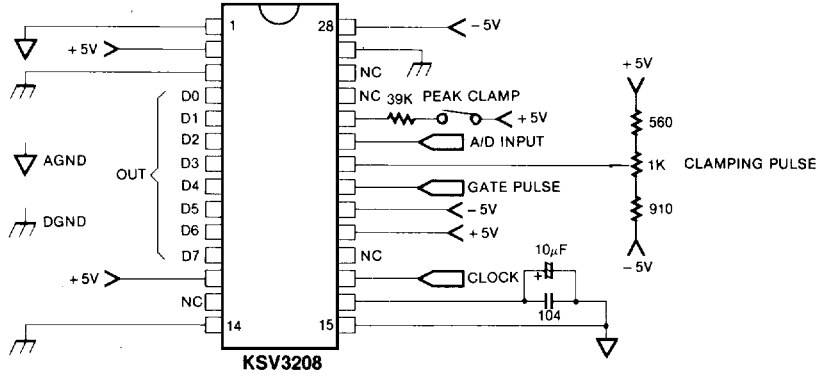


Fig. 2

ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Value	Unit
Positive Supply Voltage	V_{CC}	−0.5 to +6	V
Negative Supply Voltage	V_{EE}	−0.5 to +6	V
Digital Input Voltage	V_{DI}	−0.5 to 5.5	V
Analog Input Voltage	V_{AI}	−0.5 to 5.5	V
Digital Output Applied Voltage	V_{DO}	−0.5 to 5.5	V
Digital Output Forced Current	I_{DO}	−2.0 to 6.0	V
Single Digital Output Short Time Duration	t_{short}	1	sec
Ambient Operating Temperature	T_A	−25 to +85	°C
Storage Temperature	T_{stg}	−40 to +125	°C

Notes: 1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions.
2. Functional operation under any of these conditions in not implied.
3. Applied voltage must be current limited to a specified range.
4. Current is specified as positive when flowing into the device.

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Typ	Max	Unit
Positive Supply Voltage	V_{CC}	4.75	5	5.25	V
Negative Supply Voltage	V_{EE}	−4.75	−5	−5.25	V
Analog Input Voltage	V_{AI}	0	—	V_{ref}	V
Analog Input Frequency	f_i	—	—	$f_{ck/2}$	—
Digital Input High Voltage	V_{DIH1}	2.0	—	—	V
Digital Input Low Voltage	V_{DIL1}	0	—	0.8	V
Conversion Rate	f_{17}	0	—	20	MSPS*
Clock High Time 1 (See Fig. 3)	t_{CKH1}	15	—	—	ns
Clock Low Time 1 (See Fig. 3)	t_{CKL1}	25	—	—	ns
Clamping Level	V_{22}	−1	—	+2	V
Clamping Pulse High Time	t_{CLPH}	1	—	—	μs
Clamping Pulse Low Time	t_{CLPL}	1	—	—	μs
Digital Output High Current	I_{DOH}	—	—	−400	μA
Digital Output Low Current	I_{DOL}	—	—	3	mA
Resistance for Peak Clamping	R_{pin20}	20	39	60	KΩ
Ambient Temperature	T_a	0	—	70	°C

* MSPS (Mega Sample Per Second)

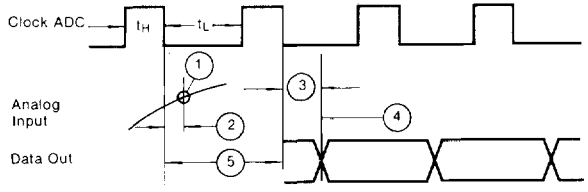
ELECTRICAL CHARACTERISTICS (V_{CC} = +5V, V_{EE} = −5V, f_{17} = 20MHz, Ta = 25°C)

Characteristics	Symbol	Condition	Min	Typ	Max	Unit
Positive Supply Current	I_{CC}	V_{CC} = Max	—	100	120	mA
Negative Supply Current	I_{EE}	V_{EE} = Max	—	−76	−100	mA
Analog Input Bias Current	I_{AIN}	V_{AI} = 2.0V, V_{EE} = Max	—	—	5	μA
Analog Input Capacitance	C_{AIN}		—	5	—	pF

ELECTRICAL CHARACTERISTICS (V_{CC} = +5V, V_{EE} = −5V, f_{17} = 20MHz, Ta = 25°C)

Characteristics	Symbol	Condition	Min	Typ	Max	Unit
Analog Input Equ. Resistance	R_{AIN}	F_{AIN} = 100KHz		100		KΩ
Total String Resistance	R_{string}	$R_{(pin\ 16-pin\ 1)}$	120	200	300	ohm
Reference Voltage	V_{ref}	$V_{pin\ 16}$	1.8	2.0	2.2	V
Clock High Current	I_{CKH1}	V_{CC} = Max, V_{CK} = 2.4V			50	μA
Clock Low Current	I_{CKL1}	V_{CC} = Max, V_{CK} = 0.4V			−800	μA
Clamping Pulse High Current	I_{CLPH}	V_{CC} = Max, V_{CLP} = 2.4V			50	μA
Clamping Pulse Low Current	I_{CLPL}	V_{CC} = Max, V_{CLP} = 0.4V			−500	μA
Digital Output High Voltage	V_{DOH}	V_{CC} = Min, I_{DOH} = 0.4mA	2.4			V
Digital Output Low Voltage	V_{DOL}	V_{CC} = Min, I_{DOL} = 3mA			0.4	V
Maximum Conversion Rate	F_{AS}	V_{CC} = Min, V_{EE} = Min	20			MSPS
Aperture Delay Time	t_{AP}	V_{CC} = Min, V_{EE} = Min	−10		0	ns
Digital Output Delay	t_D	V_{CC} = Min, V_{EE} = Min		15	20	ns
Clamp Level Sink Current	I_{22SNK}	Peak: off, Keyed: off	0		150	μA
Clamping Level Source Current	I_{22SOR}	Peak or Keyed: on	−250		0	μA
Peak Clamp Level Difference	$\triangle V_{Peak}$	$V_{22} - V_{21}$	−250	−100	0	mV
Keyed Clamp Level Difference	$\triangle V_{Keyed}$	$V_{22} - V_{21}$	−60		0	mV
Peak Clamp Charge Resistance	R_{Peak}	$\triangle V_{21}/\triangle I_{21}$, $V_{21} < V_{22}$		150		ohm
Keyed Clamp Charge Resistance	R_{Key}	$\triangle V_{21}/\triangle I_{21}$, $V_{21} < V_{22}$		150		ohm
Keyed Clamp Discharge Current	I_{Key}	$V_{21} > V_{22}$		100		μA
Static Differential Nonlinearity	SDNL	A_{IN} = 1KHz, CK = 1MHz		0.2		%
Dynamic Differential Nonlinearity	DDNL	A_{IN} = 1.02MHz, CK = 10MHz		0.3		%
		A_{IN} = 6.0018MHz, CK = 25MHz			0.6	%
Full Power Input Band Width	BW		6			MHz
Full Code Offset Error	E_{Full}	(Full Code Input) − (V_{ref})	0		+200	mV
Zero Code Offset Error	E_{Zero}	(Zero Code Input) − (V_{37})	−100		+100	mV
Signal to Noise Ratio	SNR	A_{IN} = 1.013MHz, CK = 25MHz	40			dB
(RMS Signal/RMS Noise)		A_{IN} = 3.601MHz, CK = 25MHz	36	39		dB
Differential Gain Error	DG	A_{IN} = 3.58649MHz, CK = 14.318MHz	−2		2	%
Differential Phase Error	DP	A_{IN} = 3.58649MHz, CK = 14.318MHz	−2		2	°C

TIMING DIAGRAM



① Sample
② Aperture Delay
③ Digital Output Delay
④ Data Valid (after Sample ①)
⑤ Transfer Time A/D

Fig. 3

INNER CONFIGURATION OF THE CONNECTION PINS

The following figures schematically show the circuitry at the various pins.

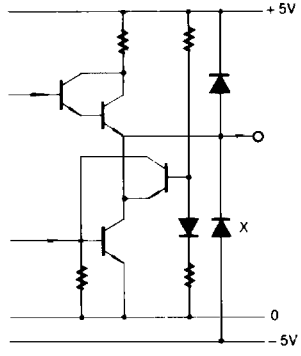


Fig. 4: Pin 4 to 11, Outputs

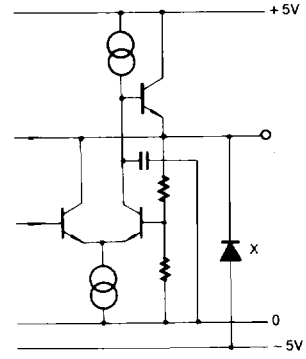


Fig. 5: Pin 16, Reference Voltage

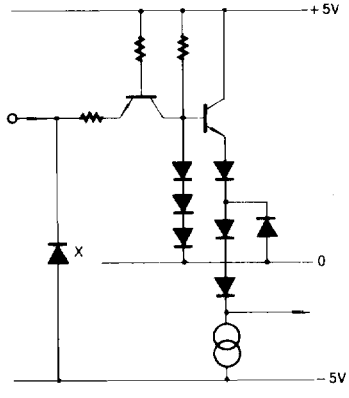


Fig. 6: Pin 17, 21 Input

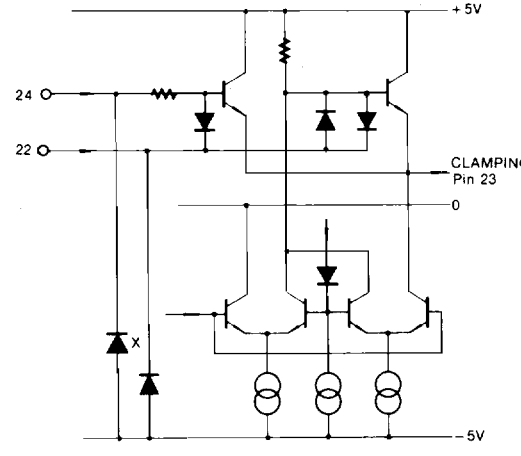


Fig. 7 Pins 22 and 24, Inputs

x: Protection Diode

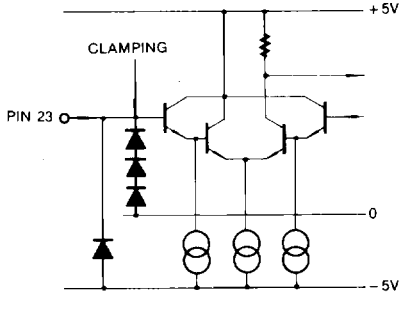


Fig. 8: Pin 23, Input

DESCRIPTION OF THE CONNECTIONS AND THE SIGNALS

Pin No.	Description
Pin 1	GND of Reference Resistor String This pin must be connected to the ground of the decoupling capacitor which is at Pin 16.
Pin 2	+5-volt Supply of ECL Logic Part, Digital This pin is the positive supply pin for the ECL logic part.
Pin 3	Digital Ground of ECL to TTL Transistor Part. This pin is the digital ground connection for the TTL output stage, where the ECL level is translated to the TTL level.
Pin 4 to Pin 11	Digital Outputs Bit 0 to Bit 7. Fig. 4 shows the diagram of those outputs which supply the digitized analog signal in a parallel 8-bit code.
Pin 12	+5-volt Supply of TTL Output Part, Digital This pin is the digital positive supply pin for the TTL output stage, where the ECL level is translated to the TTL level.
Pin 14	Digital GNP of ECL Logic Part This pin serves as the digital ground for the ECL logic part.
Pin 15	Analog GND of Input Stage This pin serves as the analog ground for the input stage; buffer amp, bandgap reference, clamp block.
Pin 16	+V_{REF}, Reference Voltage Point of Resistor String This pin, whose diagram is shown is Fig. 5, is intended for connecting a decoupling capacitor to the A/D converter's reference voltage. The other end of this capacitor is connected to Pin 1. (GND of Reference Resistor String).
Pin 17	Clock Input The diagram of this pin is shown in Fig. 6. Pin 17 is supplied with the clock of the A/D converter.
Pin 19	+5-volt Supply of Input Stage, Analog This pin is the analog positive supply pin for the input stage; bandgap reference.
Pin 20	−5-volt Supply of Input Stage, Analog This pin is the analog negative supply pin for the input stage; buffer amp, bandgap reference, clamp block.
Pin 21	Clamping Pulse Input Fig. 6 is diagram of this pin. Pin 21 must be supplied with the key pulse if keyed clamping is required.
Pin 22	Clamping Level Input Via this pin, whose diagram is shown is Fig. 7, the input of the A/D converter is supplied with the desired clamping level.
Pin 23	Analog Signal Input Fig. 8 is the diagram of this input. To Pin 23 is applied the analog signal to be converted into digital.
Pin 24	Peak Clamp Enable Input Via Pin 24, whose diagram is shown in Fig. 7, the peak clamping facilities can be used.
Pin 27	Digital GNP of ECL Clock Part This pin serves as the digital ground for the ECL clock block.
Pin 28	−5-volt Supply of ECL Logic Part, Digital This pin is the digital negative supply for the ECL logic part.

APPENDIX: APPLICATION CIRCUITS

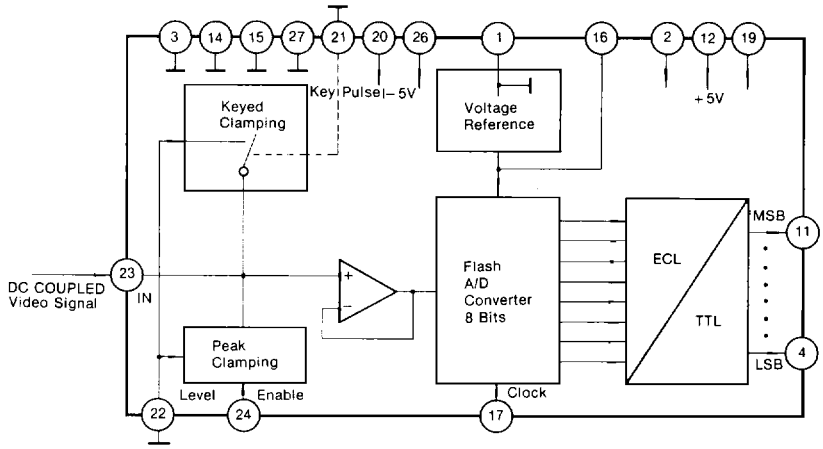


Fig. 9: Operation without clamping of the input signal
Pin 24 (peak clamping enable input) should be opened, while Pin 21 (clamping pulse input) remains at 0V. The input signal is applied to the analog input, Pin 23, without a coupling capacitor as long as it lies between 0 and + 2V

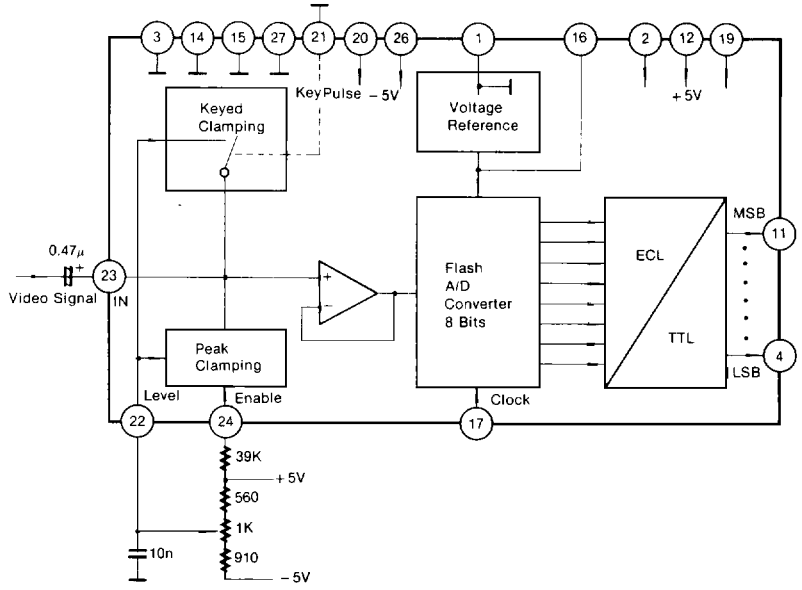


Fig. 10: Operation with peak clamping
The input signal is clamped automatically to the negative peak value. Pin 24 is connected to + 5V via a 39KΩ resistor, and Pin 22 (clamping level input) is connected, as desired, to zero or a voltage between – 1 and + 2V. The input signal is fed to Pin 23 by way of a coupling capacitor, and no key pulse (clamping pulse) is needed.

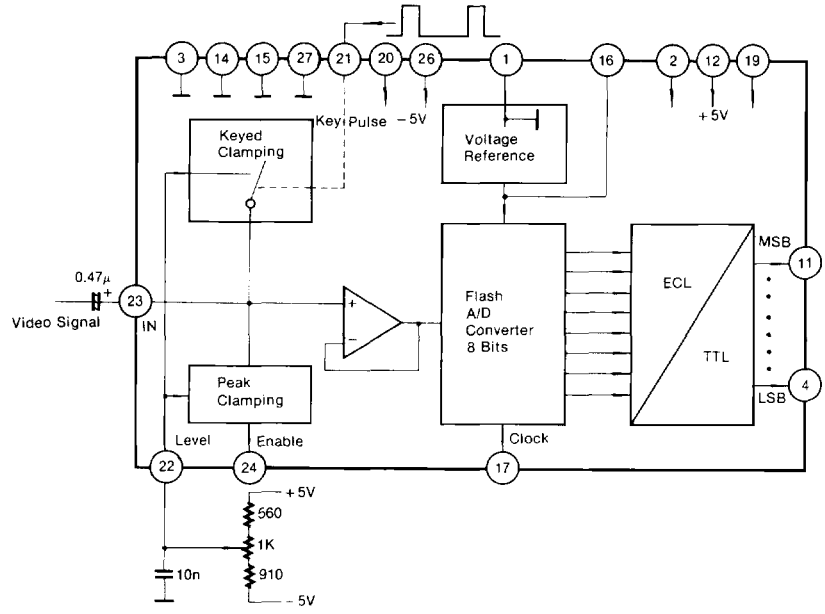


Fig. 11: Operation with keyed clamping

The input signal is applied to Pin 23 through a coupling capacitor. Pin 24 must not be connected. While the input signal is at the desired clamping level, a high-level is applied at the clamping pulse input, Pin 21. By this means the clamping switch in the KSV3208 connects the input with the clamping level at Pin 22 and recharges the coupling capacitor accordingly. The clamping level can be set to zero or, by means of an external voltage devider, to any desired value between −1 and +2V.