H1831/1833
H1831C/1833C

1800 CMOS Microprocessor Family
Static ROM

HUGHES AIRCRAFT COMPANY

MICROELECTRONICS CENTER

512 x 8 Static ROM – 1831
1024 x 8 Static ROM – 1833

DESCRIPTION

Hughes 1831 and 1833 are static CMOS Mask Programmable Read Only Memories. The 1831 and 1833 respond to a 16-bit address time multiplexed on the 8 address lines (MA 0-MA 7).

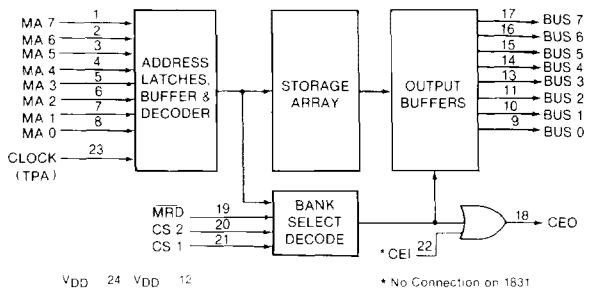
The eight most significant address lines are latched on chip by the clock input. This address may be decoded by a mask option to allow the 1831 to operate in any 512 word area, and the 1833 in any 1024 word area within the 65,536 byte memory space. In addition, three chip select signals may be decoded for simplified system interfacing. The Chip Enable Output (CEO) is activiated when the chip is selected and can be used as a disable control for the small RAM memory systems. Data is accessed from the memory by decoding the Address inputs and enabled on the data bus by the two Chip Selects (CS2 and CS1), the Memory Read ($\overline{MRD}$) and the upper address decode. The CEI signal may be used as an additional control of the ROM selected output signal, CEO, on the 1833.

The 1831 and 1833 operate over a 4-10.5 voltage range while the 1831C and 1833C operate over a 4-6.5 voltage range. The ROMs are available in a 24 lead hermetic dual-in-line ceramic package (D suffix), plastic package (P suffix), cerdip (Y suffix) or leadless chip carrier (L suffix). Devices in chip form (H suffix) are available upon request.

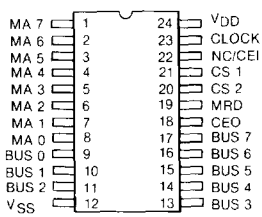
FEATURES

- Static Silicon Gate CMOS Circuitry
- Interfaces Directly with 1802A Microprocessor without Additional Components
- Access Time (1831/1833)
  830/650ns Typical at V_{DD} = 5V
  415/350ns Typical at V_{DD} = 10V
- Single Voltage Supply
- Low Quiescent and Operating Power
- Static – No Clocks Required
- Chip Select and Address Location Within 64K Memory Space, Mask Programmable

FUNCTIONAL DIAGRAM



PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range (T_A)
- Ceramic Package ..... −55 to +125°C
- Plastic Package ..... −40 to + 85°C

DC Supply-Voltage Range (V_{DD})
(All voltage values referenced to V_{SS} terminal)
- 1831/1833 ..... −0.5 to +13V
- 1831C/1833C ..... −0.5 to + 7V

Input Voltage Range ..... V_{SS} −0.3V to V_{DD} + 0.3V
Storage Temperature Range (T_{stg}) . . −65 to +150°C

NOTE: Operating the device above the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS at T_A = −55 to 125°C, V_{DD} = ±5%

CHARACTERISTICS	CONDITIONS	LIMITS								UNITS
	V_{DD} (V)	1831		1831C		1833		1833C		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Supply Voltage Range (At T_A = Full Package Temperature Range)	–	4	10.5	4	6.5	4	10.5	4	6.5	V
Recommended Input Voltage Range	–	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V
Clock Pulse Width (TPA), t_{PAW}	5	200	–	200	–	130	–	130	–	ns
	10	70	–	–	–	70	–	–	–	
Address Setup Time, t_{AS}	5	50	–	50	–	75	–	75	–	ns
	10	25	–	–	–	40	–	–	–	
Address Hold Time, t_{AH} [1]	5	150	–	150	–	100	–	100	–	ns
	10	75	–	–	–	50	–	–	–	

ELECTRICAL CHARACTERISTICS AT T_A = −55 to 125°C, V_{DD} = *nominal*

CHARACTERISTICS	CONDITIONS		1831			1831C			1833			1833C			UNITS
	V_O (V)	V_{DD} (V)	Min.	Typ.*	Max.	Min.	Typ.*	Max.	Min.	Typ.*	Max.	Min.	Typ.*	Max.	
STATIC															
Quiescent Device Current, I_L [2]	–	5	–	40	80	–	170	400	–	50	50	–	200	200	µA
	–	10	–	170	400	–	–	–	–	200	200	–	–	–	
Output Drive Current,	0.4	5	.47	.67	–	0.55	–	–	0.8	–	–	0.8	–	–	mA
N-Channel (Sink), I_{DN}	0.5	10	1.1	1.6	–	–	–	–	1.8	–	–	–	–	–	
P-Channel (Source), I_{DP}	4.6	5	−.3	−.43	–	−0.35	–	–	−0.8	–	–	−0.8	–	–	
	9.5	10	−.55	−.8	–	–	–	–	−1.8	–	–	–	–	–	
Output Voltage	–	5	–	0	0.5	–	0	0.5	–	0	0.5	–	0	0.5	V
Low Level, V_{OL} [1]	–	10	–	0	0.5	–	–	–	–	0	0.5	–	–	–	
Output Voltage	–	5	4.9	5	–	4.9	5	–	4.9	5	–	4.9	5	–	V
High Level, V_{OH} [1]	–	10	9.9	10	–	–	–	–	9.9	10	–	–	–	–	
Input Leakage Current,	–	5	–	±1	±2	–	–	±2	–	–	±1	–	–	±1	µA
I_{IL}, I_{IH} [2]	–	10	–	±1	±2	–	–	–	–	–	±1	–	–	–	
3-State Output Leakage	0,5	5	–	±1	±2	–	–	±2	–	–	±1	–	–	±1	µA
Current, I_{OUT} [2]	0,10	10	–	±1	±2	–	–	–	–	–	±1	–	–	–	

* Typical values are for T_A = 25°C and nominal V_{DD}

Note 1: Design assured but not tested.
Note 2: Parameters guaranteed by other tests at −55 C.

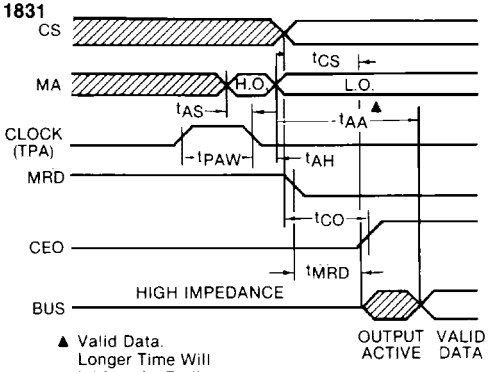
ELECTRICAL CHARACTERISTICS, Cont.

CHARACTERISTICS	CONDITIONS		1831			1831C			1833			1833C			UNITS
	V_O (V)	V_{DD} (V)	Min.	Typ.*	Max.	Min.	Typ.*	Max.	Min.	Typ.*	Max.	Min.	Typ.*	Max.	
DYNAMIC T_A = −55° to 125°C, V_{DD} = ±5%, C_L = 50pF, R_L > 10MΩ															
Access Time From Address Change, t_{AA}	–	5	–	830	1100	–	830	1100	–	650	875	–	650	875	ns
	–	10	–	415	550	–	–	–	–	350	475	–	–	–	
Access Time From Chip Select, t_{ACS}	–	5	–	660	880	–	660	880	–	600	810	–	600	810	ns
	–	10	–	250	330	–	–	–	–	330	400	–	–	–	
CEO From Address Change, t_{CA} [3]	–	5	–	500	600	–	500	600	–	125	180	–	125	180	ns
	–	10	–	200	250	–	–	–	–	85	115	–	–	–	
Bus Contention Delay, t_D [3]	–	5	–	200	350	–	200	350	–	220	270	–	220	270	ns
	–	10	–	100	150	–	–	–	–	130	150	–	–	–	
Daisy Chain Delay, t_{IO}	–	5	–	–	–	–	–	–	–	200	270	–	200	270	ns
	–	10	–	–	–	–	–	–	–	125	150	–	–	–	
Read Delay, to Output Valid t_{MRD}	–	5	–	515	650	–	515	650	–	550	740	–	550	740	ns
	–	10	–	175	220	–	–	–	–	320	430	–	–	–	
Chip Select Delay, t_{CS} [3]	–	5	–	600	750	–	600	750	–	250	320	–	250	320	ns
	–	10	–	200	300	–	–	–	–	125	180	–	–	–	
Chip Enable Output Delay Time From CS, t_{CO} [3]	–	5	–	400	500	–	400	500	–	200	250	–	200	250	ns
	–	10	–	200	250	–	–	–	–	100	150	–	–	–	

* Typical values are for T_A = 25°C and nominal V_{DD}

TIMING DIAGRAMS

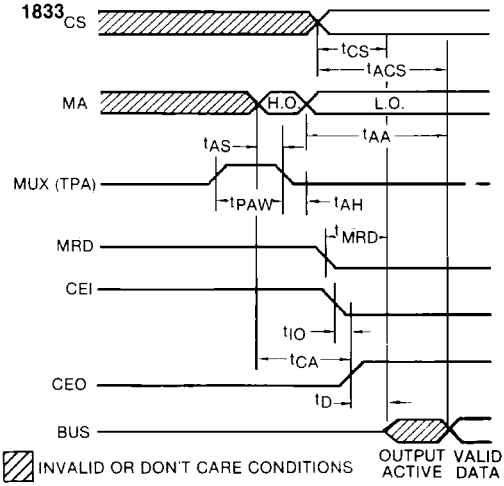
1831



▲ Valid Data. Longer Time Will Initiate An Earlier But Invalid Output

H.O. = High Order Address
L.O. = Low Order Address

1833



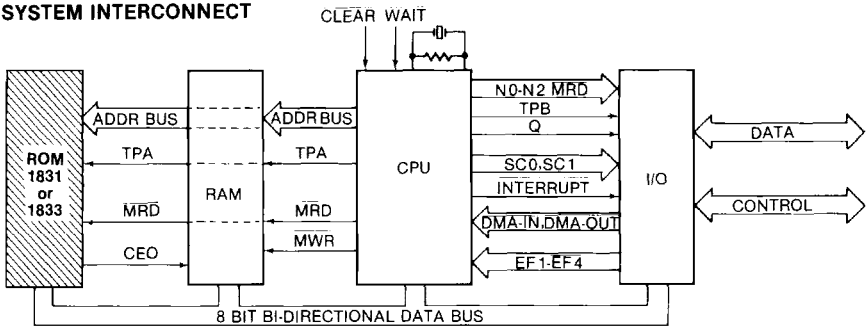
INVALID OR DON'T CARE CONDITIONS

The dynamic characteristic table and the above timing diagrams represent maximum performance capability of the 1831/1833. When used in direct system interface with the 1802A microprocessor, the timing relation will be determined by the clock frequency and timing signal generation of the microprocessor. In the latter case the following general timing conditions hold: $t_{AH} = 0.5t_C$

$t_{PAW} = 1.0t_C$

$\overline{MRD}$ occurs one clock period (t_C) earlier than address bus MA0 – MA7.
t_C = 1/1802A clock frequency.

SYSTEM INTERCONNECT



SIGNAL DESCRIPTION

MA0 – MA7: High order byte of a 16-bit memory address appears on the memory address lines (MA0–MA7) first. Those bits required by the memory system are strobed into internal address latches by Clock (TPA) input. The low order byte of 16-bit address appears on the address lines after the termination of TPA.

BUS0 – BUS7: These eight bi-directional three state data lines form a common bus with the 1802A microprocessor.

CLOCK (TPA): A timing signal from 1802A microprocessor (trailing edge of TPA) is used to latch the high order byte of the 16-bit memory address. The polarity of TPA is user mask programmable.

CS1, CS2, MRD: Chip Select and Memory Read (output enable) signals. The polarity of the chip select signals are user mask programmable.

CEO, CEI: Chip Enable Output signal (CEO) is high when either the chip is selected or CEI is high (1833 only). CEO and CEI can be connected in daisy chain operation between several ROMs to control selection of RAM chips in a microprocessor system without additional components. The polarity of CEI is user mask programmable in the 1833.

ORDERING INFORMATION:

Contact Hughes for prices and other information relating to ROMs. ROM order forms and instructions concerning means of data conveyance are available from Hughes Microelectronics Center or Hughes' Representatives.

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