Dense-Pac Microsystems, Inc.

DPS128X16A3

CERAMIC 128K X 16 CMOS SRAM MODULE

PRELIMINARY

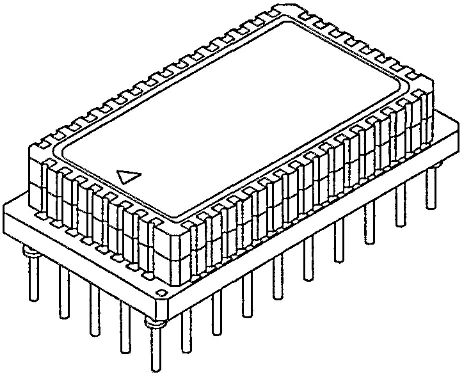
DESCRIPTION:

The DPS128X16A3 "DENSE-STACK" module is a revolutionary new memory subsystem using Dense-Pac Microsystems' ceramic Stackable Leadless Chip Carriers (SLCC) mounted on a *co-fired ceramic substrate*. The module packs 2-Megabits of low-power CMOS static RAM in an area of just over one half square inch (0.540 in^2), while maintaining a height of only 0.280 inches.

The DPS128X16A3 contains two individual 128K x 8 SRAMs, packaged in their own hermetically sealed SLCC making the module suitable for commercial, industrial and military applications.

The module can be organized as 128K x 16 or 256K x 8 and features extremely low standby power making it suitable for battery backup.

By using SLCCs, the "Dense-Stack" family of modules offers a higher board density of memory than available with conventional through-hole, surface mount or hybrid techniques.

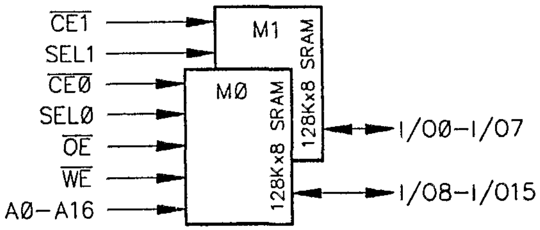


FEATURES:

- Organizations Available: 128K x 16, 256K x 8
- Access Times: 70*, 85, 100, 120, 150ns
- Fully Static Operation - No clock or refresh required
- Single +5V Power Supply, ±10% Tolerance
- TTL Compatible
- Common Data Inputs and Outputs
- Low Data Retention Voltage: 2.0V min.
- 50-Pin PGA Package

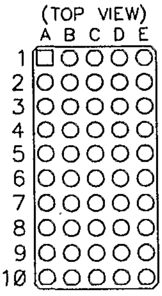
* Commercial only.

FUNCTIONAL BLOCK DIAGRAM



PIN-OUT DIAGRAM

	A	B	C	D	E
1	N.C.	N.C.	N.C.	N.C.	$\overline{\text{CE1}}$
2	VSS	N.C.	N.C.	SEL1	VDD
3	N.C.	A16	$\overline{\text{WE}}$	SEL0	A15
4	A14	A12	A7	A8	A13
5	A6	A5	$\overline{\text{OE}}$	A11	A9
6	A4	A3	A2	$\overline{\text{CE0}}$	A10
7	A1	A0	I/O5	I/O4	I/O3
8	I/O2	I/O1	I/O0	I/O7	I/O6
9	VSS	I/O9	I/O11	I/O13	VDD
10	I/O8	I/O10	I/O12	I/O14	I/O15



PIN NAMES

A0 - A16	Address Inputs
I/O0 - I/O15	Data Input/Output
$\overline{\text{CE0}}$, $\overline{\text{CE1}}$	Low Chip Enables
SEL0, SEL1	High Chip Enables
$\overline{\text{WE}}$	Write Enable
$\overline{\text{OE}}$	Output Enable
VDD	Power (+5V)
Vss	Ground
N.C.	No Connect

PRELIMINARY

RECOMMENDED OPERATING RANGE[3]					
Symbol	Characteristic	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input HIGH Voltage	2.2		V_{DD}+0.3	V
V_{IL}	Input LOW Voltage	-0.5[2]		0.8	V
T_A	Operating Temp.	-55	+25	+125	°C

DC OUTPUT CHARACTERISTICS					
Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{OH}	HIGH Voltage	I_{OH}= -1.0mA	2.4	-	V
V_{OL}	LOW Voltage	I_{OL}=2.1mA	-	0.4	V

ABSOLUTE MAXIMUM RATINGS[3]			
Symbol	Parameter	Value	Unit
T_{STC}	Storage Temperature	-65 to +150	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
V_{DD}	Supply Voltage [1]	-0.5 to +7.0	V
$V_{I/O}$	Input/Output Voltage [1]	-0.5 to V_{DD} +0.5	V

TRUTH TABLE						
Mode	SEL	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O Pin	Supply Current
Not Selected	L	X	X	X	HIGH-Z	Standby
Not Selected	X	H	X	X	HIGH-Z	Standby
D_{OUT} Disable	H	L	H	H	HIGH-Z	Active
Read	H	L	H	L	D_{OUT}	Active
Write	H	L	L	X	D_{IN}	Active

H=HIGH-Z L=LOW-Z X=Don't Care

CAPACITANCE [4]: T_A = 25°C, F = 1.0MHz				
Symbol	Parameter	Max.	Unit	Condition
C_{ADR}	Address Input	25	pF	V_{IN}^2 = 0V
C_{CE}	Chip Enable	16		
C_{SEL}	Active High Chip Select	16		
C_{WE}	Write Enable	25		
C_{OE}	Output Enable	25		
$C_{I/O}$	Data Input/Output	20		

AC TEST CONDITIONS	
Input Pulse Levels	0V to 3.0V
Input Pulse Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V

OUTPUT LOAD		
Load	C_L	Parameters Measured
1	100 pF	except t_{LZ1}, t_{LZ2}, t_{HZ1}, t_{HZ2}, t_{OHZ}, t_{OLZ}, t_{OW}, and t_{WHZ}
2	5 pF	t_{LZ1}, t_{LZ2}, t_{HZ1}, t_{HZ2}, t_{OHZ}, t_{OLZ}, t_{OW}, and t_{WHZ}

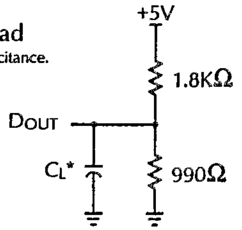


Figure 1. Output Load

* Including Probe and Jig Capacitance.

DC OPERATING CHARACTERISTICS: Over operating ranges												
Symbol	Characteristics	Test Conditions		TYP. (†)	C		I		M		Unit
					Min.	Max.	Min.	Max.	Min.	Max.	
I_{IN}	Input Leakage Current	V_{IN} = 0V to V_{DD}		-	-4	+4	-4	+4	-4	+4	µA
I_{OUT}	Output Leakage Current	$V_{I/O}$ = 0V to V_{DD}, $\overline{CE}$ or $\overline{OE}$ = V_{IH}, or $\overline{WE}$ = V_{IL}		-	-2	+2	-2	+2	-2	+2	µA
I_{CC1}	Active Supply Current	$\overline{CE}$ = V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT} = 0mA	X8	15		40		50		55	mA
			X16	30		70		90		100	
I_{CC2}	Operating Supply Current	Cycle = min., Duty = 100% I_{OUT} = 0mA	X8	45		75		80		85	mA
			X16	90		140		150		160	
I_{SB1}	Full Standby Supply Current (CMOS)	V_{IN} ≥ V_{DD} -0.2V or V_{IN} ≤ V_{SS} +0.2V		4		200		400		1000	µA
I_{SB2}	Standby Current (TTL)	$\overline{CE}$ = V_{IH}		2		6		6		6	mA
I_{DR3}	Data Retention Supply Current (3V)	V_{DR} = 3V, $\overline{CE}$ ≥ V_{DR} -0.2V, or SEL ≤ 0.2V		2		100		200		800	µA
I_{DR2}	Data Retention Supply Current (2V)	V_{DR} = 2V, $\overline{CE}$ ≥ V_{DR} -0.2V, SEL ≥ V_{DR} -0.2V or SEL ≤ 0.2V		2		90		170		700	µA
V_{OL}	Output Low Voltage	I_{OUT} = 2.1mA		-		0.4		0.4		0.4	V
V_{OH}	Output High Voltage	I_{OUT} = -1.0mA		-	2.4		2.4		2.4		V

† Typical measurements made at +25°C, Cycle = min., V_{DD} = 5.0V.

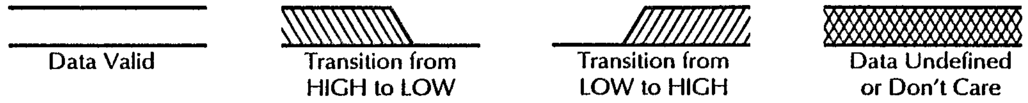
AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE: Over operating ranges													
No.	Symbol	Parameter	-70		-85		-10		-12		-15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{RC}	Read Cycle Time	70		85		100		120		150		ns
2	t_{AA}	Address Access Time		70		85		100		120		150	ns
3	t_{CO1}	$\overline{CE}$ to Output Valid		70		85		100		120		150	ns
4	t_{CO2}	SEL to Output Valid		70		85		100		120		150	ns
5	t_{OE}	Output Enable to Output Valid		40		45		50		60		70	ns
6	t_{LZ1}	$\overline{CE}$ to Output in LOW-Z [4, 5]	5		5		10		10		10		ns
7	t_{LZ2}	SEL to Output in LOW-Z [4, 5]	5		5		10		10		10		ns
8	t_{OLZ}	Output Enable to Output in LOW-Z [4, 5]	0		0		0		0		0		ns
9	t_{HZ1}	$\overline{CE}$ to Output in HIGH-Z [4, 5]		30		30		35		45		50	ns
10	t_{HZ2}	SEL to Output in HIGH-Z [4, 5]		30		30		35		45		50	ns
11	t_{OHZ}	Output Enable to Output in HIGH-Z [4, 5]		30		30		35		45		50	ns
12	t_{OH}	Output Hold from Address Change	10		10		10		10		10		ns

AC OPERATING CONDITIONS AND CHARACTERISTICS - WRITE CYCLE [6,7]: Over operating ranges													
No.	Symbol	Parameter	-70		-85		-10		-12		-15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
13	t_{WC}	Write Cycle Time	70		85		100		120		150		ns
14	t_{AW}	Address Valid to End of Write	65		75		90		100		120		ns
15	t_{CW}	Chip Enable to End of Write	65		75		90		100		120		ns
16	t_{AS}	Address Set-up Time***	0		0		0		0		0		ns
17	t_{WP}	Write Pulse Width	55		65		75		85		90		ns
18	t_{WR}	Write Recovery Time	10		10		10		15		15		ns
19	t_{WHZ}	Write Enable to Output in HIGH-Z [4, 5]		30		30		35		40		45	ns
20	t_{DW}	Data to Write Time Overlap	35		35		40		50		60		ns
21	t_{DH}	Data Hold from Write Time	0		0		0		0		0		ns
22	t_{OW}	Output Active from End of Write	5		5		5		5		5		ns

*** Valid for both Read and Write Cycles.

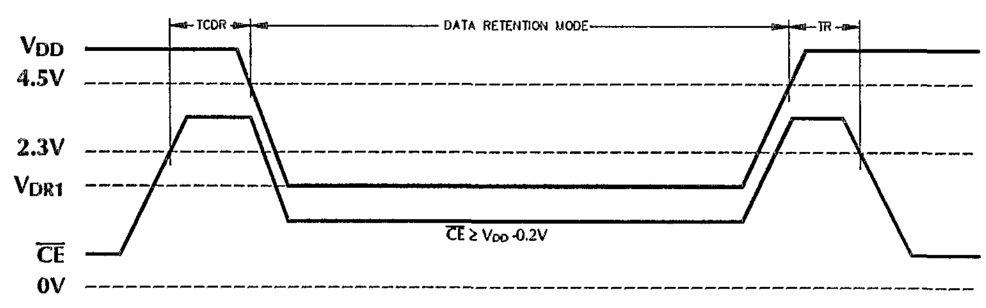
Data Retention AC Characteristics						
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DR}	V_{DD} for Data Retention	$\overline{CE} \geq V_{DD}$ -0.2V, SEL $\geq V_{DD}$ -0.2V or SEL $\leq V_{DD}$ 0.2V	2.0	-	-	V
t_{CDR}	Chip Disable to Data Retention Time	See Data Retention Waveform	0	-	-	ns
t_R	Operation Recovery Time	See Data Retention Waveform	5	-	-	ms

WAVEFORM KEY

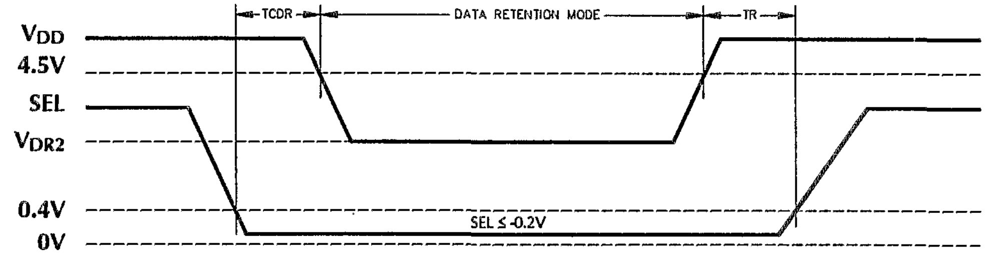


PRELIMINARY

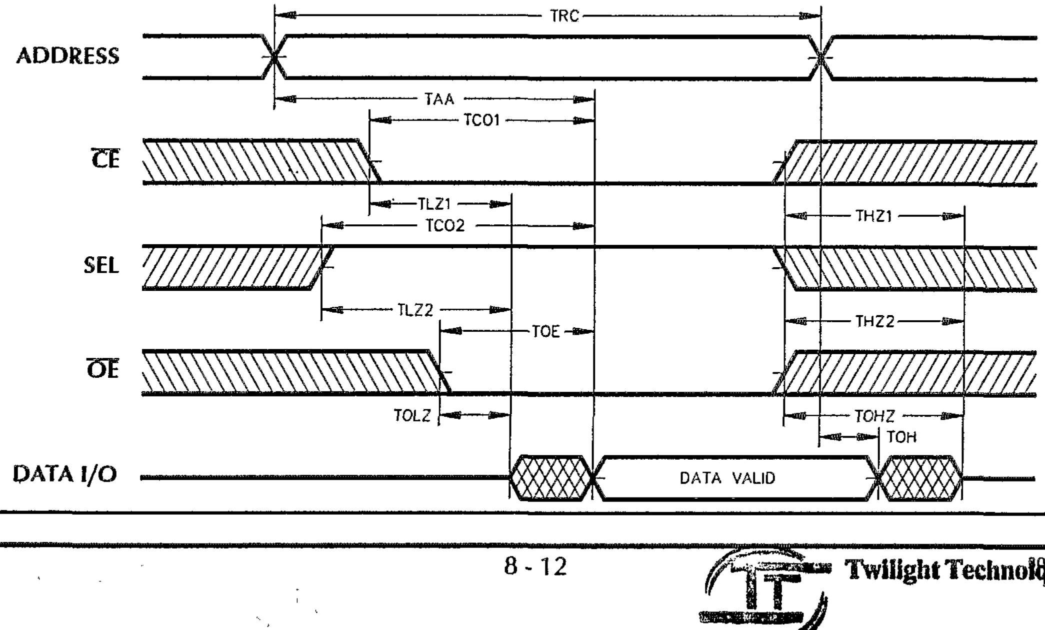
DATA RETENTION WAVEFORM: $\overline{CE}$ Controlled.



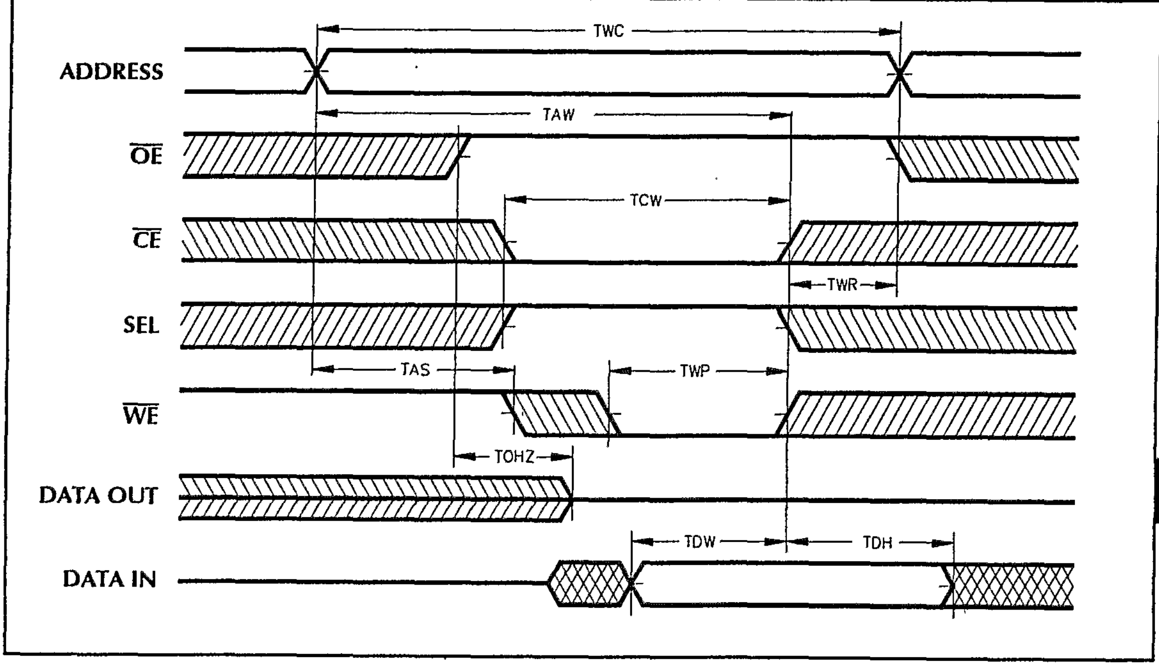
DATA RETENTION WAVEFORM: [8] SEL Controlled.



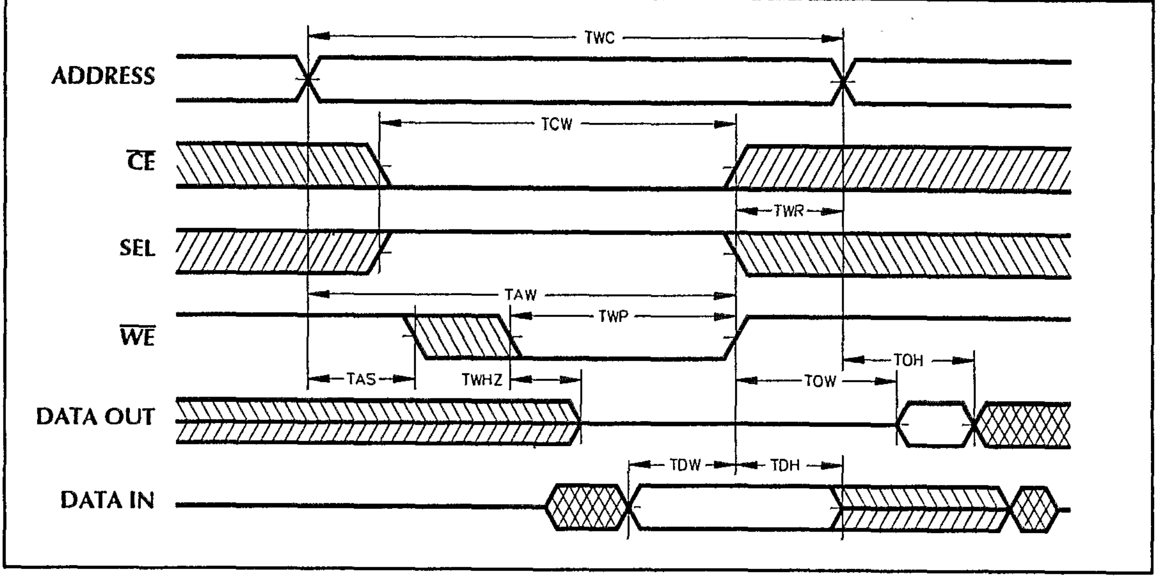
READ CYCLE



WRITE CYCLE 1: $\overline{\text{WE}}$ Controlled. $\overline{\text{OE}}$ Clocked.



WRITE CYCLE 2: $\overline{\text{CE}}$ Controlled. $\overline{\text{OE}}$ is LOW.



PRELIMINARY

ORDERING INFORMATION

DP	S	128	X	16	A3	– XX	X
PREFIX	TYPE	MEMORY DEPTH	DESIG	MEMORY WIDTH	PACKAGE	SPEED	GRADE

GRADE:

C	COMMERCIAL	0°C to +70°C
I	INDUSTRIAL	–40°C to +85°C
M	MILITARY	–55°C to +125°C
B	MIL–PROCESSED	–55°C to +125°C

SPEED:

70	70ns (COMMERCIAL ONLY)
85	85ns
10	100ns
12	120ns
15	150ns

PACKAGE: CERAMIC PIN GRID ARRAY (PGA)/(3–D) DENSE–STACK

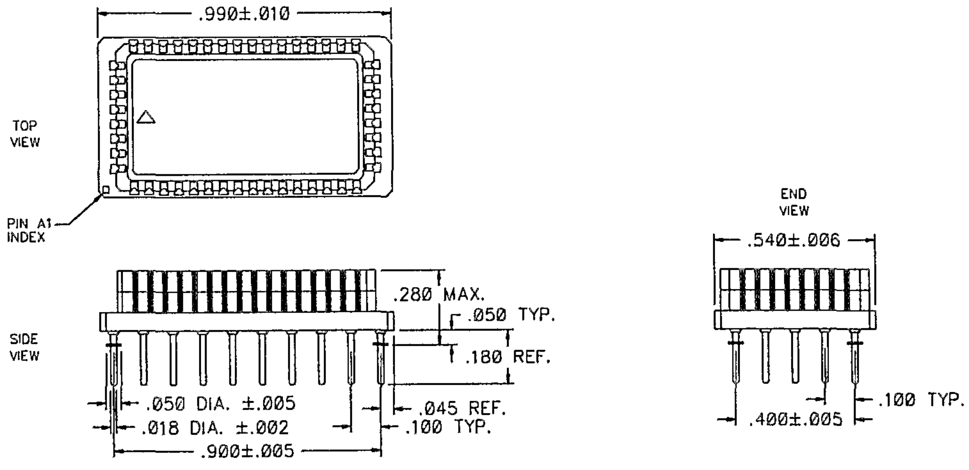
DESIG: MODULE WITHOUT SUPPORT LOGIC

TYPE: CMOS SRAM DEVICES

NOTES:

1. All voltages are with respect to V_{SS}.
2. -2.0V min. for pulse width less than 20ns (V_{IL} min. = -0.5V at DC level).
3. Stresses greater than those under **ABSOLUTE MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
4. This parameter is guaranteed and not 100% tested.
5. Transition is measured at the point of ±500mV from steady state voltage.
6. When $\overline{OE}$ and $\overline{CE}$ are LOW and $\overline{WE}$ is HIGH, I/O pins are in the output state,and input signals of opposite phase to the outputs must not be applied.
7. The outputs are in a high impedance state when $\overline{WE}$ is LOW.
8. SEL controls address buffer, $\overline{WE}$ buffer, $\overline{CE}$ buffer and $\overline{OE}$ buffer and D_{IN} buffer. If SEL controls Data Retention Mode, V_{IN} levels (Address, $\overline{WE}$, $\overline{OE}$, $\overline{CE}$, I/O) can be in the high impedance state. If $\overline{CE}$ controls Data Retention Mode, SEL must be $SEL \geq V_{DD}$ -0.2V or $0V \leq SEL \leq 0.2V$. The other input levels (Address, $\overline{WE}$, $\overline{OE}$, I/O) can be in the High Impedance State.

MECHANICAL DRAWING



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