# 128K X76F128 16Kx8+64x8

## Secure SerialFlash

### FEATURES

- **64-bit Password Security**
  - **—Five 64-bit Passwords for Read, Program and Reset**
- **16384 Byte+64 Byte Password Protected Arrays**
  - **—Seperate Read Passwords**
  - **—Seperate Write Passwords**
  - **—Reset Password**
- **Programmable Passwords**
- **Retry Counter Register**
  - **—Allows 8 tries before clearing of both arrays**
  - **—Password Protected Reset**
- **32-bit Response to Reset (RST Input)**
- **64 byte Sector Program**
- **400kHz Clock Rate**
- **2 wire Serial Interface**
- **Low Power CMOS**
  - **—2.7 to 5.5V operation**
  - **—Standby current Less than 1µA**
  - **—Active current less than 3 mA**
- **High Reliability Endurance:**
  - **—100,000 Write Cycles**
- **Data Retention: 100 years**
- **Available in:**
  - **—SmartCard Module**
  - **—TQFP Package**

### DESCRIPTION

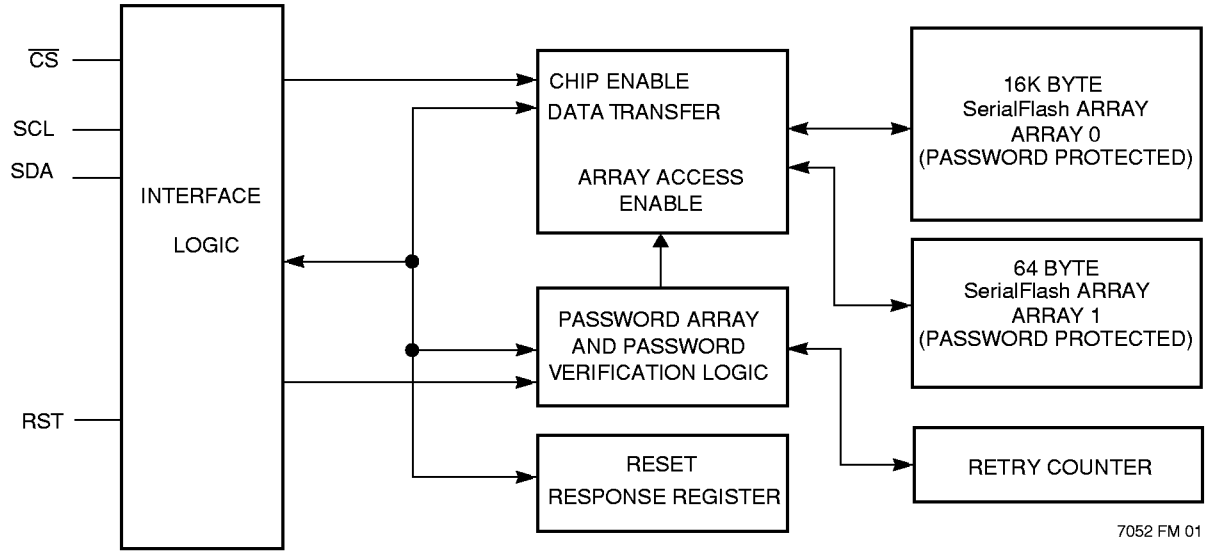
The X76F128 is a Password Access Security Supervisor, containing one 131072-bit Secure SerialFlash array and one 512-bit Secure SerialFlash array. Access to each memory array is controlled by two 64-bit passwords. These passwords protect read and write operations of the memory array. A separate RESET password is used to reset the passwords and clear the memory arrays in the event the read and write passwords are lost.

The X76F128 features a serial interface and software protocol allowing operation on a popular two wire bus. The bus signals are a clock Input (SCL) and a bidirectional data input and output (SDA). Access to the device is controlled through a chip select ($\overline{CS}$) input, allowing any number of devices to share the same bus.

The X76F128 also features a synchronous response to reset providing an automatic output of a hard-wired 32-bit data stream conforming to the industry standard for memory cards.

The X76F128 utilizes Xicor's proprietary Direct Write™ cell, providing a minimum endurance of 100,000 cycles and a minimum data retention of 100 years.

## Functional Diagram



## PIN DESCRIPTIONS

### Serial Clock (SCL)

The SCL input is used to clock all data into and out of the device.

### Serial Data (SDA)

SDA is a true three state serial data input/output pin. During a read cycle, data is shifted out on this pin. During a write cycle, data is shifted in on this pin. In all other cases, this pin is in a high impedance state.

### Chip Enable ($\overline{CS}$)

When $\overline{CS}$ is high, the X76F128 is deselected and the SDA pin is at high impedance and unless an internal write operation is underway, the X76F128 will be in standby mode. $\overline{CS}$ low enables the X76F128, placing it in the active mode.

### Reset (RST)

RST is a device reset pin. When RST is pulsed high while $\overline{CS}$ is low the X76F128 will output 32 bits of fixed data which conforms to the standard for "synchronous response to reset". $\overline{CS}$ must remain LOW and the part must not be in a write cycle for the response to reset to occur. See Figure 11. If at any time during the response to reset $\overline{CS}$ goes HIGH, the response to reset will be aborted and the part will return to the standby state. The response to reset is "mask programmable" only!

## DEVICE OPERATION

There are two primary modes of operation for the X76F128; Protected READ and protected WRITE. Protected operations must be performed with one of four 8-byte passwords.

The basic method of communication for the device is established by first enabling the device ($\overline{CS}$ LOW), generating a start condition, then transmitting a command, followed by the correct password. All parts will be shipped from the factory with all passwords equal to '0'. The user must perform ACK Polling to determine the validity of the password, before starting a data transfer (see Acknowledge Polling.) Only after the correct password is accepted and a ACK polling has been performed, can the data transfer occur.

To ensure the correct communication, RST must remain LOW under all conditions except when running a "Response to Reset sequence".

Data is transferred in 8-bit segments, with each transfer being followed by an ACK, generated by the receiving device.

If the X76F128 is in a nonvolatile write cycle a "no ACK" (SDA=High) response will be issued in response to loading of the command byte. If a stop is issued prior to the nonvolatile write cycle the write operation will be terminated and the part will reset and enter into a standby mode.

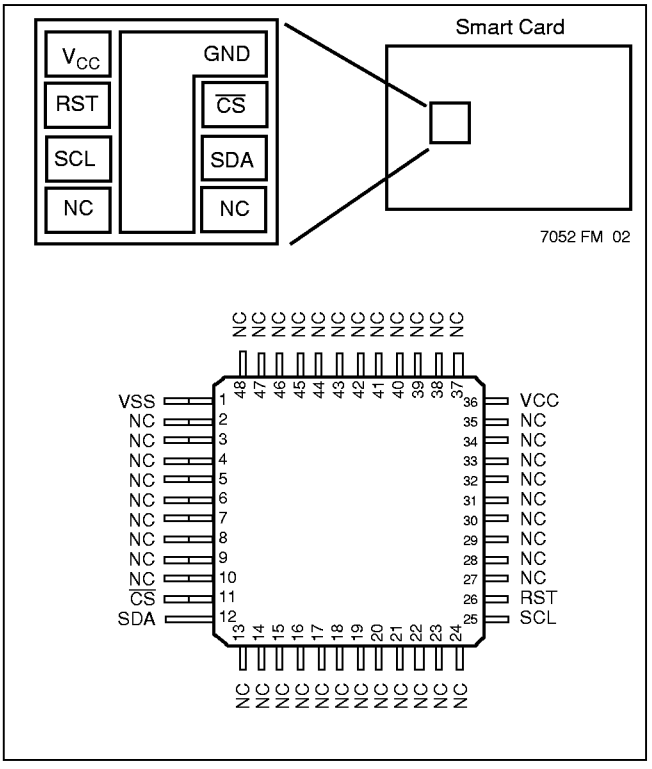
The basic sequence is illustrated in Figure 1.

## PIN NAMES

| Symbol | Description |
|---|---|
| $\overline{CS}$ | Chip Select Input |
| SDA | Serial Data Input/Output |
| SCL | Serial Clock Input |
| RST | Reset Input |
| Vcc | Supply Voltage |
| Vss | Ground |
| NC | No Connect |

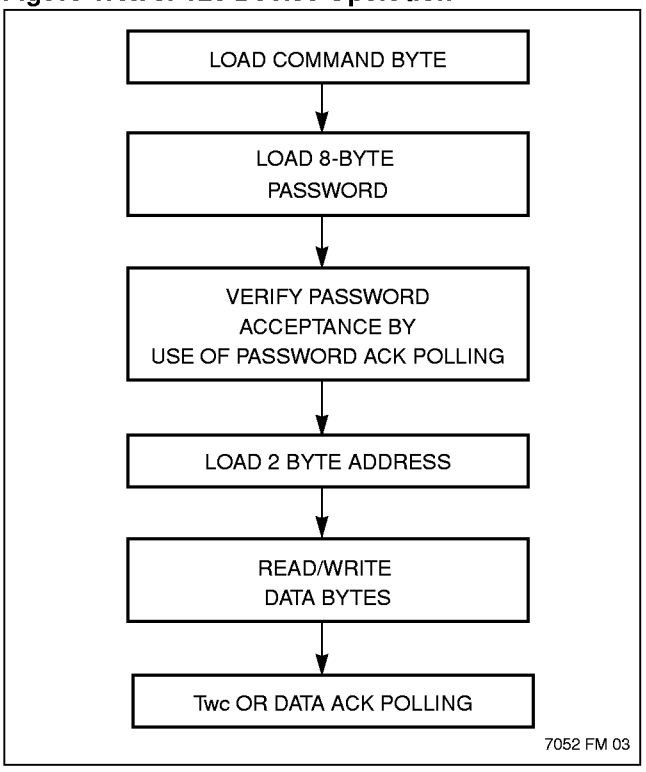
7052 FM T01

## PIN CONFIGURATION




After each transaction is completed, the X76F128 will reset and enter into a standby mode. This will also be the response if an unsuccessful attempt is made to access a protected array.

**Figure 1. X76F128 Device Operation**




### Retry Counter

The X76F128 contains a retry counter. The retry counter allows 8 accesses with an invalid password before any action is taken. The counter will increment with any combination of incorrect passwords. If the retry counter overflows, all memory areas are cleared and the device is locked by preventing any read or write array password matches. The passwords are unaffected. If a correct password is received prior to retry counter overflow, the retry counter is reset and access is granted. In order to reset the operation of a locked up device, a special reset command must be used with a RESET PASSWORD.

### Device Protocol

The X76F128 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as a receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the X76F128 will be considered a slave in all applications.

### Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to Figure 2 and Figure 3.

### Start Condition

All commands are preceeded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The X76F128 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition is met.

A start may be issued to terminate the input of a control byte or the input data to be written. This will reset the device and leave it ready to begin a new read or write command. Because of the push/pull output, a start cannot be generated while the part is outputting data. Starts are inhibited while a write is in progress.

### Stop Condition

All communications must be terminated by a stop condition. The stop condition is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used to reset the device during a command or data input sequence and will leave the device in the standby power mode. As with starts, stops are inhibited when outputting data and while a write is in progress.

### Acknowledge

Acknowledge is a software convention used to indicate successful data transfer. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data.

The X76F128 will respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write condition have been selected, the X76F128 will respond with an acknowledge after the receipt of each subsequent eight-bit word.

### RESET DEVICE Command

The RESET DEVICE command is used to clear the retry counter and reactivate the device. When the RESET DEVICE command is used prior to the retry counter overflow, the retry counter is reset and no arrays or passwords are affected. If the retry counter has overflowed, all memory areas are cleared and all commands are blocked and the retry counter is disabled. Issuing a valid RESET DEVICE command (with reset password) to the device resets and re-enables the retry counter and re-enables the other commands. Again, the passwords are not affected.

### RESET PASSWORD Command

A RESET PASSWORD command will clear both arrays and set all passwords to all zero.