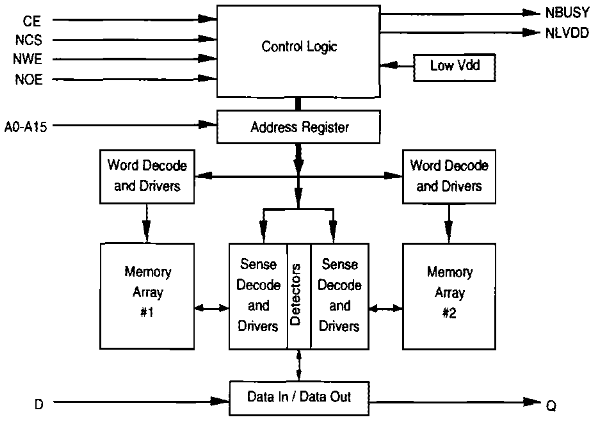
NON-VOLATILE RAM *Advance Information*

64K x 1 NON-VOLATILE RAM-MAGNETORESISTIVE HC7464

FEATURES

- Non-volatile and NDRO (Non-destructive read out)
- Unlimited read/write (>1E15 cycles)
- Fabricated with bulk RICMOS™ 0.8 µm Process
- Strategic Radiation Hardened
- Total Dose Hard
- Neutron Hard
- Dynamic and Static Transient Upset Hard
- Immune to Single Event Upset (SEU)
- Dose Rate Survivable
- 1 µs Read Cycle Time
- 250 ns Write Cycle Time
- Power off data retention
- Synchronous Operation
- CMOS Input Levels (TTL Optional)
- Tri-State Outputs
- High Output Drive
- Full Military Temperature Operation (-55°C to 125°C)
- Single 5 V ± 10% Power Supply
- Power is 500mW Active, 10mW Standby

FUNCTIONAL DIAGRAM

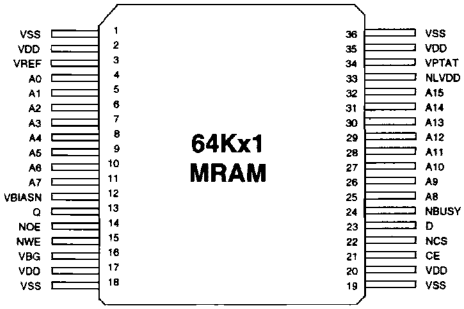


TRUTH TABLE

CE	NCS	NWE	NOE	MODE	Q
H	L	H	L	Read	Data Out
H	L	L	X	Write	High Z
H	H	X	XX	Deselected	High Z
L	XX	XX	XX	Disabled	High Z

Notes: X : $V_I = V_{IH}$ or V_{IL} XX: $V_{SS} \leq V_I \leq V_{DD}$

PINOUT CONFIGURATION



GENERAL DESCRIPTION

The 64Kx1 Magnetoresistive RAM (MRAM™) is a non-volatile and non-destructive read out random access memory. Fabricated with our Radiation Insensitive CMOS (RICMOS™) process, it is designed for strategic radiation environments. Attractive features include unlimited power off storage, unlimited read/write cycles, and 5 volt operation. The 64Kx1 is offered in a JEDEC compatible 36-lead flat pack designed for radiation environments, with optional decoupling capacitors.

DC and AC ELECTRICAL CHARACTERISTICS (1,2)

Symbol	Parameter	Min	Max	Units	Test Condition
IDDSB	Standby Supply Current		2	mA	VIH/VIL=VDD/VSS IO=0, Inputs Stable
IDDOP	Dynamic Supply Current, Selected		100	mA	f=1 MHz VIH/VIL=VDD/ VSS IO=0, Note 4
VIL	Low-Level Input Voltage		$0.3*V_{DD}$	V	Addr. Compliment Pattern VDD = 4.5 V
VIH	High-Level Input Voltage	$0.7*V_{DD}$		V	Addr. Compliment Pattern VDD = 4.5 V
VOL	Low-Level Output Voltage		0.4	V	IOL= 4 mA, VDD=4.5 V
VOH	High-Level Output Voltage	2.4		V	IOH= -1 mA, VDD=4.5 V
II	Input Leakage Current	-1	1	µA	VSS≤VI≤VDD
IOZ	Output Leakage Current	-1	1	µA	VSS≤VO≤VDD Output=high Z
TSLSLR	Read Cycle Time (NCS Control)	1		µs	(3)
TSLSLW	Write Cycle Time (NCS Control)	250		ns	(3)
TAVSL	Address Set Up Time	10		ns	
TSLQV	Chip Select Access Time		750	ns	
TSHQZ	Chip Deselect to Output High Z Time		25	ns	
TPUP	Power Up Time from 0V to Spec.	2		µs	
HEXT	Shielding to External Magnetic Fields		50	Oe	Either AC or DC fields 1 Oersted = 79.58 A/m

(1) For timing diagrams and Absolute Maximum Ratings see the HC6364 data sheet.

(2) Worst case operating conditions: VDD=4.5 V to 5.5 V, TA=-55°C to +125°C, total dose through $1x10^6$ rad(SiO_2) unless otherwise noted.

(3) Input levels are VIL/VIH=0.5/VDD-0.5V, input rise and fall times <5ns, timing reference =VDD/2 V, CL=50pF.

(4) All inputs switching. DC average current.

ORDERING INFORMATION

H C 7464/1 X S H N C

SOURCE
H=HONEYWELL

PART NUMBER

SCREEN LEVEL (1)
C=Brass Board
S=Class S

SOFT ERROR RATE (2)
N=No Upsets

PROCESS
C=CMOS

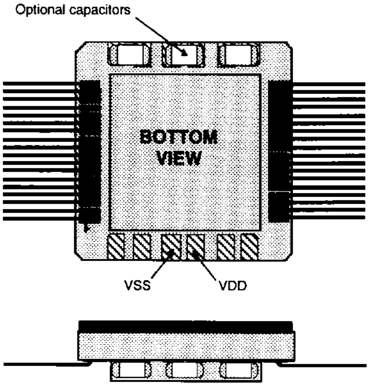
PACKAGE DESIGNATION
X=36-Lead Flat Pack

RADIATION HARDNESS
H=1E6 rad(SiO_2)

INPUT BUFFER TYPE
C=CMOS Levels
T=TTL Levels

(1) Refer to HC6364 data sheet for Honeywell modified Class S screening procedures.
(2) SER spec. indicate worst case, high temperature (125°C), post-total dose performance.

Optional decoupling capacitors can be mounted on the backside of the package. This helps to reduce supply rail collapse under transient upset conditions.



36 - LEAD FLAT PACK

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