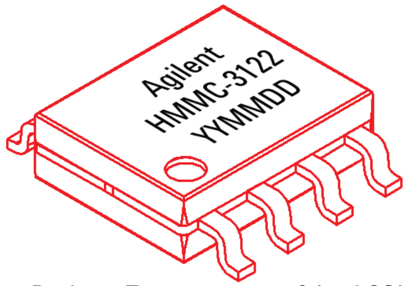
Agilent HMMC-3122 DC-12 GHz Packaged High Efficiency Divide-by-2 Prescaler

1GC1-8209-TR1-7" diameter reel/500 each
1GC1-8209-BLK-bubble strip/10 each

Data Sheet



Package Type:	8-lead SOIC Plastic
Package Dimensions:	4.9 x 3.9 mm typ.
Package Thickness:	1.55 mm typ.
Lead Pitch:	1.25 mm nom.
Lead Width:	0.42 mm nom.

Features

- **Wide Frequency Range: 0.2-12 GHz**
- **High Input Power Sensitivity: On-chip pre- and post-amps -15 to +10 dBm (1-8 GHz) -10 to +8 dBm (8-10 GHz) -5 to +2 dBm (10-12 GHz)**
- **P_{out}: 0 dBm (0.5 V_{p-p})**
- **Low Phase Noise: -153 dBc/Hz @ 100 kHz Offset**
- **(+) or (-) Single Supply Bias Operation**
- **Wide Bias Supply Range: 4.5 to 6.5 volt operating range**
- **Differential I/O with on-chip 50 Ω matching**

Description

The HMMC-3122 is a packaged GaAs HBT MMIC pre-scaler which offers dc to 12 GHz frequency translation for use in communications and EW systems incorporating high-frequency PLL oscillator circuits and signal-path down conversion applications. The prescaler provides a large input power sensitivity window and low phase noise.

Absolute Maximum Ratings[1]

(@ T_A = 25°C, unless otherwise indicated)

Symbol	Parameters/Conditions	Min.	Max.	Units
V_{CC}	Bias supply voltage		+7	volts
V_{EE}	Bias supply voltage	-7		volts
V_{CC} - V_{EE}	Bias supply delta	0	+7	volts
V_{Logic}	Logic threshold voltage	V_{CC} -1.5	V_{CC} -1.2	volts
$P_{in(CW)}$	CW RF input power		+10	dBm
V_{RFin}	DC input voltage (@ RF_{in} or $\overline{RF}_{in}$ ports)		V_{CC} ±0.5	volts
T_{BS}[2]	Backside operating temperature	-40	+85	°C
T_{st}	Storage temperature	-65	+165	°C
T_{max}	Maximum assembly temperature (60 s max.)		310	°C

Notes

1. Operation in excess of any parameter limit (except T_{BS}) may cause permanent damage to the device.
2. MTTF > 1 x 10^6 hours @ T_{BS} ≤ 85°C. Operation in excess of maximum operating temperature (T_{BS}) will degrade MTTF.

DC Specifications/Physical Properties

(T_A = 25°C, $V_{CC} – V_{EE}$ = 5.0 volts, unless otherwise listed)

Symbol	Parameters/Conditions	Min.	Typ.	Max.	Units
$V_{CC} – V_{EE}$	Operating bias supply difference[1]	4.5	5.0	6.5	volts
$\|I_{CC}\|$ or $\|I_{EE}\|$	Bias supply current	34	40	46	mA
$V_{RFin(q)}$ $V_{RFout(q)}$	Quiescent dc voltage appearing at all RF ports		V_{CC}		volts
V_{Logic}	Nominal ECL Logic Level (V_{Logic} contact self-bias voltage, generated on-chip)	V_{CC} -1.45	V_{CC} -1.32	V_{CC} -1.25	volts

Notes

1. Prescaler will operate over full specified supply voltage range, V_{CC} or V_{EE} not to exceed limits specified in Absolute Maximum Ratings section.

RF Specifications

(T_A = 25°C, Z_0 = 50 Ω, $V_{CC} – V_{EE}$ = 5.0 volts)

Symbol	Parameters/Conditions	Min.	Typ.	Max.	Units
$f_{in(max)}$	Maximum input frequency of operation	12	14		GHz
$f_{in(min)}$	Minimum input frequency of operation[1] (P_{in} = -10 dBm)		0.2	0.5	GHz
$f_{Self-Osc.}$	Output Self-Oscillation Frequency[2]		3.4		GHz
P_{in}	@ dc, (Square-wave input)	-15	> -25	+10	dBm
	@ f_{in} = 500 MHz, (Sine-wave input)	-15	> -20	+10	dBm
	f_{in} = 1 to 8 GHz	-15	> -20	+10	dBm
	f_{in} = 8 to 10 GHz	-10	> -15	+5	dBm
	f_{in} = 10 to 12 GHz	-5	> -10	+1	dBm
RL	Small-Signal Input/Output Return Loss (@ f_{in} < 10 GHz)		15		dB
S_{12}	Small-Signal Reverse Isolation (@ f_{in} < 10 GHz)		30		dB
Φ_N	SSB Phase noise (@ P_{in} = 0 dBm, 100 kHz offset from a f_{out} = 1.2 GHz Carrier)		-153		dBc/Hz
Jitter	Input signal time variation @ zero-crossing (f_{in} = 10 GHz, P_{in} = -10 dBm)		1		ps
T_r or T_f	Output transition time (10% to 90% rise/fall time)		70		ps

Notes

1. For sine-wave input signal. Prescaler will operate down to dc for square-wave input signal. Minimum divide frequency limited by input slew-rate.
2. Prescaler may exhibit this output signal under bias in the absence of an RF input signal. This condition may be eliminated by use of the Input dc offset technique described on page 4.

RF Specifications (Continued)

(T_A = 25°C, Z_0 = 50 Ω, $V_{CC} - V_{EE}$ = 5.0 volts)

Symbol	Parameters/Conditions	Min.	Typ.	Max.	Units
P_{out}[3]	@ f_{out} < 1 GHz	-2	0		dBm
	@ f_{out} = 2.5 GHz	-3.5	-1.5		dBm
	@ f_{out} = 3.0 GHz	-4.5	-2.5		dBm
$\lvert V_{out(p-p)} \rvert$[4]	@ f_{out} < 1 GHz		0.5		volts
	@ f_{out} = 2.5 GHz		0.42		volts
	@ f_{out} = 3.0 GHz		0.37		volts
$P_{Spitback}$	f_{out} power level appearing at RF_{in} or $\overline{RF}_{in}$ (@ f_{in} 10 GHz, unused RF_{out} or $\overline{RF}_{out}$ **unterminated**)		-50		dBm
	f_{out} power level appearing at RF_{in} or $\overline{RF}_{in}$ (@ f_{in} = 10 GHz, both RF_{out} & $\overline{RF}_{out}$ **terminated**)		-55		dBm
$P_{feedthru}$	Power level of f_{in} appearing at RF_{out} or $\overline{RF}_{out}$ (@ f_{in} = 12 GHz, P_{in} = 0 dBm, referred to P_{in} (f_{in}))		-30		dBc
H_2	Second harmonic distortion output level (@ f_{out} = 3.0 GHz, referred to P_{out} (f_{out}))		-25		dBc

Notes

3. Fundamental of output square wave's Fourier Series.
4. Square wave amplitude calculated from P_{out}.

Applications

The HMMC-3122 is designed for use in high frequency communications, microwave instrumentation, and EW radar systems where low phase-noise PLL control circuitry or broad-band frequency translation is required.

Operation

The device is designed to operate when driven with either a single-ended or differential sinusoidal input signal over a 200 MHz to 12 GHz bandwidth. Below 200 MHz the prescaler input is "slew-rate" limited, requiring fast rising and falling edge speeds to properly divide. The device will operate at frequencies down to dc when driven with a square-wave.

Due to the presence of an off-chip RF-bypass capacitor inside the package (connected to the V_{CC} contact on the device), and the unique design of the device itself, the component may be biased from either a single positive or single negative supply bias. The backside of the package is not dc connected to any dc bias point on the device.

For positive supply operation, V_{CC} pins are nominally biased at any voltage in the +4.5 to +6.5 volt range with pin 8 (V_{EE}) grounded. For negative bias operation V_{CC} pins are typically grounded and a negative voltage between -4.5 to -6.5 volts is applied to pin 8 (V_{EE}).

AC-Coupling and DC-Blocking

All RF ports are dc connected on-chip to the V_{CC} contact through on-chip 50 Ω resistors. Under any bias conditions where V_{CC} is not dc grounded the RF ports should be ac coupled via series capacitors mounted on the PC board at each RF port. Only under bias conditions where V_{CC} is dc grounded (as is typical for negative bias supply operation) may the RF ports be direct coupled to adjacent circuitry or in some cases, such as level shifting to subsequent stages. In the latter case the package heat sink may be "floated" and bias applied as the difference between V_{CC} and V_{EE}.

Input DC Offset

If an RF signal with sufficient signal to noise ratio is present at the RF input lead, the prescaler will operate and provide a divided output equal the input frequency divided by the divide modulus. Under certain “ideal” conditions where the input is well matched at the right input frequency, the component may “self-oscillate”, especially under small signal input powers or with only noise present at the input. This “self-oscillation” will produce a undesired output signal also known as a false trigger. To prevent false triggers or self-oscillation conditions, apply a 20 to 100 mV dc offset voltage between the RF_{in} and RF_{in} ports. This prevents noise or spurious low level signals from triggering the divider.

Adding a 10 kΩ resistor between the unused RF input to a contact point at the V_{EE} potential will result in an offset of ≈ 25 mV between the RF inputs. Note however, that the input sensitivity will be reduced slightly due to the presence of this offset.

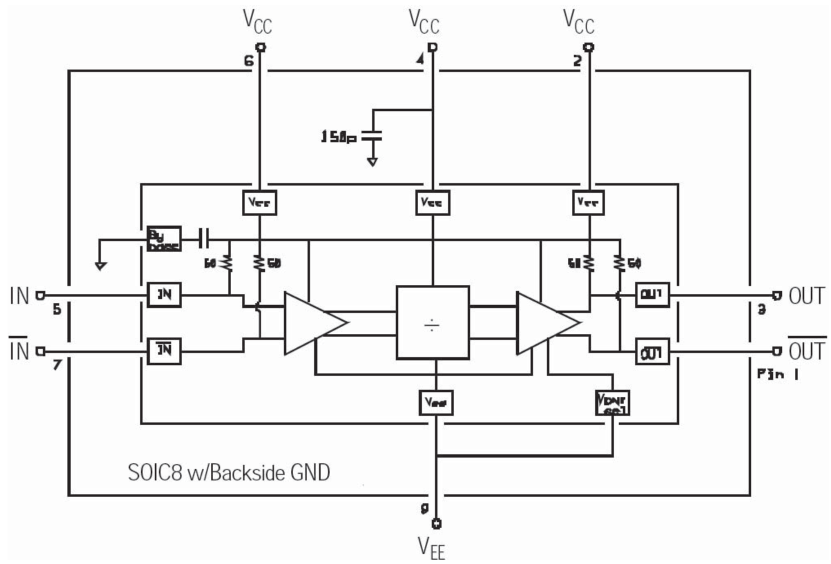


Figure 1. Simplified Schematic

Assembly Notes

Independent of the bias applied to the package, the backside of the package should always be connected to both a good RF ground plane and a good thermal heat sinking region on the PC board to optimize performance. For single-ended output operation the unused RF output lead should be terminated into 50 Ω to a contact point at the V_{CC} potential or to RF ground through a dc blocking capacitor.

A minimum RF and thermal PC board contact area equal to or greater than 2.67 × 1.65 mm (0.105" × 0.065") with eight 0.020" diameter plated-wall thermal vias is recommended.

MMIC ESD precautions, handling considerations, die attach and bonding methods are critical factors in successful GaAs MMIC performance and reliability.

Agilent application note #54, “GaAs MMIC ESD, Die Attach and Bonding Guidelines” provides basic information on these subjects.

Moisture Sensitivity Classification: Class 1, per JESD22-A112-A.

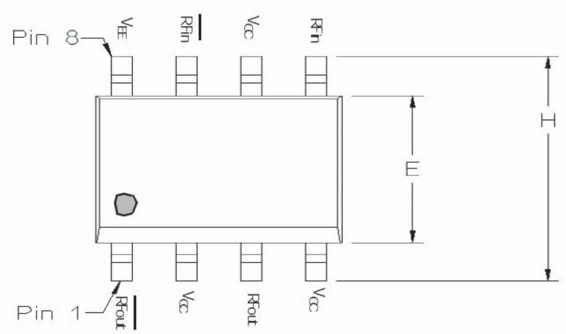
Additional References:

PN #18, “HBT Prescaler Evaluation Board.”

Symbol	Min.	Max.
A	1.35	1.75
A1	0.0	.25
B	0.33	0.51
C	0.19	.025
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	1.27 BSC
H	5.80	6.20
L	0.40	1.27
a	0°	8°

Notes:

- All dimensions in millimeters.
- Refer to JEDEC Outline MS-012 for additional tolerances.
- Exposed heat slug area on package bottom = 2.67 x 1.65.
- Exposed heat sink on package bottom must be soldered to PCB rf ground plane.



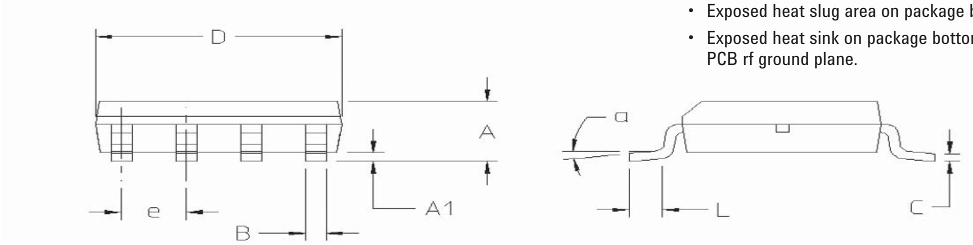


Figure 2. Package and dimensions

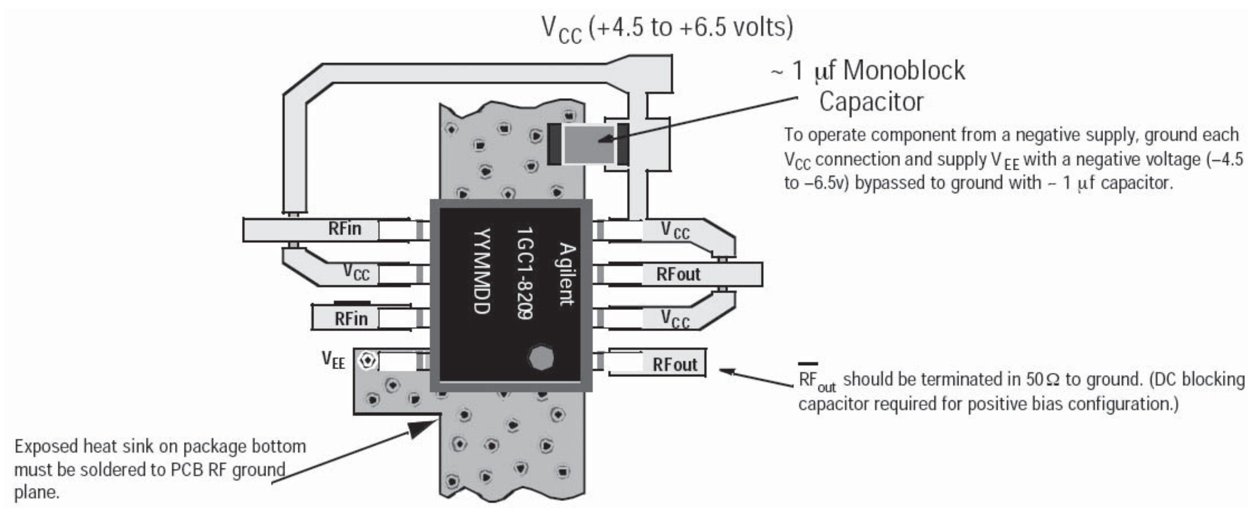


Figure 3. Assembly diagram (Single-supply, positive-bias configuration shown)

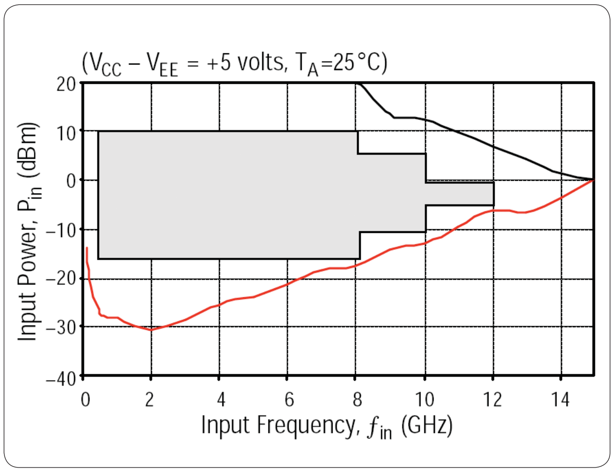


Figure 4. Typical input sensitivity window

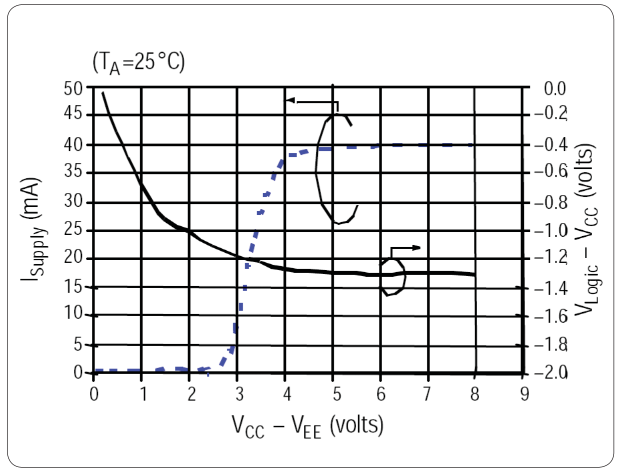


Figure 5. Typical supply current & V_{Logic} vs. supply voltage

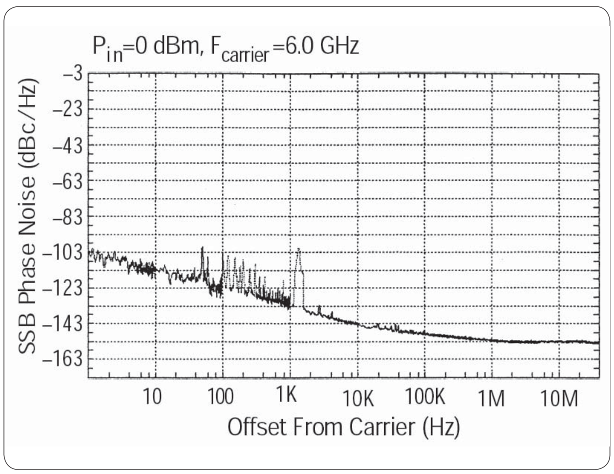


Figure 6. Typical phase noise performance

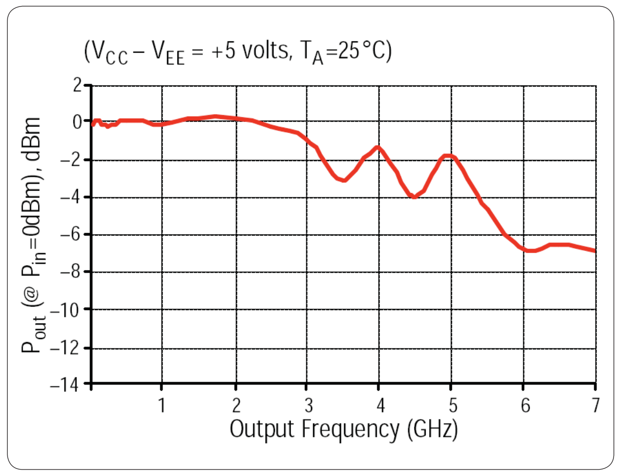


Figure 7. Typical output power vs. output frequency, f_{out} (GHz)

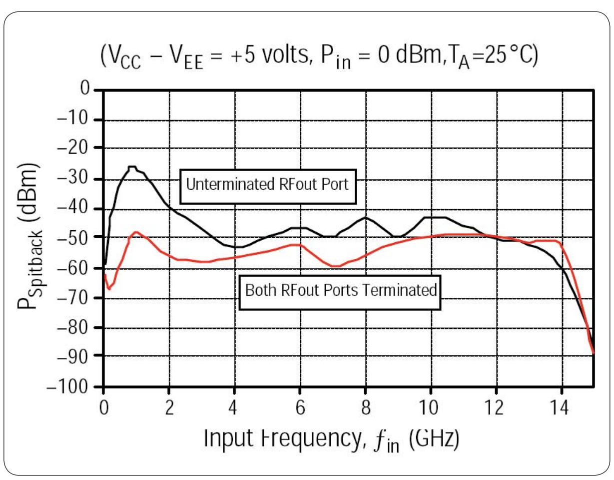
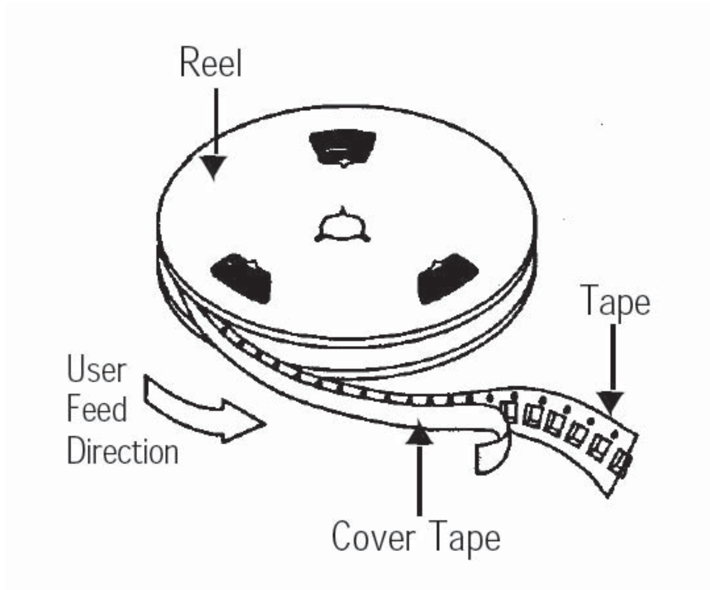
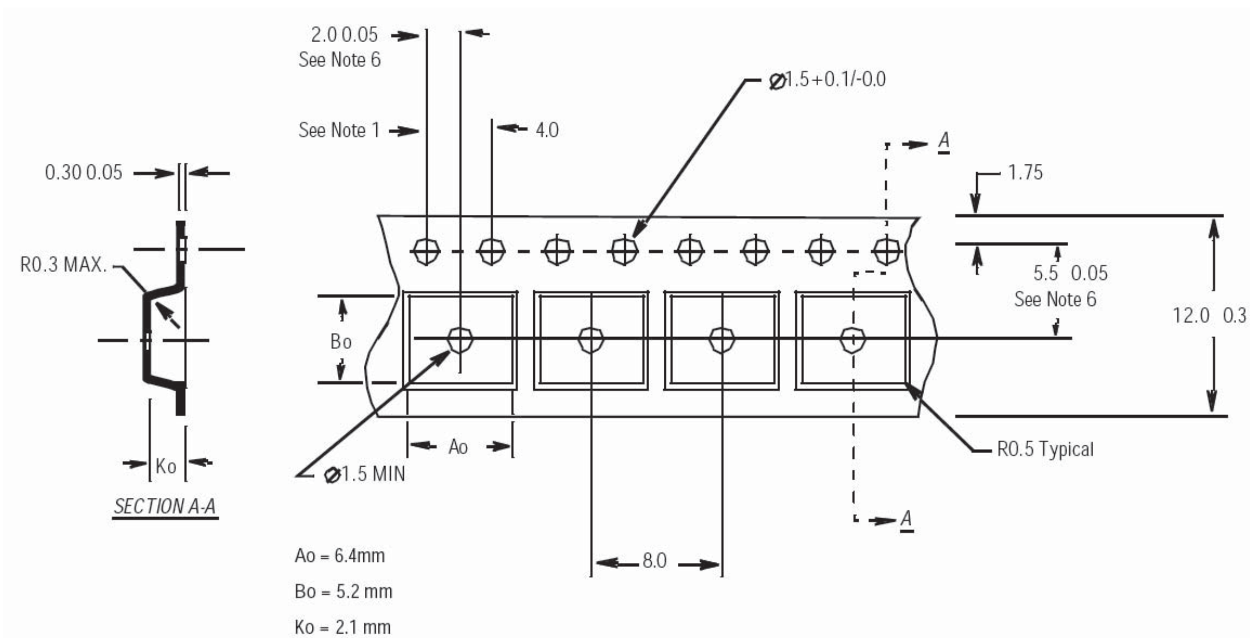


Figure 8. Typical "Spitback" power P(f_{out}) appearing at RF input port

Device Orientation



Tape Dimensions and Product Orientation



Notes:

1. 10 sprocket hole pitch cumulative tolerance: 0.2 mm.
2. Camber not to exceed 1 mm in 100 mm.
3. Material: Black Conductive Advantek Polystyrene.
4. Ao and Bo measured on a plane 0.3 mm above the bottom of the pocket.
5. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

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