

Am2916A

Quad Three-State Bus Transceiver With Interface Logic

Distinctive Characteristics

- Quad high-speed LSI bus-transceiver
- Three-state bus driver
- Two-port input to D-type register on driver
- Bus driver output can sink 48mA at 0.5V max.
- Internal odd 4-bit parity checker/generator
- Receiver has output latch for pipeline operation
- Receiver outputs sink 12mA
- Advanced low-power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883
- 3.5V minimum output high voltage for direct interface to MOS microprocessors

FUNCTIONAL DESCRIPTION

The Am2916A is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops with a built-in two-input multiplexer on each. The flip-flop outputs are connected to four three-state bus drivers. Each bus driver is internally connected to the input of a receiver. The four receiver outputs drive four D-type latches. The device also contains a four-bit odd parity checker/generator.

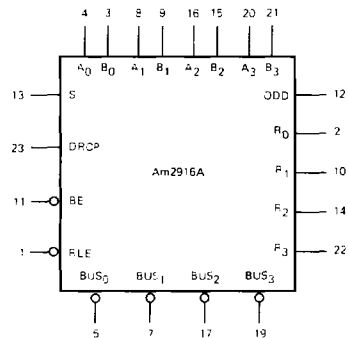
The LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The three-state bus output can sink up to 48mA at 0.5V maximum. The bus enable input (\overline{BE}) is used to force the driver outputs to the high-impedance state. When \overline{BE} is HIGH, the driver is disabled.

The input register consists of four D-type flip-flops with a buffered common clock and a two-input multiplexer at the input of each flip-flop. A common select input (S) controls the four multiplexers. When S is LOW, the A_i data is stored in the register and when S is HIGH, the B_i data is stored. The buffered common clock (DRCP) enters the data into this driver register on the LOW-to-HIGH transition.

Data from the A or B input is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data in non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable (\overline{RLE}) input. When the \overline{RLE} input is LOW, the latch is open and the receiver outputs will follow the bus inputs (BUS data inverted). When the \overline{RLE} input is HIGH, the latch will close and retain the present data regardless of the bus input.

The Am2916A features a built-in four-bit odd parity checker/generator. The bus enable input (\overline{BE}) controls whether the parity output is in the generate or check mode. When the bus enable is LOW (driver enabled), odd parity is generated based on the A or B field data input to the driver register. When \overline{BE} is HIGH, the parity output is determined by the four latch outputs of the receiver. Thus, if the driver is enabled, parity is generated and if the driver is in the high-impedance state, the BUS parity is checked.

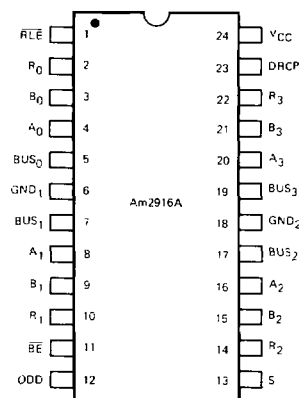
LOGIC SYMBOL



V_{CC} = Pin 24
 GND_1 = Pin 6
 GND_2 = Pin 18

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CONNECTION DIAGRAM Top View



Note: Pin 1 is marked for orientation.

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ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2916AXC (COM'L) $T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC\text{MIN.}} = 4.75\text{V}$ $V_{CC\text{MAX.}} = 5.25\text{V}$
 Am2916AXM (MIL) $T_A = -55^\circ\text{C to } -125^\circ\text{C}$ $V_{CC\text{MIN.}} = 4.50\text{V}$ $V_{CC\text{MAX.}} = 5.50\text{V}$

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

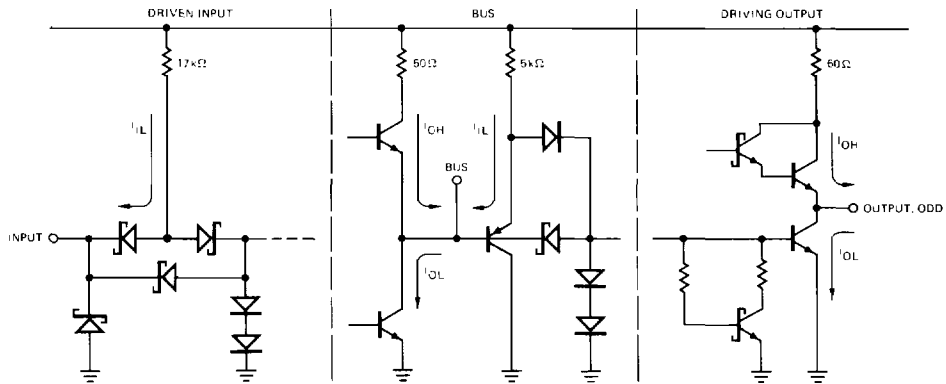
Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V _{OH}	Receiver Output HIGH Voltage	V _{CC} = MIN.	MIL: I _{OH} = -1.0mA	2.4	3.4		Volts
		V _{IN} = V _{IL} or V _{IH}	COM'L: I _{OH} = -2.6mA	2.4	3.4		
		V _{CC} = 5.0V, I _{OH} = -100μA		3.5			
V _{OH}	Parity Output HIGH Voltage	V _{CC} = MIN., I _{OH} = -660μA V _{IN} = V _{IH} or V _{IL}	MIL	2.5	3.4		Volts
			COM'L	2.7	3.4		
V _{OL}	Output LOW Voltage (Except Bus)	V _{CC} = MIN. V _{IN} = V _{IL} or V _{IH}	I _{OL} = 4.0mA		0.27	0.4	Volts
			I _{OL} = 8.0mA		0.32	0.45	
			I _{OL} = 12mA		0.37	0.5	
V _{IH}	Input HIGH Level (Except Bus)	Guaranteed input logical HIGH for all inputs		2.0			Volts
V _{IL}	Input LOW Level (Except Bus)	Guaranteed input logical LOW for all inputs	MIL			0.7	Volts
			COM'L				
V _I	Input Clamp Voltage (Except Bus)	V _{CC} = MIN., I _{IN} = -18mA				-1.2	Volts
I _{IL}	Input LOW Current (Except Bus)	V _{CC} = MAX., V _{IN} = 0.4V	\overline{BE} , $\overline{RL\overline{E}}$			-0.72	mA
			All other inputs				
I _{IH}	Input HIGH Current (Except Bus)	V _{CC} = MAX., V _{IN} = 2.7V				20	μA
I _I	Input HIGH Current (Except Bus)	V _{CC} = MAX., V _{IN} = 7.0V				100	μA
I _{SC}	Output Short Circuit Current (Except Bus)	V _{CC} = MAX.	RECEIVER	-30		-130	mA
			PARITY	-20		-100	
I _{CC}	Power Supply Current	V _{CC} = MAX., All Inputs = GND			75	110	mA

SWITCHING CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions	Am2916AXM			Am2916AXC			Units
			Min.	Typ. (Note 2)	Max.	Min.	Typ. (Note 2)	Max.	
t _{PHL}	Driver Clock (DRCP) to Bus	C _L (BUS) = 50pF R _L (BUS) = 130Ω		21	36		21	32	ns
t _{PLH}				21	36		21	32	
t _{ZH} , t _{ZL}	Bus Enable (\overline{BE}) to Bus			13	26		13	23	ns
t _{HZ} , t _{LZ}				13	21		13	18	
t _s	Data Inputs (A or B)			15			12		ns
t _h				8.0			6.0		
t _s	Select Inputs (S)			28			25		ns
t _h				8.0			6.0		
t _{PW}	Clock Pulse Width (HIGH)			20			17		ns
t _{PLH}	Bus to Receiver Output (Latch Enabled)			18	33		18	30	ns
t _{PHL}				18	30		18	27	
t _{PLH}	Latch Enable to Receiver Output			21	33		21	30	ns
t _{PHL}				21	30		21	27	
t _s	Bus to Latch Enable ($\overline{RL\overline{E}}$)	C _L = 15pF R _L = 2.0kΩ		15			13		ns
t _h				6.0			4.0		
t _{PLH}	A or B Data to Odd Parity Output (Driver Enabled)			32	46		32	42	ns
t _{PHL}				26	40		26	36	
t _{PLH}	Bus to Odd Parity Output (Driver Inhibited, Latch Enabled)			21	36		21	32	ns
t _{PHL}				21	36		21	32	
t _{PLH}	Latch Enable ($\overline{RL\overline{E}}$) to Odd Parity Output			21	36		21	32	ns
t _{PHL}				21	36		21	32	

- Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
 2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
 3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

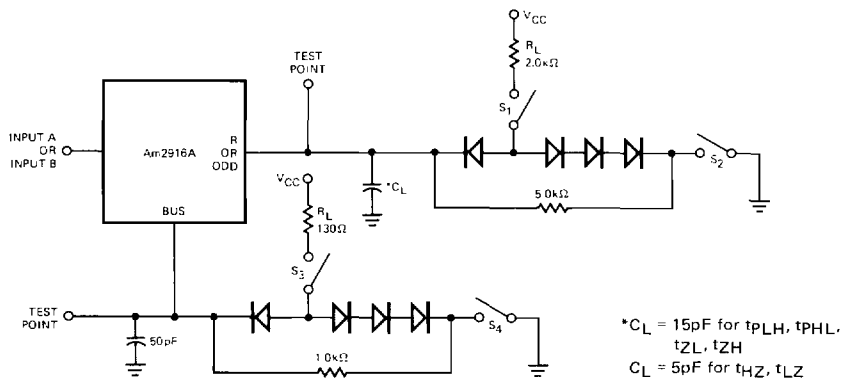
INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

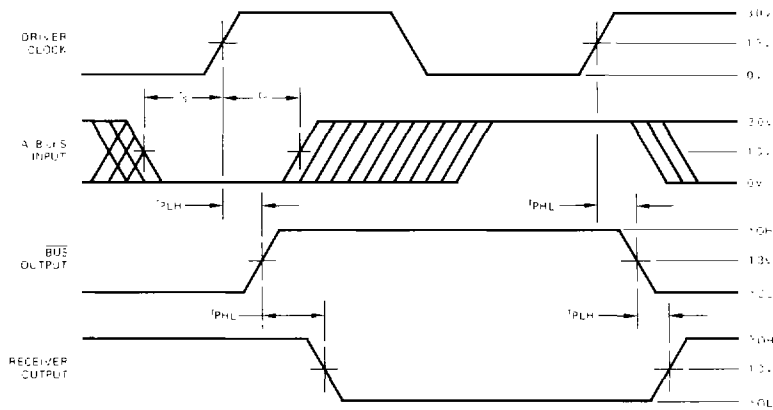
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SWITCHING TEST CIRCUIT



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SWITCHING WAVEFORMS



Note: Bus to Receiver output delay is measured by clocking data into the driver register and measuring the $\overline{\text{BUS}}$ to R combinatorial delay.

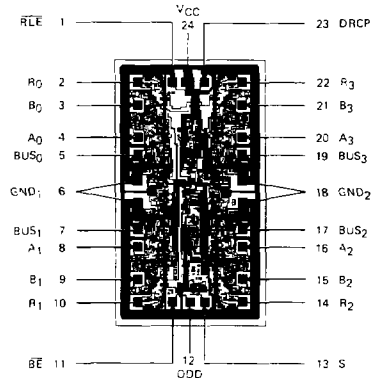
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FUNCTION TABLE

INPUTS				INTERNAL TO DEVICE				BUS	OUTPUT	FUNCTION	
S	A _i	B _i	DRCP	BE	RLE	OE	D _i	Q _i	BUS _i		R _i
X	X	X	X	H	X	X	X	X	Z	X	Driver output disable
X	X	X	X	X	X	H	X	X	X	Z	Receiver output disable
X	X	X	X	H	L	L	X	L	L	H	Driver output disable and receive data via Bus input
X	X	X	X	H	L	L	X	H	H	L	Driver output disable and receive data via Bus input
X	X	X	X	X	H	X	X	NC	X	X	Latch received data
L	L	X	↑	X	X	X	L	X	X	X	Load driver register
L	H	X	↑	X	X	X	H	X	X	X	
H	X	L	↑	X	X	X	L	X	X	X	
H	X	H	↑	X	X	X	H	X	X	X	
X	X	X	L	X	X	X	NC	X	X	X	No driver clock restrictions
X	X	X	H	X	X	X	NC	X	X	X	No driver clock restrictions
X	X	X	X	L	X	X	L	X	H	X	Drive Bus
X	X	X	X	L	X	X	H	X	L	X	

H = HIGH Z = HIGH impedance X = Don't care i = 0, 1, 2, 3
 L = LOW NC = No change ↑ = LOW to HIGH transition

Metallization and Pad Layout



DIE SIZE .074" X .130"

DEFINITION OF FUNCTIONAL TERMS

- A₀, A₁, A₂, A₃** The "A" word data input into the two input multiplexer of the driver register.
- B₀, B₁, B₂, B₃** The "B" word data input into the two input multiplexers of the driver register.
- S** Select. When the select input is LOW, the A data word is applied to the driver register. When the select input is HIGH, the B word is applied to the driver register.
- DRCP** Driver Clock Pulse. Clock pulse for the driver register.
- BE** Bus Enable. When the Bus Enable is HIGH, the four drivers are in the high impedance state.

- BUS₀, BUS₁, BUS₂, BUS₃** The four driver outputs and receiver inputs (data is inverted).
- R₀, R₁, R₂, R₃** The four receiver outputs. Data from the bus is inverted while data from the A or B inputs is non-inverted.
- RLE** Receiver Latch Enable. When RLE is LOW, data on the BUS inputs is passed through the receiver latches. When RLE is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.
- OE** Output Enable. When the OE input is HIGH, the four three state receiver outputs are in the high-impedance state.

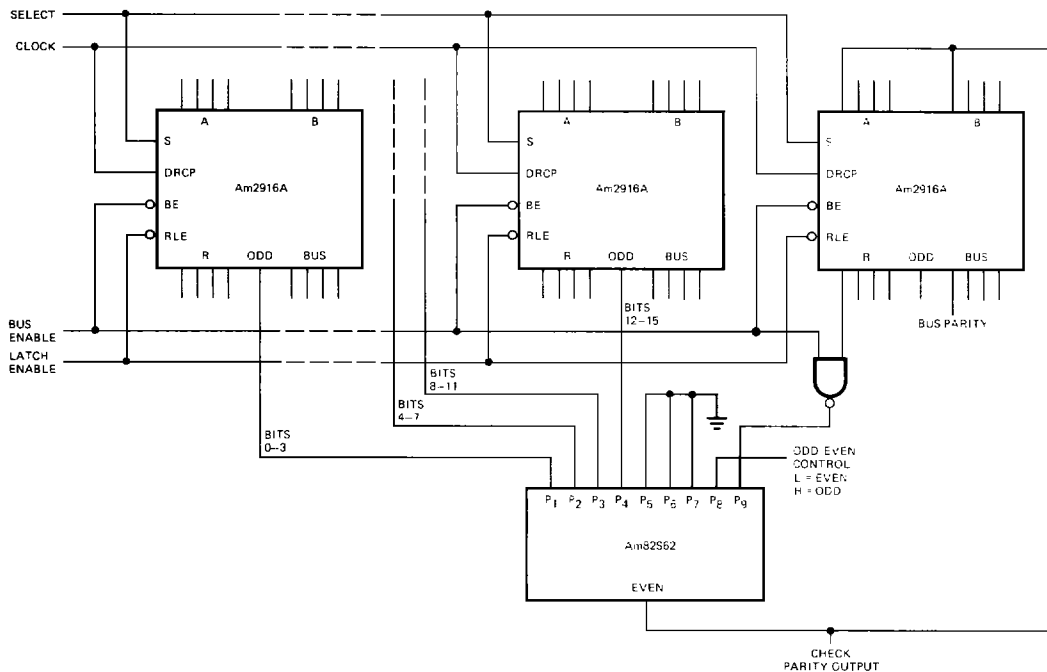
ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Temperature Range (Note 2)	Screening Level (Note 3)
AM2916APC	P-24	C	C-1
AM2916ADC	D-24	C	C-1
AM2916ADC-B	D-24	C	B-1
AM2916ADM	D-24	M	C-3
AM2916ADM-B	D-24	M	B-3
AM2916AFM	F-24	M	C-3
AM2916AFM-B	F-24	M	B-3
AM2916AXC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2916AXM	Dice	M	

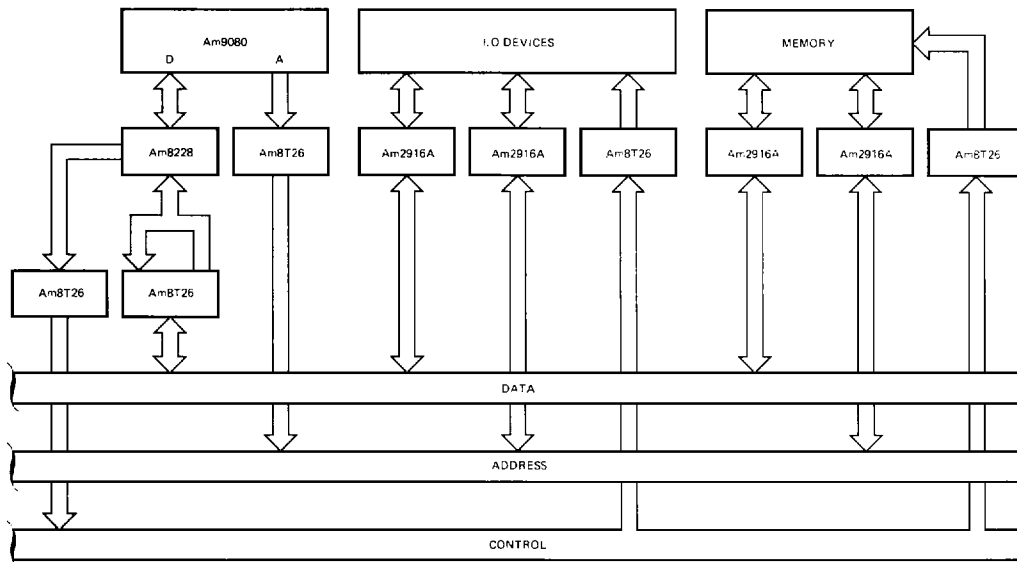
- Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
 2. C = 0°C to +70°C, M = -55°C to +125°C.
 3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

APPLICATIONS



Generating or checking parity for 16 data bits.

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Using the Am2916A and Am8T26 in a terminated Bus system for the Am9080 MOS Microprocessor.

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