LR3692 LCD Dot Matrix Controller LSI

Description

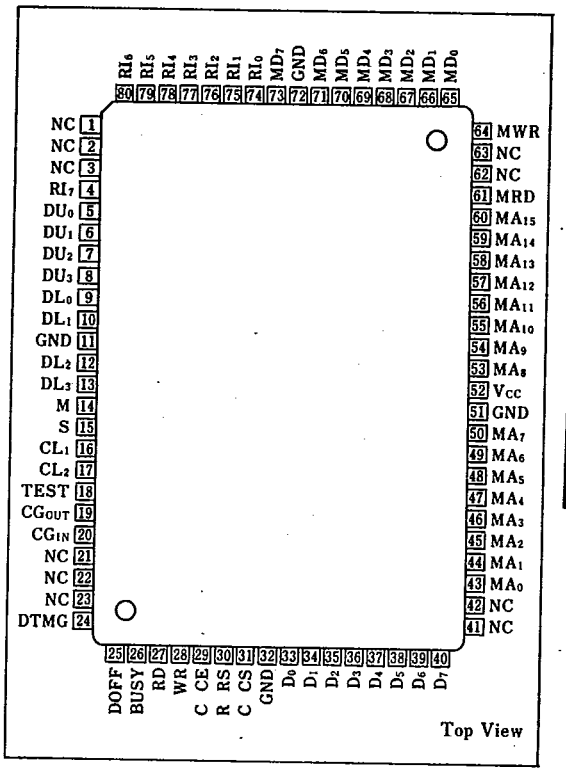
The LR3692 is a CMOS controller LSI for dot matrix graphic LCD unit. It stores display data transferred from 8-bit microcomputer in the external RAM and generates the LCD drive signal which meets the serial type LCD driver.

It has selectable two modes including a graphic mode and a character mode using character generator ROM.

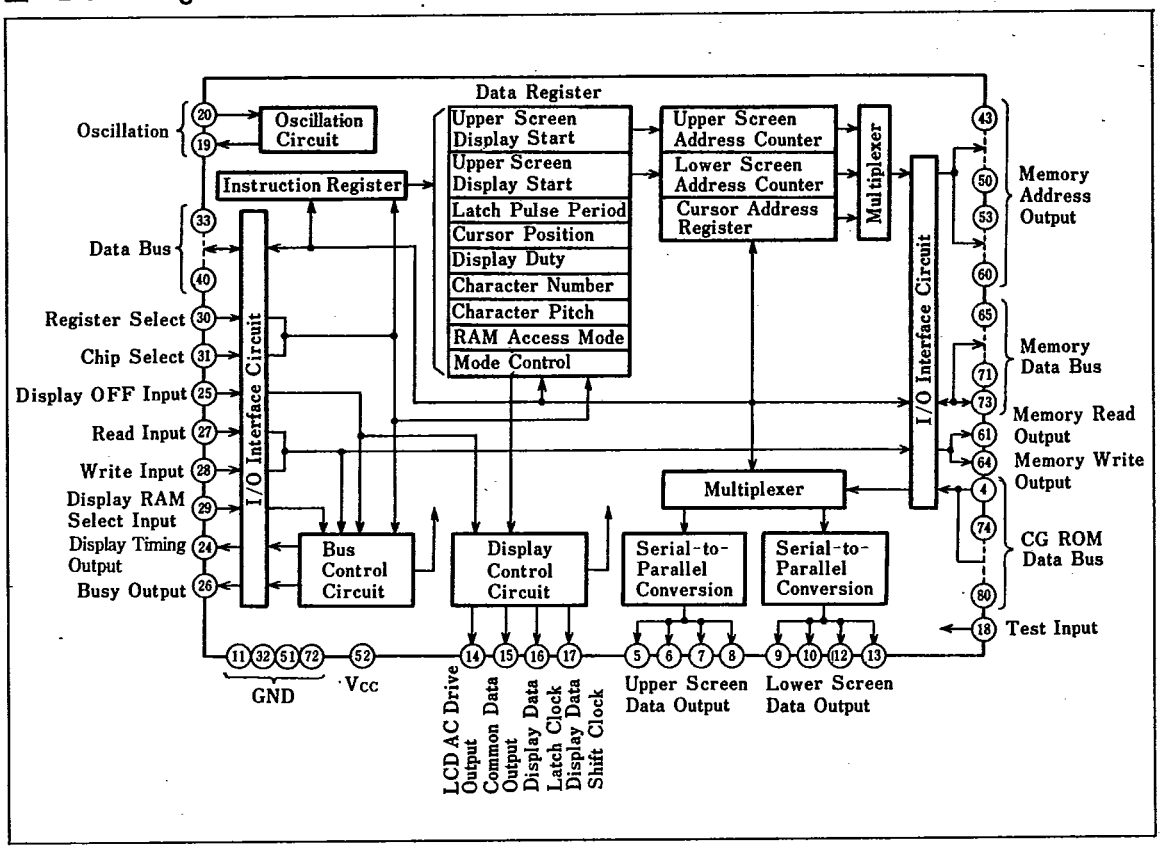
Features

1. Graphic or character mode selectable
2. Display duty : 1/32-1/256
3. Maximum display capability
   Graphic mode : 640 × 256 dots
   Character mode : 80 × 32 characters
   (if character font is 8 × 8)
4. Capable of interfacing to an 8-bit CPU
5. Serial/ 4-bit parallel output
6. Separated LCD screen drive for upper and lower divisions
7. Scroll function
8. Cursor display : ON, OFF, and BLINK
9. Character BLINK
10. Display ON, OFF
11. On-chip crystal oscillator
12. Single power supply : 5V (TYP.)
13. CMOS process
14. 80-pin quad-flat package

Pin Connections



Block Diagram



■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Note
Supply voltage	V_{DD}	−0.3 to +7	V	1
Input voltage	V_{IN}	−0.3 to V_{DD}+0.3	V	1
Operating temperature	T_{opr}	−20 to +70	°C	
Storage temperature	T_{stg}	−55 to +150	°C	

Note 1: The maximum applicable voltage on any pin with respect to GND.

■ Recommended Operating Conditions

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}	4.75		5.25	V

■ DC Characteristics

(V_{DD}=5V±5%, Ta=0 to +50℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Input low voltage	V_{ILT}		0		0.4	V	1
Input high voltage	V_{IHT}		2.4		V_{DD}	V	1
Input low voltage	V_{ILC}		0		0.2V_{DD}	V	2
Input high voltage	V_{IHC}		0.8V_{DD}		V_{DD}	V	2
Output low voltage	V_{OLT}	I_{OL}=2.0mA			0.4	V	3
Output high voltage	V_{OHT}	I_{OH}=1.0mA	2.4			V	3
Output low voltage	V_{OLC}	I_{OL}=0.6mA			0.4	V	4
Output high voltage	V_{OHC}	I_{OH}=0.6mA	V_{DD}−0.4			V	4
Pull-up current	I_{LI}	V_{IN}=0V		6	30	μA	5
Supply current	I_{DD}	fosc = 4MHz		2	10	mA	
Oscillator frequency	fosc	With crystal oscillator		4		MHz	6
Ext. clock frequency	f_{CL}		0.2		4	MHz	6
Ext. clock duty	Duty		47.5	50	52.5	%	6
Rise time	t_{RCL}				50	ns	6
Fall time	t_{FCL}				50	ns	6

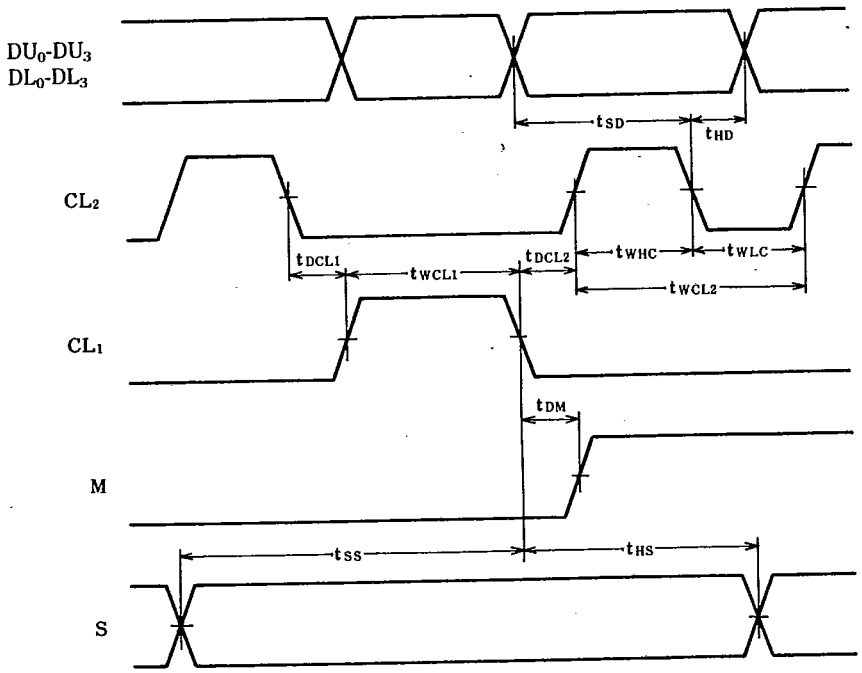
Note 1: Applied to pins $\overline{MD_0}$-MD_7, RI_0-RI_7, D_0-D_7, $\overline{CS}$, RS, $\overline{CE}$, $\overline{WR}$, $\overline{RD}$, and $\overline{DOFF}$.
Note 2: Applied to pins $\overline{TEST}$ and CG_{IN}.
Note 3: Applied to pins MA_0-MA_{15}, MD_0-MD_7, $\overline{MWR}$, $\overline{MRD}$, D_0-D_7, $\overline{BUSY}$, and DTMG.
Note 4: Applied to pins CL_1, CL_2, S, DU_0-OU_3, DL_0-DL_3, and M.
Note 5: Applied to pins TEST, MA_0-MA_{15}, MD_0-MD_7, RI_0-RI_7, D_0-D_7, $\overline{CS}$, RS, $\overline{CE}$, $\overline{WR}$, $\overline{RD}$, and $\overline{DOFF}$.
Note 6: Applied to pins CG_{IN} and CG_{OUT}.

AC Characteristics

(1) LCD control signal

(V_{CC}=5V±5%, fosc=4MHz, C_L=15pF, Ta=0~+50℃)

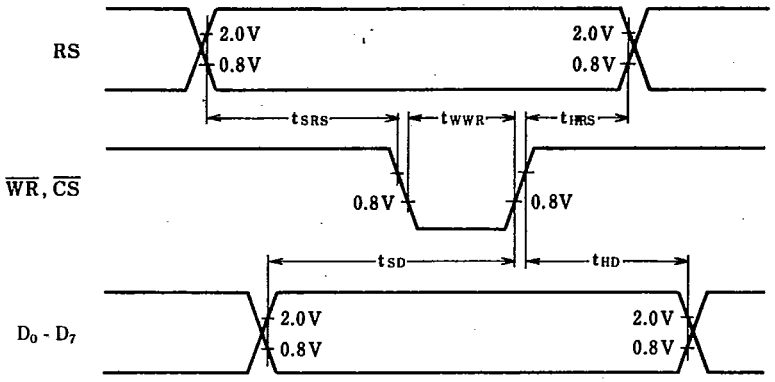
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data setup time	t_{SD}		100	375		ns
Data hold time	t_{HD}		50	125		ns
Clock pulse low width	t_{WLC}		150	250		ns
Clock pulse high width	t_{WHC}		150	250		ns
Clock cycle time	t_{WCL2}			500		ns
Clock delay time	t_{DCL1}		0	125		ns
Clock pulse width	t_{WCL1}		2	4		μs
Clock delay time	t_{DCL2}		0	125		ns
Data delay time	t_{DM}				50	ns
Data hold time	t_{HS}		2			μs
Data setup time	t_{SS}		2			μs
Signal rise time	t_r	$0.1V_{DD}$ to $0.9V_{DD}$			50	ns
Signal fall time	t_f	$0.1V_{DD}$ to $0.9V_{DD}$			50	ns



(2) Writing display control command

(V_{DD}=5V±5%, Ta=0 to +50℃)

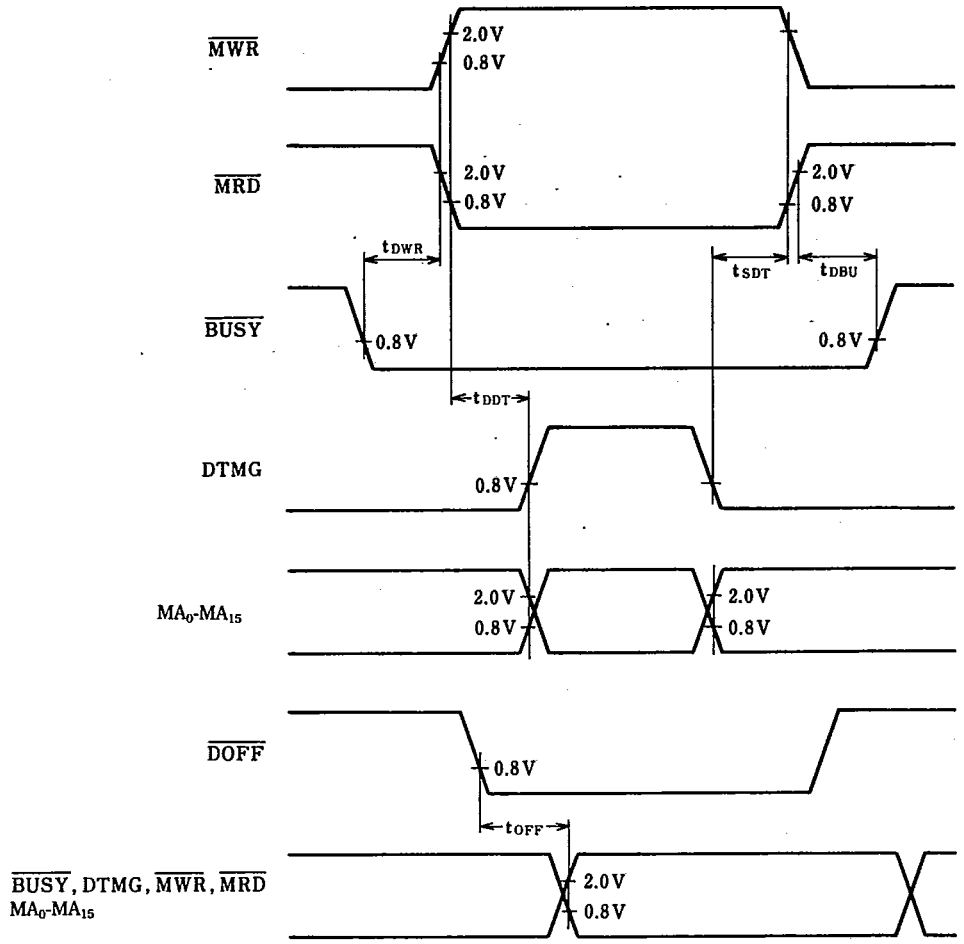
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Signal setup time	t_{SRS}		500			ns
Signal pulse width	t_{WWR}	$\overline{WR}$ and $\overline{CS}$ overlap time	220			ns
Signal hold time	t_{HRS}		30			ns
Data setup time	t_{SD}		250			ns
Data hold time	t_{HD}		30			ns



(3) Control signal timing

(V_{DD}=5V±5%, fosc=4MHz, C_L=15pF Ta=0 to +50℃)

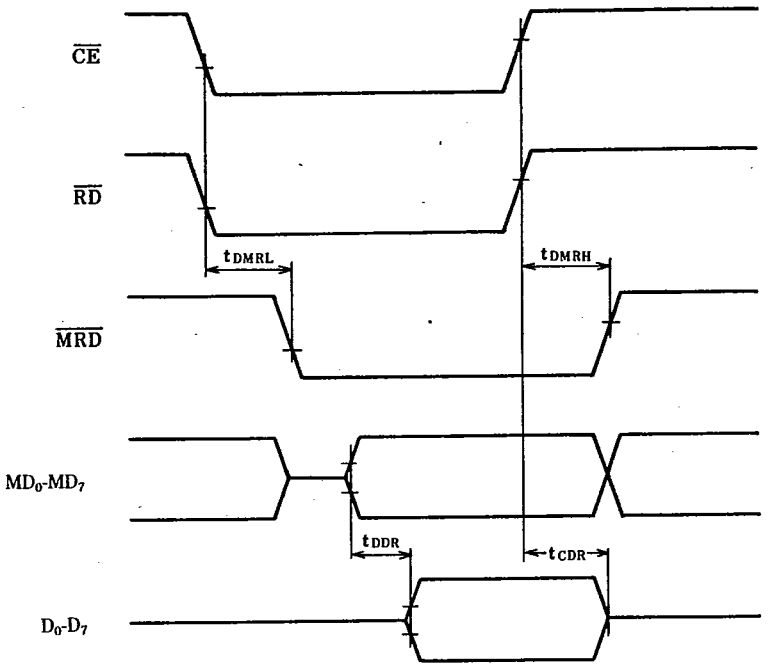
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Signal delay time	t_{DWR}		0.2	0.5		μs
Signal delay time	t_{DDT}		0.2	0.5		μs
Signal setup time	t_{SDT}		0.2	1		μs
Signal delay time	t_{DBU}		0.2	1		μs
Signal delay time	t_{OFF}				200	ns

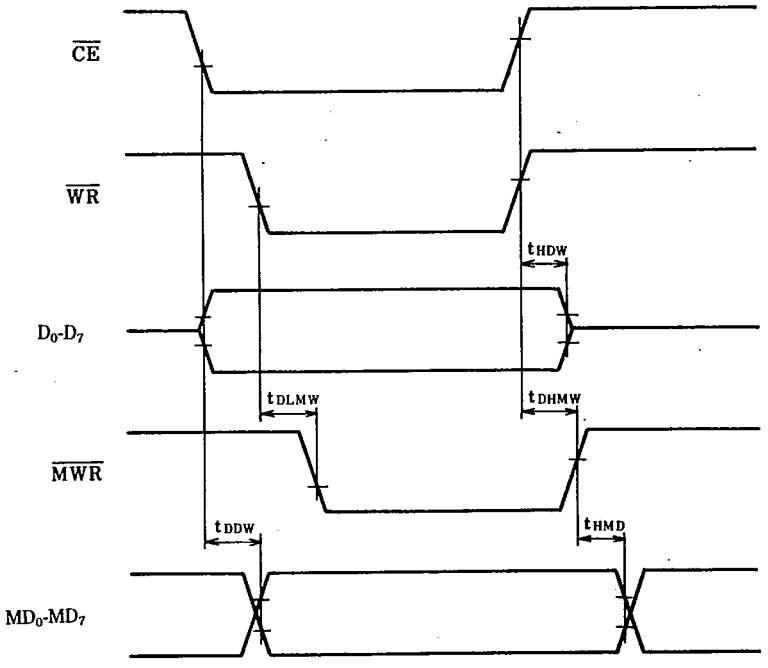


(4) Bus timing (Direct mode)

(V_{DD}=5V±5%, fosc=4MHz, C_L=15pF, Ta=0 to +50℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
MDR delay time	t_{DMRL}				150	ns
	t_{DMRH}				150	
Data delay time	t_{DDR}				150	ns
Bus switching time	t_{CDR}		0			ns
MWR delay time	t_{DLMW}				150	ns
	t_{DHMW}				150	ns
Data delay time	t_{DDW}				150	ns
Data hold time	t_{HDW}		50			ns
Data hold time	t_{HMD}		0			ns

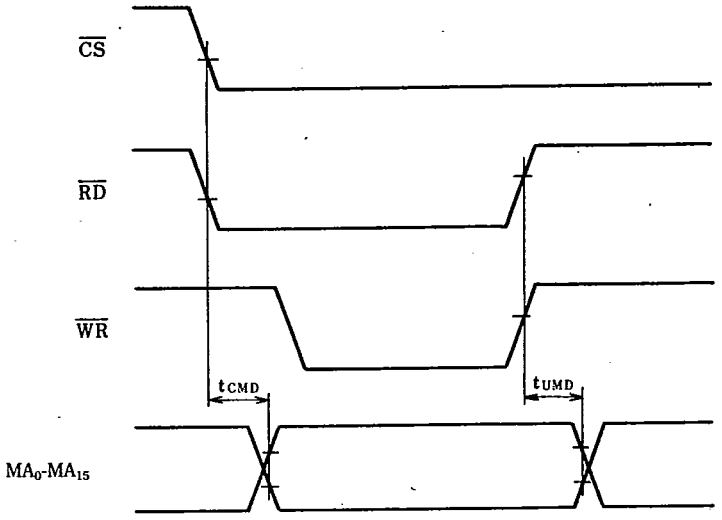

CE
RD
tDMRL
tDMRH
MRD
MD0-MD7
tDDR
tCDR
D0-D7


CE
WR
tHDW
D0-D7
tDLMW
tDHMW
MWR
tDDW
tHMD
MD0-MD7

(5) Bus timing (I/O mode)

(V_{DD}=5V±5%, fosc=4MHz, C_L=15pF, Ta=0 to +50℃)

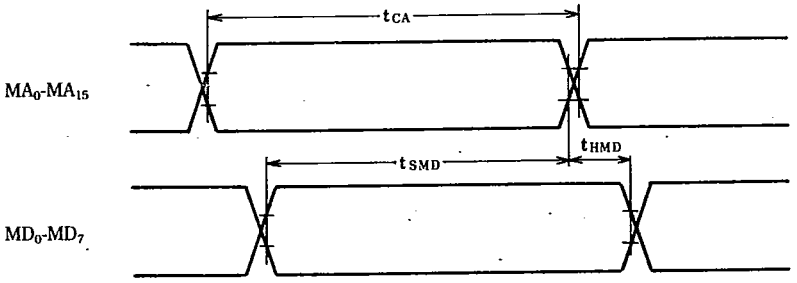
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Address delay time	t_{CMD}				150	ns
Address hold time	t_{UMD}				1	μs



(6) Display RAM access (display busy in 4-bit mode)

(V_{DD}=5V±5%, fosc=4MHz, C_L=15pF, Ta=0 to +50℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data setup time	t_{SMD}		200			ns
Data hold time	t_{HMD}		0			ns
Access cycle time	t_{CA}			500		ns



■ Display Control Commands

Display control is accomplished by writing commands and data into the command and data registers.

(1) Mode control

When writing data into the data register, write code 00H into the command register to specify the Write Mode Control register.

Register name: Mode Control register

RS	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	0	0	0
0	0	0	0	MODE DATA				

Data contents

D4	1: 4-bit parallel output	0: 1-bit serial output
D3	1: Character mode	0: Graphic mode
D2	1: Display ON	0: Display OFF
D1	1: Cursor blink (character blink when cursor is off.)	
D0	1: Cursor ON	0: Cursor OFF

(2) Setting character pitch

Register name: Character Pitch register

RS	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	0	0	1
0	(VP-1)				0	0	(HP)	

VP: Vertical pitch in character mode. Invalid for Graphic mode.
HP: Horizontal pitch in character mode. Invalid for Graphic mode.

The HP can take on any of the following three values. However, when in the 4-bit parallel output mode, the horizontal character pitch is fixed at 8.

HP	D1	D0	
5	0	1	Horizontal character pitch 5
6	1	0	Horizontal character pitch 6
8	0	0	Horizontal character pitch 8

(3) Setting the number of characters per row

Register name: Characters Per Row register

RS	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	0	1	0
0	0	(HN-1)						

HN: Specifies the number of characters per row when in the character mode, and the number of bytes per row when in the Graphic mode. When in the 4-bit parallel output mode, HN should be set to a multiple of four (4).

Nunmber of pixels per row NX:
NX=HP × HN in Character mode
NX=8 × HN in Graphic mode

(4) Setting display duty

Register name: Display register

RS	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	0	1	1
0	(NY-1)							

NY: Display duty —— 1/(32-256)

(5) Setting cursor position

Register name: Cursor Position register

RS	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	1	0	0
0	0	0	0	0	(CP-1)			

CP: Specifies the row on which the cursor is located in Character mode. The horizontal length of the cursor is identical to the HP.

(6) Setting lower byte of display start address (upper screen)

Register name: Display Start Address register

RS	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	1	0	0	0
0	Lower byte of start address							

(7) Setting upper byte of display start address (upper screen)

Register name: Display Start Address register

RS	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	1	0	0	1
0	Upper byte of start address							

This command sets the display start address for the upper section of the screen. The display start address refers to the RAM location in which the data to be displayed in the upper left corner of the screen is stored.

(8) Setting lower byte of display start address (lower screen)

Register name: Display Start Address register

RS	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	1	0	1
0	Lower byte of start address							

(9) Setting upper byte of display start address (lower screen)

Register name: Display Start Address register

RS	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	1	1	0
0	Upper byte of start address							

This command sets the display start address for the lower section of the screen. The display start address refers to the RAM location in which the data to be displayed in the upper left corner of the lower section of the screen is stored.

3

(10) Setting lower byte of cursor address
Register name: Cursor Address register

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	0	1	0	1	0
0	Lower byte of cursor address							

(11) Setting upper byte of cursor address
Register name: Cursor Address register

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	0	1	0	1	1
0	Upper byte of cursor address							

This command sets cursor address data into the cursor address counter.

(12) Setting latch pulse period
Register name: Latch Pulse Period register

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	0	0	1	1	1
0	0	(NLP−1)						

NLP: HN + 1 ≦ NLP ≦ 128 when in serial mode.
HN/4 + 1 ≦ NLP ≦ 128 when in 4-bit mode.
The display frequency f_d is related with the latch pulse period NLP by the following formula:
$f_d = 1/(8NLP.\ TXS.\ NY)$
TXS: Shift clock period
TXS = 500 ns when OSC frequency is 4 MHz.

(13) Setting display RAM access mode

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	0	1	1	0	0
0	DATA							

I/O mode is selected by writing $0C_H$ into the command register. When BUSY = 1, the display RAM location specified by the Cursor Address register can be accessed through DI_0-DI_7 for read or write operations.

The LR3692 also permits direct display RAM access using the address data furnished from the CPU. In either case the value of the Cursor Address register is incremented each time the display RAM is accessed.

■ System Configuration Example

(1) Interface with CPU

As shown in Figs. 1 and 2, the LR3692 (LCDC) is connected to the standard bus of the Z80-type CPU, which controls data comunication with the CPU.

If the $\overline{CS}$ is at low and RS is at high, the command register within the LCDC is specified and the data on the data bus is written in. The write timing is determined by the $\overline{WR}$ signal. If the $\overline{CS}$ is at low and RS is at high, the contents of the LCDC's internal register requested by the command register cannot be read.

The $\overline{CE}$, $\overline{BUSY}$, $\overline{DOFF}$, and DTMG signals are used for CPU access to the display RAM.

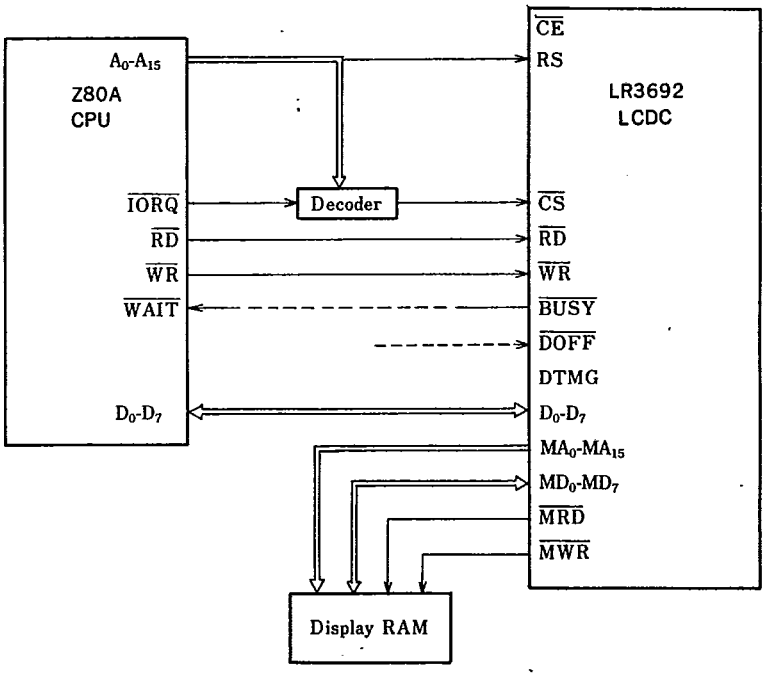


Fig. 1 Interface with CPU(I/O mode)

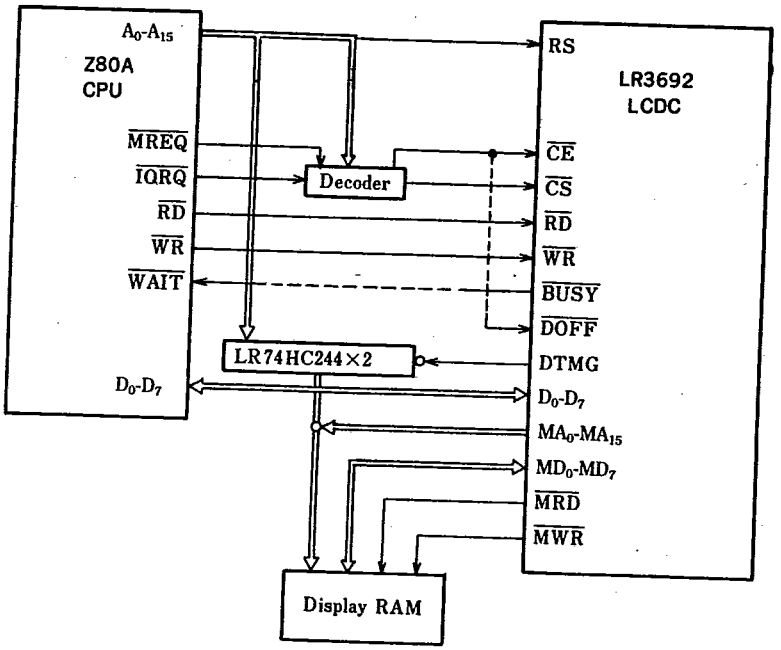


Fig. 2 Interface with CPU (Direct mode)

(2) CPU access to display RAM

CPU access to the display RAM includes the I/O mode which is made through the LCDC, and the Direct mode which is directly performed from the CPU.

① I/O mode A sample system configuration for I/O mode access is shown in Fig. 1. A value for $0C_H$ is first set into the command register. If the $\overline{BUSY}$ is high, $\overline{CS}$ is low, and RS is low, the $\overline{RD}$, $\overline{WR}$, and D_0-D_7 lines are linked to the $\overline{MRD}$, $\overline{MWR}$, and MD_0-MD_7 lines, respectively. At this time the value of the Cursor Address register is output at the MA_0-MA_{15} pins. The Cursor Address register is incremented at the rising edge of the $\overline{RD}$ or $\overline{WR}$ signal. The $\overline{BUSY}$ line is set to high during the fly-back period in which the LCDC does not access the display RAM. Setting the $\overline{DOFF}$ to low causes the $\overline{BUSY}$ to be set to high, making the display RAM accessible at any timing. At this time, the LCD display is turned off.

② Direct mode A sample system configuration for Direct mode access is shown in Fig. 2. The Direct mode is selected if the value of the command register is anything but $0C_H$. If $\overline{BUSY}$ is high and $\overline{CE}$ is low, the $\overline{RD}$, $\overline{WR}$ and D_0-D_7 pins are linked to the $\overline{MRD}$, $\overline{MWR}$, and MD_0-MD_7 lines, respectively. At this time the DTMG is set at low and the MA_0-MA_{15} pins are set to high impedance, to transfer the address specified of the CPU directly to the display RAM. The Cursor Address register is incremented at the rising edge of the $\overline{RD}$ or $\overline{WR}$ signal. The functions of the $\overline{BUSY}$ and $\overline{DOFF}$ signals are identical to those in the I/O mode.

Note: In either mode the $\overline{BUSY}$ signal is output only when the CPU is accessing the display RAM. (When $\overline{CE}=0$ in Direct mode; when $\overline{CS}=0$, RS=0 and the command register value is $0C_H$ in I/O mode.) The $\overline{BUSY}$ is set to high in all other cases.

■ LCD Control

(1) Graphic mode

The Graphic mode is selected by the Mode Control register value. In this mode each bit of the display RAM corresponds to each pixel on the LCD screen.

① Screen configuration The numbers of pixels per row and per column are determined by the values of the Character-Per-Row register and Duty register.

No. of pixels per row: HN×8, HN=16 to 128
No. of pixels per column: NY×2, NY=32 to 256
(When both the upper and lower sections of the screen are used.)

② Display start address The display start address can be specified by 16-bit data for the first location of the display RAM area.
Independent specification for the upper and lower sections of the screen is possible. Further, the utilization of display start address makes page con-

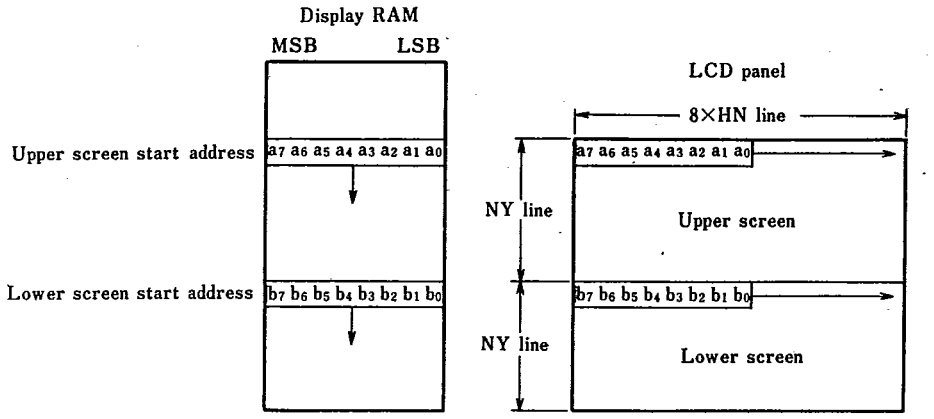


Fig. 3 Screen configuration (Graphic mode)

trol and screen scroll possible.

(2) Character mode

The Character mode is specified by the value of the Mode Control register. In this mode pixel patterns are displayed by combining character codes of the display RAM with the corresponding character patterns of the character generator ROM (CGROM).

① Screen configuration The numbers of characters per row and per column are determined by the content of the Character-Per Row register, Duty register, and Character Pitch register.

No. of characters per row: HN=16 to 128
No. of characters per column: NY×2/VVP, NY=32×256
(When the upper and lower sections of the screen are used.)

The numbers of pixels per row and per column are determined as follows:

No. of pixels per row: HHY×2

② Character font The character font is specified by the value of the Character Pitch register.

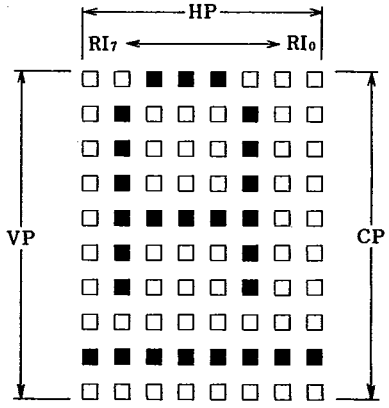
Horizontal pitch: HP=5, 6, 8
Vertical pitch: VP=1~16

Fig. 4 shows an example of character font. If HP=5 or 6, the LSB side of the RI_0-RI_7 is invalid.

③ Cursor display The cursor display mode is determined by the value of the Mode Control register. The cursor position is specified by the value of Cursor Address register. Since the character code address on the display RAM is specified for cursor position specification, screen scrolling is accompained by cursor scrolling.,

The cursor position in a character font is specified by the Cursor Position register.

④ Cursor blink Cursor or character blinking is controlled by the Mode Control register.



CGROM address			
MA_{15}	MA_{14}	MA_{13}	MA_{12}
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1

Fig. 4 Example of character font (HP=8, VP=10, CP=9)

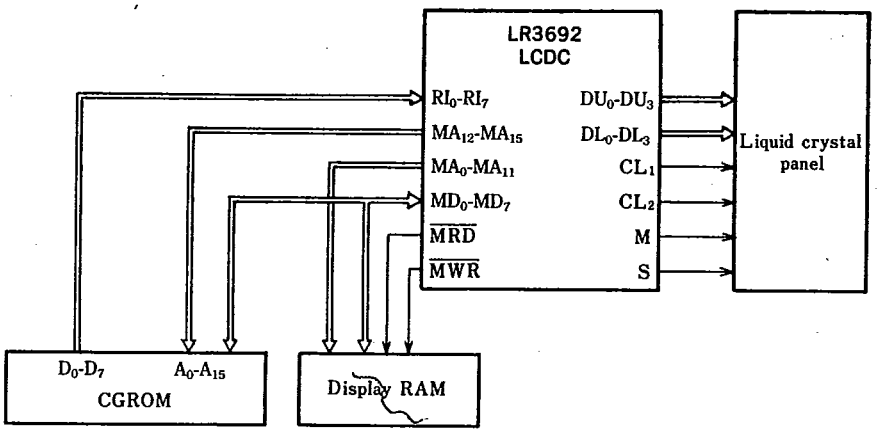


Fig. 5 Connections to CGROM and LCD panel

Blinking is performed for approx. 1H(64 frames) at 1/2 duty.

(3) Parameter setting

① Display frequency The LR3692 uses the two-frame AC display system.

The display frequency is determined by Display Duty and the value of the Latch Pulse Period register.

One frame period: $T_d = 8NLP \cdot TXS \cdot NY$

Display frequency: $f_d = 1/T_d$

(TXS=500 ns when OSC frequency is 4 MHz.)

② Flyback period The LCDC does not access the display RAM during flyback period.

Flyback period TDIS:

When in Serial mode,

$TDIS = \{8(NLP-1)-8HN\} \cdot TXS$

When in 4-bit mode,

$TDIS = \{8(NLP-1)-2HN\} \cdot TXS$

Fig. 6 Flyback period