Dual Decade Counter

The TC74HC390A is a high speed CMOS DUAL DECADE COUNTER LATCH fabricated with silicon gate C^2MOS technology.

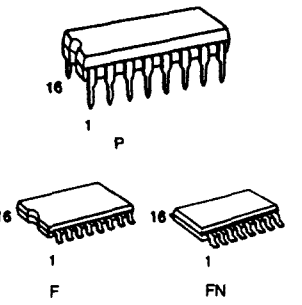
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

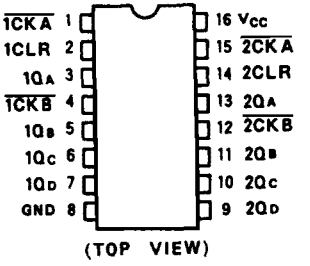
It consists of two independent 4-bit counters, each composed of a divide-by-two and a divide-by-five counter. The divide-by-two counter is incremented on the negative going transition of clock A($\overline{CKA}$). The divided-by-five counter is incremented on the negative going transition of clock B($\overline{CKB}$). The counter can be cascaded to form decade, biquinary, or various combinations up to a divide-by-100 counter. When the CLEAR input is set high, the Q outputs are set to low independent of the clock inputs.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

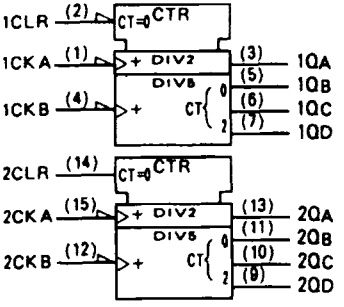
Features

- High Speed: f_{MAX} = 84MHz(Typ.) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 4μA(Max.) at Ta = 25°C
- High Noise Immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC}(Min.)
- Output Drive Capability: 10 LSTTL Loads
- Symmetrical Output Impedance: $|I_{OH}| = I_{OL}$ = 4mA(Min.)
- Balanced Propagation Delays: $t_{pLH} = t_{pHL}$
- Wide Operating Voltage Range: V_{CC}(opr) = 2V ~ 6V
- Pin and Function Compatible with 74LS390

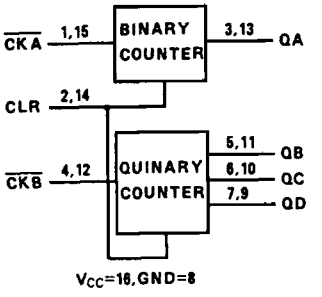




Pin Assignment



IEC Logic Symbol

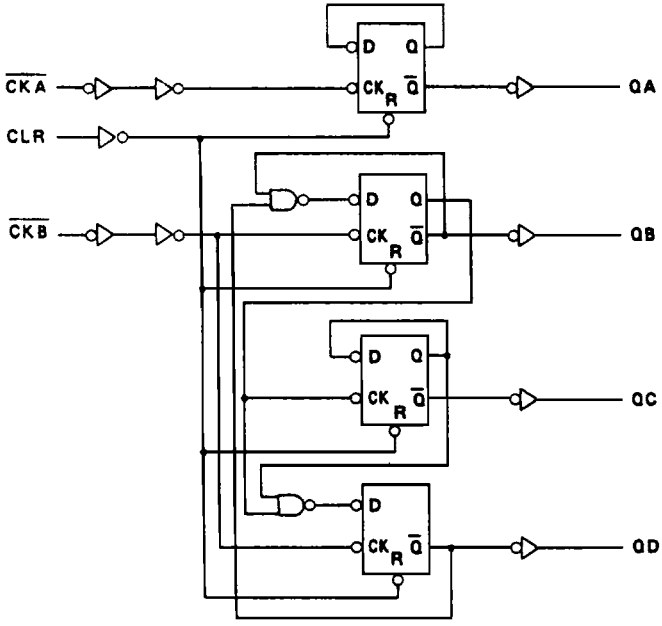


Block Diagram

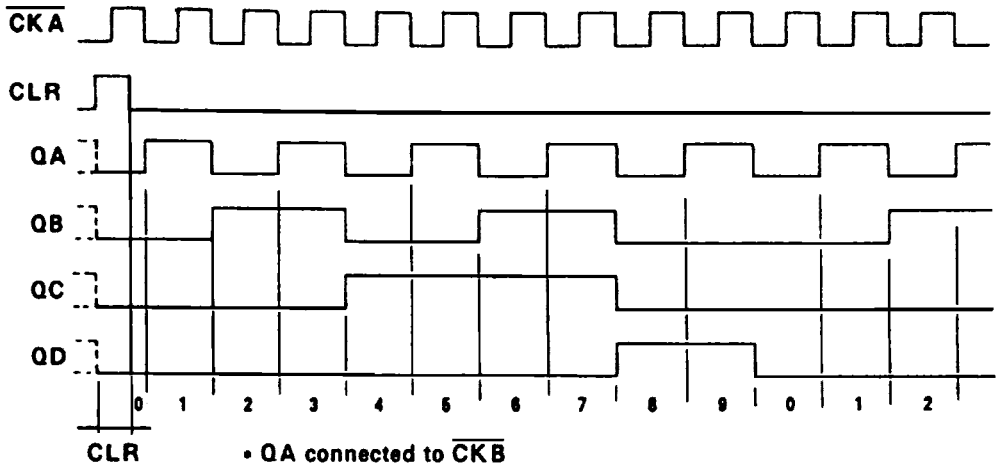
Truth Table

Inputs			Outputs			
$\overline{CKA}$	$\overline{CKB}$	CLR	QA	QB	QC	QD
X	X	H	L	L	L	L
↓	X	L	Binary Count Up			
	↓	L	Quinary Count Up			

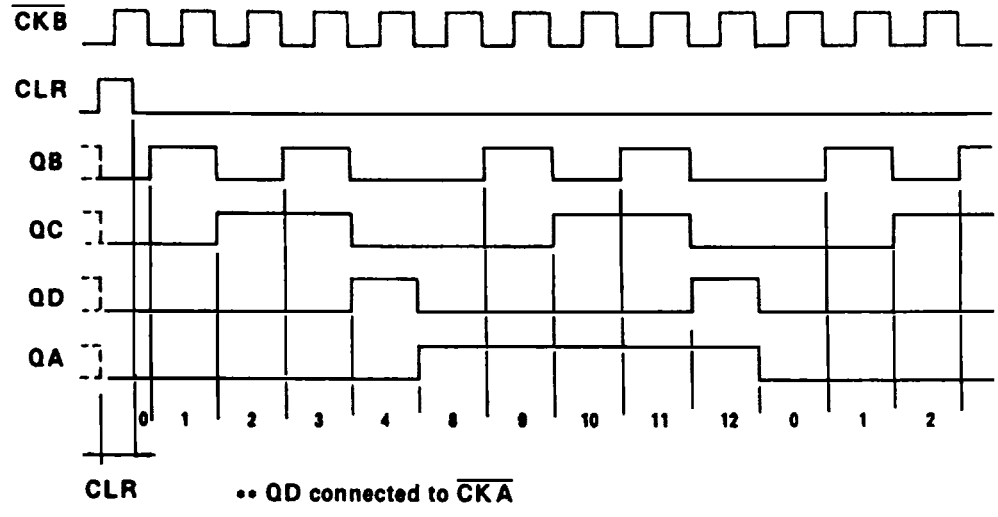
X: Don't Care



Logic Diagram



(1) BCD Count Sequence*



(2) Bi-Quinary Count Sequence**

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage Range	V_{CC}	-0.5~7	V
DC Input Voltage	V_{IN}	-0.5 ~ V_{CC} + 0.5	V
DC Output Voltage	V_{OUT}	-0.5 ~ V_{CC} + 0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temperature 10sec	T_L	300	°C

*500mW in the range of Ta = -40°C ~ 65°C. From Ta = 65°C to 85°C a derating factor of -10mW/°C shall be applied until 300mW.

Recommended Operating Conditions

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	-40 ~ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC} = 2.0V) 0 ~ 500(V_{CC} = 4.5V) 0 ~ 400(V_{CC} = 6.0V)	ns

DC Electrical Characteristics

Parameter	Symbol	Test Condition			Ta = 25°C			Ta = -40 ~ 85°C		Unit
				V_{CC}	Min.	Typ.	Max.	Min.	Max.	
High-Level Input Voltage	V_{IH}	–		2.0 4.5 6.0	1.5 3.15 4.2	– – –	– – –	1.5 3.15 4.2	– – –	V
Low-Level Input Voltage	V_{IL}	–		2.0 4.5 6.0	– – –	– – –	0.5 1.35 1.8	– – –	0.5 1.35 1.8	V
High-Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = -20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	– – –	1.9 4.4 5.9	– – –	V
			I_{OH} = -4 mA I_{OH} = -5.2mA	4.5 6.0	4.18 5.68	4.31 5.80	–	4.13 5.63	–	
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20μA	2.0 4.5 6.0	– – –	0.0 0.0 0.0	0.1 0.1 0.1	– – –	0.1 0.1 0.1	V
			I_{OL} = 4 mA I_{OL} = 5.2mA	4.5 6.0	– –	0.17 0.18	0.26 0.26	– –	0.33 0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	–	–	±0.1	–	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	–	–	4.0	–	40.0	

Timing Requirements (Input $t_r = t_f = 6ns$)

Parameter	Symbol	Test Condition		Ta = 25°C		Ta = -40 ~ 85°C	Unit
			V_{CC}	Typ.	Limit	Limit	
Minimum Pulse Width ($\overline{CLOCK}$)	$t_{W(H)}$ $t_{W(L)}$	–	2.0	–	75	95	ns
			4.5	–	15	19	
			6.0	–	13	16	
Minimum Pulse Time (CLR)	$t_{W(H)}$	–	2.0	–	75	95	
			4.5	–	15	19	
			6.0	–	13	16	
Minimum Removal Time	t_{rem}	–	2.0	–	25	30	
			4.5	–	5	6	
			6.0	–	5	5	
Clock Frequency ($\overline{CKA}$)	f	–	2.0	–	6	5	
			4.5	–	32	26	
			6.0	–	38	31	
Clock Frequency ($\overline{CKB}$)	f	–	2.0	–	6	5	
			4.5	–	31	25	
			6.0	–	36	29	

AC Electrical Characteristics ($C_L = 15pF$, $V_{CC} = 5V$, Ta = 25°C)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Output Transition Time	t_{TLH} t_{THL}	–	–	4	8	ns
Propagation Delay Time ($\overline{CKA}$-QA)	t_{pLH} t_{pHL}	–	–	10	20	
Propagation Delay Time ($\overline{CKA}$-QC)	t_{pLH} t_{pHL}	QA connected to $\overline{CKB}$	–	29	51	
Propagation Delay Time ($\overline{CKB}$-QB, QD)	t_{pLH} t_{pHL}	–	–	12	22	
Propagation Delay Time ($\overline{CKB}$-QC)	t_{pLH} t_{pHL}	–	–	17	32	
Propagation Delay Time (CLR-Qn)	t_{pLH} t_{pHL}	–	–	12	26	
Maximum Clock Frequency ($\overline{CKA}$)	f_{MAX}	–	35	84	–	MHz
Maximum Clock Frequency ($\overline{CKB}$)	f_{MAX}	–	33	65	–	

AC Electrical Characteristics (C_L = 50pF, Input $t_r = t_f$ = 6ns)

Parameter	Symbol	Test Condition		Ta = 25°C			Ta = -40~85°C		Unit
			V_{CC}	Min.	Typ.	Max.	Min.	Max.	
Output Transition Time	t_{TLH} t_{THL}	–	2.0 4.5 6.0	– – –	30 8 7	75 15 13	– – –	95 19 16	ns
Propagation Delay Time ($\overline{CKA}$-QA)	t_{pLH} t_{pHL}	–	2.0 4.5 6.0	– – –	39 13 11	120 24 20	– – –	150 30 26	
Propagation Delay Time ($\overline{CKA}$-QC)	t_{pLH} t_{pHL}	QA connected to $\overline{CKB}$	2.0 4.5 6.0	– – –	102 34 29	290 58 49	– – –	365 73 62	
Propagation Delay Time ($\overline{CKB}$-QB, QD)	t_{pLH} t_{pHL}	–	2.0 4.5 6.0	– – –	45 15 13	130 26 22	– – –	165 33 28	
Propagation Delay Time ($\overline{CKB}$-QC)	t_{pLH} t_{pHL}	–	2.0 4.5 6.0	– – –	63 21 18	185 37 31	– – –	165 33 28	
Propagation Delay Time (CLR-Qn)	t_{pLH} t_{pHL}	–	2.0 4.5 6.0	– – –	45 15 13	150 30 26	– – –	190 38 33	
Maximum Clock Frequency ($\overline{CKA}$)	f_{MAX}	–	2.0 4.5 6.0	6 32 38	20 77 90	– – –	5 26 31	– – –	MHz
Maximum Clock Frequency ($\overline{CKB}$)	f_{MAX}	–	2.0 4.5 6.0	6 31 36	15 60 70	– – –	5 25 29	– – –	
Input Capacitance	C_{IN}	–		–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)	–		–	44	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation:

$I_{CC(opr)} = C_{PD} \bullet V_{CC} \bullet f_{IN} + I_{CC}/2$ Counter