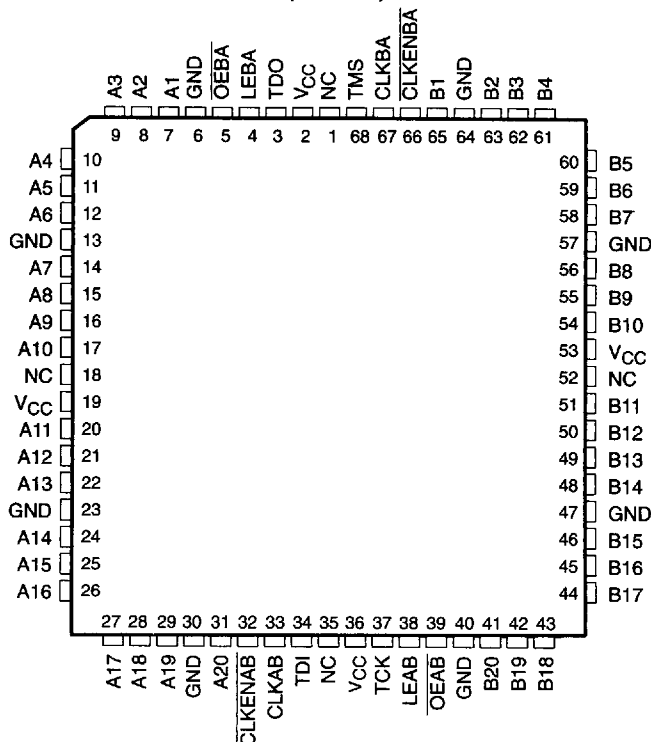
SN54ABT18504A, SN74ABT18504A SCAN TEST DEVICES WITH 20-BIT UNIVERSAL BUS TRANSCEIVERS

SCBS165 – AUGUST 1993

- **Members of the Texas Instruments *SCOPE*™ Family of Testability Products**
- **Members of the Texas Instruments *Widebus*™ Family**
- **Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture**
- ***UBT*™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode**
- **Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors**
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **One Boundary-Scan Cell per I/O Architecture Improves Scan Efficiency**
- ***SCOPE*™ Instruction Set**
  - **IEEE Standard 1149.1-1990 Required Instructions and P1149.1A CLAMP and HIGHZ**
  - **Parallel Signature Analysis at Inputs**
  - **Pseudo-Random Pattern Generation From Outputs**
  - **Sample Inputs/Toggle Outputs**
  - **Binary Count From Outputs**
  - **Device Identification**
  - **Even-Parity Opcodes**
- **Packaged in 64-Pin Plastic Thin Quad Flat Packages Using 0.5-mm Center-to-Center Spacings and 68-Pin Ceramic Quad Flat Packages Using 25-mil Center-to-Center Spacings**

PRODUCT PREVIEW

SN54ABT18504A . . . HV PACKAGE (TOP VIEW)



NC – No internal connection

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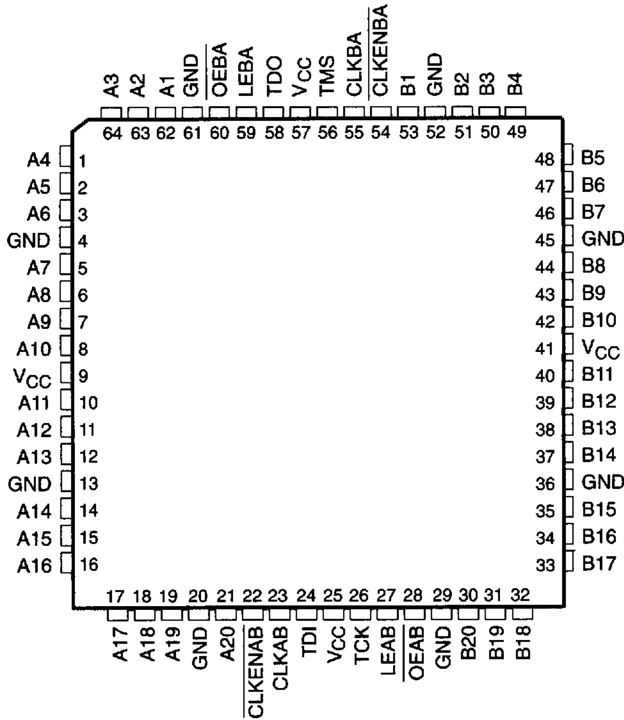
SCAN TEST DEVICES WITH
20-BIT UNIVERSAL BUS TRANSCEIVERS



PRODUCT PREVIEW

description

The SN54ABT18504A and SN74ABT18504A scan test devices with 20-bit universal bus transceivers are members of the Texas Instruments SCOPE™ testability IC family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

In the normal mode, these devices are 20-bit universal bus transceivers that combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, or clocked modes. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary test cells. Activating the TAP in the normal mode does not affect the functional operation of the SCOPE™ universal bus transceivers.

Data flow in each direction is controlled by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$), latch-enable (LEAB and LEBA), clock-enable ($\overline{CLKENAB}$ and $\overline{CLKENBA}$), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A-bus data is latched while $\overline{CLKENAB}$ is high and/or CLKAB is held at a static low or high logic level. Otherwise, if LEAB is low and $\overline{CLKENAB}$ is low, A-bus data is stored on a low-to-high transition of CLKAB. When $\overline{OEAB}$ is low, the B outputs are active. When $\overline{OEAB}$ is high, the B outputs are in the high-impedance state. B-to-A data flow is similar to A-to-B data flow but uses the $\overline{OEBA}$, LEBA, $\overline{CLKENBA}$, and CLKBA inputs.

In the test mode, the normal operation of the SCOPE™ universal bus transceivers is inhibited, and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry performs boundary scan test operations according to the protocol described in IEEE Standard 1149.1-1990.

description (continued)

Four dedicated test pins are used to observe and control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry can perform other testing functions such as parallel signature analysis on data inputs and pseudo-random pattern generation from data outputs. All testing and scan operations are synchronized to the TAP interface.

Improved scan efficiency is accomplished through the adoption of a one boundary-scan cell (BSC) per I/O pin architecture. This architecture is implemented in such a way as to capture test data of most interest. A PSA/COUNT instruction is also included to ease the testing of memories and other circuits where a binary count addressing scheme is useful.

The SN54ABT18504A is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT18504A is characterized for operation from –40°C to 85°C.

FUNCTION TABLE†
(normal mode, each register)

INPUTS					OUTPUT
$\overline{OEAB}$	LEAB	$\overline{CLKENAB}$	CLKAB	A	B
L	L	L	L	X	B_0‡
L	L	L	↑	L	L
L	L	L	↑	H	H
L	L	H	X	X	B_0‡
L	H	X	X	L	L
L	H	X	X	H	H
H	X	X	X	X	Z

† A-to-B data flow is shown. B-to-A data flow is similar but uses $\overline{OEBA}$, LEBA, $\overline{CLKENBA}$, and CLKBA.
‡ Output level before the indicated steady-state input conditions were established.

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functional block diagram

Boundary-Scan Register
$\overline{\text{CLKENAB}}$ 22
LEAB 27
CLKAB 23
$\overline{\text{OEAB}}$ 28
$\overline{\text{CLKENBA}}$ 54
LEBA 59
CLKBA 55
$\overline{\text{OEBA}}$ 60
1 of 20 Channels
A1 62
C1
1D
C1
1D
C1
1D
C1
1D
53 B1
Bypass Register
Boundary-Control Register
Identification Register
Instruction Register
V_{CC}
TDI 24
V_{CC}
TMS 56
TCK 26
TAP Controller
58 TDO

Pin numbers shown are for the PM package.

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Terminal Functions

PIN NAME	DESCRIPTION
A1–A20	Normal-function A-bus I/O ports. See function table for normal-mode logic.
B1–B20	Normal-function B-bus I/O ports. See function table for normal-mode logic.
CLKAB, CLKBA	Normal-function clock inputs. See function table for normal-mode logic.
$\overline{CLKENAB}$, $\overline{CLKENBA}$	Normal-function clock enables. See function table for normal-mode logic.
GND	Ground
LEAB, LEBA	Normal-function latch enables. See function table for normal-mode logic.
$\overline{OEAB}$, $\overline{OEBA}$	Normal-function output enables. See function table for normal-mode logic.
TCK	Test clock. One of four pins required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous to the test clock. Data is captured on the rising edge of TCK and outputs change on the falling edge of TCK.
TDI	Test data input. One of four pins required by IEEE Standard 1149.1-1990. The test data input is the serial input for shifting data through the instruction register or selected data register. An internal pullup forces TDI to a high level if left unconnected.
TDO	Test data output. One of four pins required by IEEE Standard 1149.1-1990. The test data output is the serial output for shifting data through the instruction register or selected data register.
TMS	Test mode select. One of four pins required by IEEE Standard 1149.1-1990. The test mode select input directs the device through its test access port (TAP) controller states. An internal pullup forces TMS to a high level if left unconnected.
V_{CC}	Supply voltage

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... –0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) .... –0.5 V to 7 V
Input voltage range, V_I (I/O ports) (see Note 1) .... –0.5 V to 5.5 V
Voltage range applied to any output in the high state or power-off state, V_O .... –0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT18504A .... 96 mA
SN74ABT18504A .... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) .... –18 mA
Output clamp current, I_{OK} ($V_O < 0$) .... –50 mA
Continuous current through V_{CC} .... 576 mA
Continuous current through GND .... 1152 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2) .... 885 mW
Storage temperature range .... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings can be exceeded if the input and output clamp-current ratings are observed.
2. For the SN74ABT18504A (PM package), the power derating factor for ambient temperatures greater than 55°C is –10.5 mW/°C.

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recommended operating conditions

		SN54ABT18504A		SN74ABT18504A		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–24		–32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		10		10	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 3)

PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT18504A		SN74ABT18504A		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = –18 mA					–1.2		–1.2		–1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = – 3 mA			2.5			2.5		2.5		V
	V_{CC} = 5 V, I_{OH} = – 3 mA			3			3		3		
	V_{CC} = 4.5 V, I_{OH} = – 24 mA			2			2				
	V_{CC} = 4.5 V, I_{OH} = – 32 mA			2‡					2		
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 48 mA				0.55		0.55			V
		I_{OL} = 64 mA				0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND		CLK, $\overline{CLKEN}$, LE, $\overline{OE}$, TCK			±1		±1		±1	μA
			A or B ports			±100		±100		±100	
I_{IH}	V_{CC} = 5.5 V, V_I = V_{CC}		TDI, TMS			10		10		10	μA
I_{IL}	V_{CC} = 5.5 V, V_I = GND		TDI, TMS			–150		–150		–150	μA
$I_{I(hold)}$	V_{CC} = 4.5 V	V_I = 0.8 V	A or B ports						100		μA
		V_I = 2 V							–100		
I_{OZH}§	V_{CC} = 5.5 V, V_O = 2.7 V					50		50		50	μA
I_{OZL}§	V_{CC} = 5.5 V, V_O = 0.5 V					–50		–50		–50	μA
I_{OZPU}	V_{CC} = 0 to 2 V, V_O = 2.7 V or 0.5 V		$\overline{OE}$ = 0.8 V			±50		±50		±50	μA
I_{OZPD}	V_{CC} = 2 V to 0, V_O = 2.7 V or 0.5 V		$\overline{OE}$ = 0.8 V			±50		±50		±50	μA
I_{off}	V_{CC} = 0, V_I or V_O ≤ 4.5 V					±100		±450		±100	μA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V		Outputs high			50		50		50	μA
I_O¶	V_{CC} = 5.5 V, V_O = 2.5 V			–50	–110	–200	–50	–200	–50	–200	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	A or B ports	Outputs high		2	3		3		3	mA
			Outputs low		18	24		24		24	
			Outputs disabled		1	1.5		1.5		1.5	
ΔI_{CC}#	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND					1.5		1.5		1.5	mA
C_i	V_I = 2.5 V or 0.5 V		Control inputs		3						pF
C_{io}	V_O = 2.5 V or 0.5 V		A or B ports		10						pF
C_o	V_O = 2.5 V or 0.5 V		TDO		8						pF

NOTE 3: Product preview specifications are design goals only and are subject to change without notice.
† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ The parameters I_{OZH} and I_{OZL} include the input leakage current.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Note 3 and Figure 1)

				SN54ABT18504A		SN74ABT18504A		UNIT
				MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	CLKAB or CLKBA		0	100	0	100	MHz
t_w	Pulse duration	CLKAB or CLKBA high or low				4		ns
		LEAB or LEBA	CLK high or low			3.5		
t_{su}	Setup time	A before CLKAB↑ or B before CLKBA↑				4		ns
		A before LEAB↓ or B before LEBA↓	CLK high			3.5		
			CLK low			2		
		$\overline{\text{CLKEN}}$ before CLK↑				4		
t_h	Hold time	A after CLKAB↑ or B after CLKBA↑				0		ns
		A after LEAB↓ or B after LEBA↓	CLK high or low			2		
		$\overline{\text{CLKEN}}$ after CLK↑				0		

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Note 3 and Figure 1)

			SN54ABT18504A		SN74ABT18504A		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	TCK	0	50	0	50	MHz
t_w	Pulse duration	TCK high or low			8		ns
t_{su}	Setup time	A, B, CLK, LE, or $\overline{\text{OE}}$ before TCK↑			4.5		ns
		TDI before TCK↑			7.5		
		TMS before TCK↑			3		
t_h	Hold time	A, B, CLK, LE, or $\overline{\text{OE}}$ after TCK↑			0.5		ns
		TDI after TCK↑			0.5		
		TMS after TCK↑			0.5		
t_d	Delay time	Power up to TCK↑			50		ns
t_r	Rise time	V_{CC} power up			1		µs

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Note 3 and Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT18504A		SN74ABT18504A		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	CLKAB or CLKBA		100	130		100		100		MHz
t_{PLH}	A or B	B or A						2	6	ns
t_{PHL}								2	6.5	
t_{PLH}	CLKAB or CLKBA	B or A						2.5	6.8	ns
t_{PHL}								2.5	6.5	
t_{PLH}	LEAB or LEBA	B or A						2.5	7.1	ns
t_{PHL}								2.5	7.2	
t_{PZH}	$\overline{OEAB}$ or $\overline{OEBA}$	B or A						2	7	ns
t_{PZL}								2.5	8	
t_{PHZ}	$\overline{OEAB}$ or $\overline{OEBA}$	B or A						3	8.8	ns
t_{PLZ}								2.5	7.3	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Note 3 and Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT18504A		SN74ABT18504A		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	TCK		50	90		50		50		MHz
t_{PLH}	TCK↓	A or B						2.5	13.5	ns
t_{PHL}								2.5	12.5	
t_{PLH}	TCK↓	TDO						2	5.6	ns
t_{PHL}								2	6.5	
t_{PZH}	TCK↓	A or B						4.5	13.8	ns
t_{PZL}								5	14.5	
t_{PZH}	TCK↓	TDO						2	7	ns
t_{PZL}								3	7.5	
t_{PHZ}	TCK↓	A or B						4	17	ns
t_{PLZ}								3.5	16	
t_{PHZ}	TCK↓	TDO						3	7.5	ns
t_{PLZ}								3	7.5	

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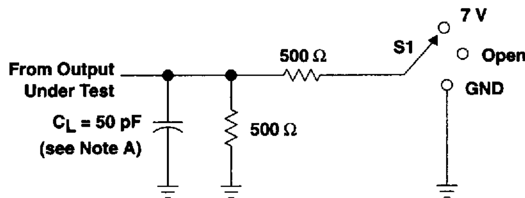
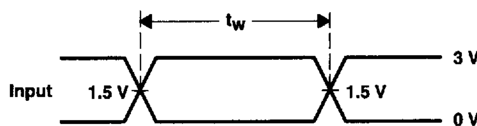
PARAMETER MEASUREMENT INFORMATION

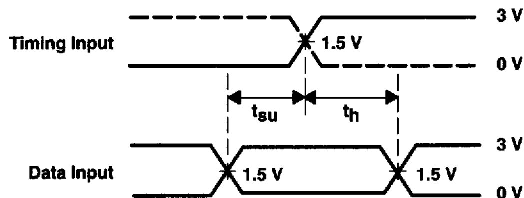


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

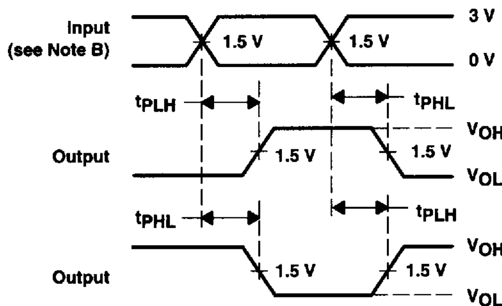
LOAD CIRCUIT FOR OUTPUTS



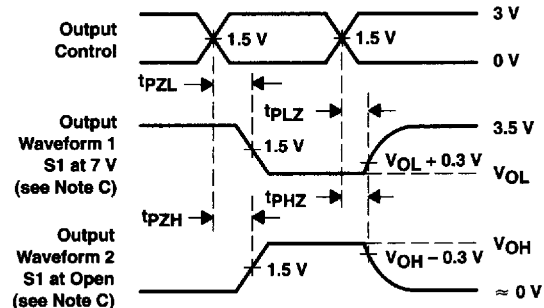
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES:
A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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