Standard Products

UT8ER1M32 32Megabit SRAM MCM
UT8ER2M32 64Megabit SRAM MCM
UT8ER4M32 128Megabit SRAM MCM

Preliminary
Data Sheet

December 16, 2009

FEATURES

- 20ns Read, 10ns Write maximum access times available
- Functionally compatible with traditional 1M, 2M and 4M x 32 SRAM devices
- CMOS compatible input and output levels, three-state bidirectional data bus
  - I/O Voltages 2.3V to 3.6V, 1.7V to 2.0Vcore
- Available densities:
  - UT8ER1M32: 33, 554, 432 bits
  - UT8ER2M32: 67, 108, 864 bits
  - UT8ER4M32: 134, 217, 728 bits
- Operational environment:
  - Total-dose: 100 krad(Si)
  - SEL Immune: 111MeV-cm^2/mg
  - SEU error rate = 6.0x10^{-16} errors/bit-day assuming geosynchronous orbit, Adam's 90% worst environment, and 6600ns default Scrub Rate Period (=97% SRAM availability)
- Packaging option:
  - 132-lead ceramic quad flatpack
- Standard Microelectronics Drawing:
  - UT8ER1M32: 5962-10202
  - UT8ER2M32: 5962-10203
  - UT8ER4M32: 5962-10204
  - QML Q, Q+ and V pending

INTRODUCTION

The UT8ER1M32, UT8ER2M32, and UT8ER4M32 are high performance CMOS static RAM multichip modules (MCMs) organized as two, four or eight individual 524,288 words x 32 bits respectively. Easy memory expansion is provided by active LOW chip enables ($\overline{En}$), an active LOW output enable ($\overline{G}$), and three-state drivers. This device has a power-down feature that reduces power consumption by more than 90% when deselected. Autonomous (master) and demanded (slave) scrubbing continues while deselected.

Writing to the device is accomplished by driving one of the chip enable ($\overline{En}$) inputs LOW and the write enable ($\overline{W}$) input LOW. Data on the 32 I/O pins (DQ0 through DQ31) is then written into the location specified on the address pins (A0 through A18). Reading from the device is accomplished by driving one of the chip enables ($\overline{En}$) and output enable ($\overline{G}$) LOW while driving write enable ($\overline{W}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins. **Note:** Only on En pin may be active at any time.

The 32 input/output pins (DQ0 through DQ31) are placed in a high impedance state when the device is deselected ($\overline{En}$ HIGH), the outputs are disabled ($\overline{G}$ HIGH), or during a write operation ($\overline{En}$ LOW, $\overline{W}$ LOW).

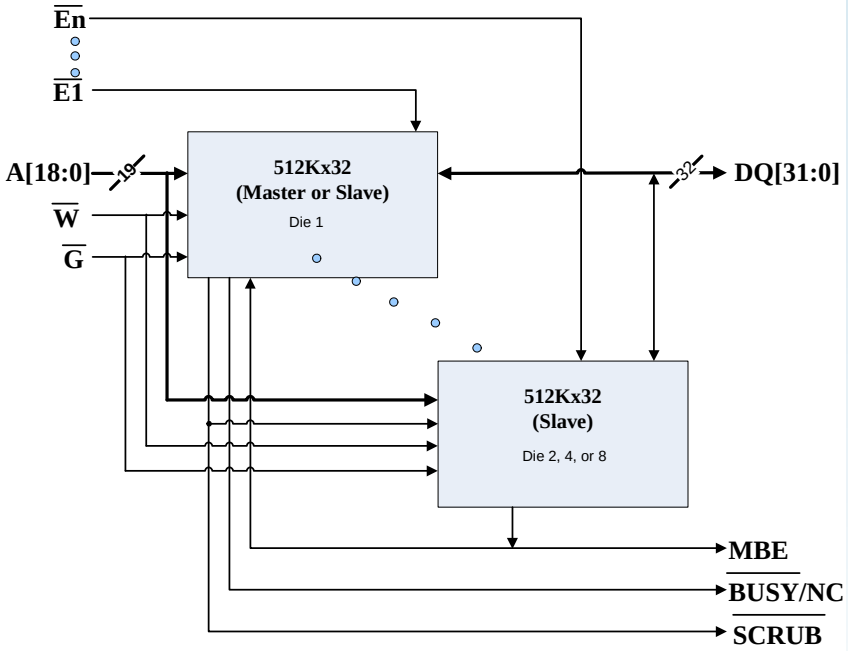
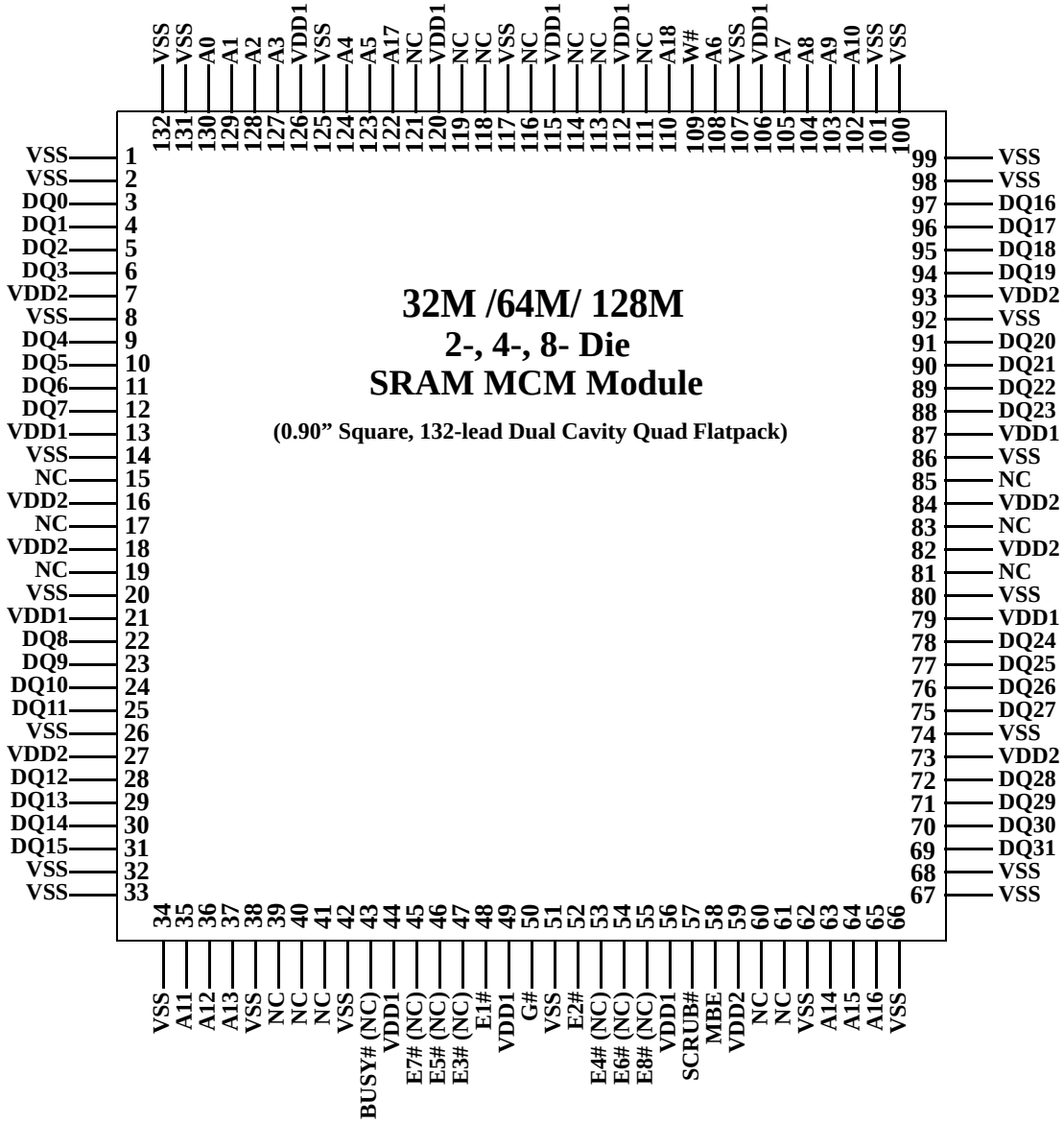


Figure 1. Block Diagram



Notes:
1. NC = Pins are not connected on die.
2. (NC) = Depending on device option, pin may be either signal as named or NC (see Table 1).

Figure 2. Pin Diagram

Table 1. Device Option: Signal and Pin Description

Pkg Pin #	UT8ER1M32M (Master) Signal Name	UT8ER1M32S (Slave) Signal Name	UT8ER2M32M (Master) Signal Name	UT8ER2M32S (Slave) Signal Name	UT8ER4M32M (Master) Signal Name	UT8ER4M32S (Slave) Signal Name	Device Pin Description
1	VSS	VSS	VSS	VSS	VSS	VSS	PWR
2	VSS	VSS	VSS	VSS	VSS	VSS	PWR
3	DQ0	DQ0	DQ0	DQ0	DQ0	DQ0	DATA I/O
4	DQ1	DQ1	DQ1	DQ1	DQ1	DQ1	DATA I/O
5	DQ2	DQ2	DQ2	DQ2	DQ2	DQ2	DATA I/O
6	DQ3	DQ3	DQ3	DQ3	DQ3	DQ3	DATA I/O
7	VDD2	VDD2	VDD2	VDD2	VDD2	VDD2	PWR
8	VSS	VSS	VSS	VSS	VSS	VSS	PWR
9	DQ4	DQ4	DQ4	DQ4	DQ4	DQ4	DATA I/O
10	DQ5	DQ5	DQ5	DQ5	DQ5	DQ5	DATA I/O
11	DQ6	DQ6	DQ6	DQ6	DQ6	DQ6	DATA I/O
12	DQ7	DQ7	DQ7	DQ7	DQ7	DQ7	DATA I/O
13	VDD1	VDD1	VDD1	VDD1	VDD1	VDD1	PWR
14	VSS	VSS	VSS	VSS	VSS	VSS	PWR
15	NC	NC	NC	NC	NC	NC	NC
16	VDD2	VDD2	VDD2	VDD2	VDD2	VDD2	PWR
17	NC	NC	NC	NC	NC	NC	NC
18	VDD2	VDD2	VDD2	VDD2	VDD2	VDD2	PWR
19	NC	NC	NC	NC	NC	NC	NC
20	VSS	VSS	VSS	VSS	VSS	VSS	PWR
21	VDD1	VDD1	VDD1	VDD1	VDD1	VDD1	PWR
22	DQ8	DQ8	DQ8	DQ8	DQ8	DQ8	DATA I/O
23	DQ9	DQ9	DQ9	DQ9	DQ9	DQ9	DATA I/O
24	DQ10	DQ10	DQ10	DQ10	DQ10	DQ10	DATA I/O
25	DQ11	DQ11	DQ11	DQ11	DQ11	DQ11	DATA I/O
26	VSS	VSS	VSS	VSS	VSS	VSS	PWR
27	VDD2	VDD2	VDD2	VDD2	VDD2	VDD2	PWR
28	DQ12	DQ12	DQ12	DQ12	DQ12	DQ12	DATA I/O
29	DQ13	DQ13	DQ13	DQ13	DQ13	DQ13	DATA I/O
30	DQ14	DQ14	DQ14	DQ14	DQ14	DQ14	DATA I/O

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Pkg Pin #	UT8ER1M32M (Master) Signal Name	UT8ER1M32S (Slave) Signal Name	UT8ER2M32M (Master) Signal Name	UT8ER2M32S (Slave) Signal Name	UT8ER4M32M (Master) Signal Name	UT8ER4M32S (Slave) Signal Name	Device Pin Description
31	DQ15	DQ15	DQ15	DQ15	DQ15	DQ15	DATA I/O
32	VSS	VSS	VSS	VSS	VSS	VSS	PWR
33	VSS	VSS	VSS	VSS	VSS	VSS	PWR
34	VSS	VSS	VSS	VSS	VSS	VSS	PWR
35	A11	A11	A11	A11	A11	A11	ADDRESS INPUT
36	A12	A12	A12	A12	A12	A12	ADDRESS INPUT
37	A13	A13	A13	A13	A13	A13	ADDRESS INPUT
38	VSS	VSS	VSS	VSS	VSS	VSS	PWR
39	NC	NC	NC	NC	NC	NC	NC
40	NC	NC	NC	NC	NC	NC	NC
41	NC	NC	NC	NC	NC	NC	NC
42	VSS	VSS	VSS	VSS	VSS	VSS	PWR
43	BUSY#	NC	BUSY#	NC	BUSY#	NC	OUTPUT[1]
44	VDD1	VDD1	VDD1	VDD1	VDD1	VDD1	PWR
45	NC	NC	NC	NC	E7#	E7#	CONTROL INPUT[2]
46	NC	NC	NC	NC	E5#	E5#	CONTROL INPUT[2]
47	NC	NC	E3#	E3#	E3#	E3#	CONTROL INPUT[2]
48	E1#	E1#	E1#	E1#	E1#	E1#	CONTROL INPUT
49	VDD1	VDD1	VDD1	VDD1	VDD1	VDD1	PWR
50	G#	G#	G#	G#	G#	G#	CONTROL INPUT
51	VSS	VSS	VSS	VSS	VSS	VSS	PWR
52	E2#	E2#	E2#	E2#	E2#	E2#	CONTROL INPUT
53	NC	NC	E4#	E4#	E4#	E4#	CONTROL INPUT[2]

Table 1. Device Option: Signal and Pin Description

Pkg Pin #	UT8ER1M32M (Master) Signal Name	UT8ER1M32S (Slave) Signal Name	UT8ER2M32M (Master) Signal Name	UT8ER2M32S (Slave) Signal Name	UT8ER4M32M (Master) Signal Name	UT8ER4M32S (Slave) Signal Name	Device Pin Description
54	NC	NC	NC	NC	E6#	E6#	CONTROL INPUT[2]
55	NC	NC	NC	NC	E8#	E8#	CONTROL INPUT[2]
56	VDD1	VDD1	VDD1	VDD1	VDD1	VDD1	PWR
57	SCRUB#	SCRUB#	SCRUB#	SCRUB#	SCRUB#	SCRUB#	CONTROL I/O[3]
58	MBE	MBE	MBE	MBE	MBE	MBE	DATA I/O
59	VDD2	VDD2	VDD2	VDD2	VDD2	VDD2	PWR
60	NC	NC	NC	NC	NC	NC	NC
61	NC	NC	NC	NC	NC	NC	NC
62	VSS	VSS	VSS	VSS	VSS	VSS	PWR
63	A14	A14	A14	A14	A14	A14	ADDRESS INPUT
64	A15	A15	A15	A15	A15	A15	ADDRESS INPUT
65	A16	A16	A16	A16	A16	A16	ADDRESS INPUT
66	VSS	VSS	VSS	VSS	VSS	VSS	PWR
67	VSS	VSS	VSS	VSS	VSS	VSS	PWR
68	VSS	VSS	VSS	VSS	VSS	VSS	PWR
69	DQ31	DQ31	DQ31	DQ31	DQ31	DQ31	DATA I/O
70	DQ30	DQ30	DQ30	DQ30	DQ30	DQ30	DATA I/O
71	DQ29	DQ29	DQ29	DQ29	DQ29	DQ29	DATA I/O
72	DQ28	DQ28	DQ28	DQ28	DQ28	DQ28	DATA I/O
73	VDD2	VDD2	VDD2	VDD2	VDD2	VDD2	PWR
74	VSS	VSS	VSS	VSS	VSS	VSS	PWR
75	DQ27	DQ27	DQ27	DQ27	DQ27	DQ27	DATA I/O
76	DQ26	DQ26	DQ26	DQ26	DQ26	DQ26	DATA I/O
77	DQ25	DQ25	DQ25	DQ25	DQ25	DQ25	DATA I/O
78	DQ24	DQ24	DQ24	DQ24	DQ24	DQ24	DATA I/O
79	VDD1	VDD1	VDD1	VDD1	VDD1	VDD1	PWR
80	VSS	VSS	VSS	VSS	VSS	VSS	PWR

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Pkg Pin #	UT8ER1M32M (Master) Signal Name	UT8ER1M32S (Slave) Signal Name	UT8ER2M32M (Master) Signal Name	UT8ER2M32S (Slave) Signal Name	UT8ER4M32M (Master) Signal Name	UT8ER4M32S (Slave) Signal Name	Device Pin Description
81	NC	NC	NC	NC	NC	NC	NC
82	VDD2	VDD2	VDD2	VDD2	VDD2	VDD2	PWR
83	NC	NC	NC	NC	NC	NC	NC
84	VDD2	VDD2	VDD2	VDD2	VDD2	VDD2	PWR
85	NC	NC	NC	NC	NC	NC	NC
86	VSS	VSS	VSS	VSS	VSS	VSS	PWR
87	VDD1	VDD1	VDD1	VDD1	VDD1	VDD1	PWR
88	DQ23	DQ23	DQ23	DQ23	DQ23	DQ23	DATA I/O
89	DQ22	DQ22	DQ22	DQ22	DQ22	DQ22	DATA I/O
90	DQ21	DQ21	DQ21	DQ21	DQ21	DQ21	DATA I/O
91	DQ20	DQ20	DQ20	DQ20	DQ20	DQ20	DATA I/O
92	VSS	VSS	VSS	VSS	VSS	VSS	PWR
93	VDD2	VDD2	VDD2	VDD2	VDD2	VDD2	PWR
94	DQ19	DQ19	DQ19	DQ19	DQ19	DQ19	DATA I/O
95	DQ18	DQ18	DQ18	DQ18	DQ18	DQ18	DATA I/O
96	DQ17	DQ17	DQ17	DQ17	DQ17	DQ17	DATA I/O
97	DQ16	DQ16	DQ16	DQ16	DQ16	DQ16	DATA I/O
98	VSS	VSS	VSS	VSS	VSS	VSS	PWR
99	VSS	VSS	VSS	VSS	VSS	VSS	PWR
100	VSS	VSS	VSS	VSS	VSS	VSS	PWR
101	VSS	VSS	VSS	VSS	VSS	VSS	PWR
102	A10	A10	A10	A10	A10	A10	ADDRESS INPUT
103	A9	A9	A9	A9	A9	A9	ADDRESS INPUT
104	A8	A8	A8	A8	A8	A8	ADDRESS INPUT
105	A7	A7	A7	A7	A7	A7	ADDRESS INPUT
106	VDD1	VDD1	VDD1	VDD1	VDD1	VDD1	PWR
107	VSS	VSS	VSS	VSS	VSS	VSS	PWR
108	A6	A6	A6	A6	A6	A6	ADDRESS INPUT

Table 1. Device Option: Signal and Pin Description

Pkg Pin #	UT8ER1M32M (Master) Signal Name	UT8ER1M32S (Slave) Signal Name	UT8ER2M32M (Master) Signal Name	UT8ER2M32S (Slave) Signal Name	UT8ER4M32M (Master) Signal Name	UT8ER4M32S (Slave) Signal Name	Device Pin Description
109	W#	W#	W#	W#	W#	W#	CONTROL INPUT
110	A18	A18	A18	A18	A18	A18	ADDRESS INPUT
111	NC	NC	NC	NC	NC	NC	NC
112	VDD1	VDD1	VDD1	VDD1	VDD1	VDD1	PWR
113	NC	NC	NC	NC	NC	NC	NC
114	NC	NC	NC	NC	NC	NC	NC
115	VDD1	VDD1	VDD1	VDD1	VDD1	VDD1	PWR
116	NC	NC	NC	NC	NC	NC	NC
117	VSS	VSS	VSS	VSS	VSS	VSS	PWR
118	NC	NC	NC	NC	NC	NC	NC
119	NC	NC	NC	NC	NC	NC	NC
120	VDD1	VDD1	VDD1	VDD1	VDD1	VDD1	PWR
121	NC	NC	NC	NC	NC	NC	NC
122	A17	A17	A17	A17	A17	A17	ADDRESS INPUT
123	A5	A5	A5	A5	A5	A5	ADDRESS INPUT
124	A4	A4	A4	A4	A4	A4	ADDRESS INPUT
125	VSS	VSS	VSS	VSS	VSS	VSS	PWR
126	VDD1	VDD1	VDD1	VDD1	VDD1	VDD1	PWR
127	A3	A3	A3	A3	A3	A3	ADDRESS INPUT
128	A2	A2	A2	A2	A2	A2	ADDRESS INPUT
129	A1	A1	A1	A1	A1	A1	ADDRESS INPUT
130	A0	A0	A0	A0	A0	A0	ADDRESS INPUT
131	VSS	VSS	VSS	VSS	VSS	VSS	PWR
132	VSS	VSS	VSS	VSS	VSS	VSS	PWR

MASTER or SLAVE OPTIONS

To reduce the bit error rates, the SRAM devices employ an embedded EDAC (error detection and correction) with user programmable auto scrubbing options. The SRAM devices can automatically correct single bit word errors in event of an upset. During a read operation, if a multiple bit error occurs in a word, the SRAMs assert the MBE output to notify the host.

All SRAM devices are offered in two options: Master (UT8ER1M32M, UT8ER2M32M and UT8ER4M32M) or Slave (UT8ER1M32S, UT8ER2M32S and UT8ER4M32S). The masters are a full function device which features user defined autonomous EDAC scrubbing options. The slave device employs a scrub on demand feature.

The master and slave device pins $\overline{\text{SCRUB}}$ and $\overline{\text{BUSY}}$ are physically different. The $\overline{\text{SCRUB}}$ pin is an output on the master device, but an input on the slave device. The master $\overline{\text{SCRUB}}$ pin asserts low when a scrub cycle initiates, and can be used to demand scrub cycles from multiple slave units when connected to the $\overline{\text{SCRUB}}$ input of slave(s). The $\overline{\text{BUSY}}$ pin is an output for the master device and can be used to generate wait states by the memory controller. The $\overline{\text{BUSY}}$ pin is a no connect (NC) for slave devices.

DEVICE OPERATION

The SRAMs have control inputs called Chip Enable ($\overline{\text{En}}$), Write Enable ($\overline{\text{W}}$), and Output Enable ($\overline{\text{G}}$); 19 address inputs, A(18:0); and 32 bidirectional data lines, DQ(31:0). The $\overline{\text{En}}$ (chip enable) controls selection between active and standby modes. Asserting $\overline{\text{En}}$ enables the device, causes I_{DD} to rise to its active value, and decodes the 19 address inputs. Only one chip enable may be active at any time. $\overline{\text{W}}$ controls read and write operations. During a read cycle, $\overline{\text{G}}$ must be asserted to enable the outputs.

Table 2. SRAM Device Control Operation Truth Table

$\overline{\text{G}}$	$\overline{\text{W}}$	$\overline{\text{En}}$	I/O Mode	Mode
X	X	H	DQ(31:0) 3-State	Standby
L	H	L	DQ(31:0) Data Out	Word Read
H	H	L	DQ(31:0) All 3-State	Word Read[2]
X	L	L	DQ(31:0) All 3-State	Word Write

Notes:
1. "X" is defined as a "don't care" condition.
2. Device active; outputs disabled.

Table 3. EDAC Control Pin Operation Truth Table

MBE	$\overline{\text{SCRUB}}$	$\overline{\text{BUSY}}$	I/O Mode	Mode
H	H	H	Read	Uncorrectable Multiple Bit Error
L	H	H	Read	Valid Data Out
X	H	H	X	Device Ready
X	H	L	X	Device Ready / Scrub Request Pending
X	L	X	Not Accessible	Device Busy

Notes:
1. "X" is defined as a "don't care" condition
2. $\overline{\text{BUSY}}$ signal is a "NC" for slave devices and are an "X" don't care.

READ CYCLE

A combination of $\overline{\text{W}}$ greater than V_{IH} (min) with a single $\overline{\text{En}}$ and $\overline{\text{G}}$ less than V_{IL} (max) defines a read cycle. Read access time is measured from the latter of device enable, output enable, or valid address to valid data output.

SRAM Read Cycle 1, the Address Access in Figure 3a, is initiated by a change in address inputs after a single $\overline{\text{En}}$ is asserted, $\overline{\text{G}}$ is asserted, $\overline{\text{W}}$ is deasserted and all are stable. Valid data appears on data outputs DQ(31:0) after the specified t_{AVQV} is satisfied. Outputs remain active throughout the entire cycle. As long as device enable and output enable are active, the minimum time between valid address changes is specified by the read cycle time (t_{AVAV}).

SRAM Read Cycle 2, the Chip Enable-controlled Access in Figure 3b is initiated by a single $\overline{\text{En}}$ going active while $\overline{\text{G}}$ remains asserted, $\overline{\text{W}}$ remains deasserted, and the addresses remain stable for the entire cycle. After the specified t_{ETQV} is satisfied, the 32-bit word addressed by A(18:0) is accessed and appears at the data outputs DQ(31:0).

SRAM Read Cycle 3, the Output Enable-controlled Access in Figure 3c, is initiated by $\overline{\text{G}}$ going active while a single $\overline{\text{En}}$ is asserted , $\overline{\text{W}}$ is deasserted, and the addresses are stable. Read access time is t_{GLQV} unless t_{AVQV} or t_{ETQV} (reference Figure 3b) have not been satisfied.

SRAM EDAC Status Indications during a Read Cycle, if MBE is Low, the data is valid. If MBE is High, the data is corrupted (reference Table 3).

WRITE CYCLE

A combination of $\overline{W}$ and a single $\overline{En}$ less than V_{IL}(max) defines a write cycle. The state of $\overline{G}$ is a "don't care" for a write cycle. The outputs are placed in the high-impedance state when either $\overline{G}$ is greater than V_{IH}(min) or when $\overline{W}$ is less than V_{IL}(max).

Write Cycle 1, the Write Enable-controlled Access in Figure 4a, is defined by a write terminated by $\overline{W}$ going high with a single $\overline{En}$ still active. The write pulse width is defined by t_{WLWH} when the write is initiated by $\overline{W}$ and by t_{ETWH} when the write is initiated by $\overline{En}$. To avoid bus contention t_{WLQZ} must be satisfied before data is applied to the 32 bidirectional pins DQ(31:0) unless the outputs have been previously placed in high impedance state by deasserting $\overline{G}$.

Write Cycle 2, the Chip Enable-controlled Access in Figure 4b, is defined by a write terminated by a single $\overline{En}$. The write pulse width is defined by t_{WLEF} when the write is initiated by $\overline{W}$ and by t_{ETEF} when the write is initiated by $\overline{En}$ going active. For the $\overline{W}$ initiated write, unless the outputs have been previously placed in the high-impedance state by $\overline{G}$, the user must wait t_{WLQZ} before applying data to the 32 bidirectional pins DQ(31:0) to avoid bus contention.

CONTROL REGISTER WRITE/READ CYCLES

Configuration options can be selected by writing to the control register. The configuration tables (Tables 5 and 6) details the programming options. Scrub rate period and $\overline{BUSY}$ to $\overline{SCRUB}$ configurations are applicable to master devices using $\overline{E1}$ chip enable only. EDAC bypass and Read/Write control register is applicable to all valid chip enables $\overline{En}$. The control register is accessed by applying a series of values to the address bus as shown in Figures 7a and 7b. After the series the contents of the control register can be either read or written depending on the value of the corresponding read/write control register address pin (A(9) for add die and A(2) for even die). **NOTE:** MBE must be driven high by the user for both a write or a read of the control register.

MEMORY SCRUBBING/CYCLE STEALING

The SRAMs use architectural improvements and embedded error detection and correction to maintain unsurpassed levels of error protection. This is accomplished by what Aeroflex refers to as Cycle Stealing. To minimize the system design impact on the speed of operation, the edge relationship between $\overline{BUSY}$ and $\overline{SCRUB}$ is programmable via the sequence described in figures 7a and 7b. The $\overline{BUSY}$ output is intended to give notification to the memory controller that a scrub cycle is impending. Since the memory cannot be accessed during an internal scrub cycle, the $\overline{BUSY}$ to SCRUB delay can be adjusted so the user may complete accesses prior to internal scrubbing.

The effective error rate is a function of the intrinsic error rate and the environment. Therefore, users are given the ability to control the scrub rate (ref. figure 7a) appropriate for the applicable environment. **NOTE:** the scrub rate will have an inverse relationship to the total throughput of the memory.

A master mode scrub cycle will occur at the user defined Scrub Rate Period. A scrub cycle is defined as the verification and correction (if necessary) of data for a single word address location. Address locations are scrubbed sequentially every Scrub Rate Period (t_{SCRT}). Scrub cycles will occur at every Scrub Rate Period regardless of the status of control pins. All inputs should remain stable while the $\overline{SCRUB}$ signal is active to avoid data corruption. Control pin function will be returned upon deassertion of $\overline{BUSY}$ pin. The Slave mode scrub cycle occurs anytime the $\overline{SCRUB}$ pin is asserted. The scrub cycle is defined the same as the master mode and will occur regardless of control pin status. Control pin function will be returned upon $\overline{SCRUB}$ deassertion.

Data is corrected during not only the internal scrub, but again during a user requested read cycle. If the data presented contains two or more errors after t_{AVAV} is satisfied, the MBE signal will be asserted. (**Note:** Reading un-initialized memory locations may result in un-intended MBE assertions.)

Table 4. Operational Environment[1]

Total Dose	100K	rad(Si)
Heavy Ion Error Rate[2]	$6.0x10^{-16}$	Errors/Bit-Day

Notes:

1. The SRAM is immune to latchup to particles >111MeV-cm^2/mg.
2. 90% worst case particle environment, Geosynchronous orbit, 100 mils of Aluminum and default EDAC scrub rate.

SUPPLY SEQUENCING

No supply voltage sequencing is required between V_{DD1} and V_{DD2}.

POWER-UP REQUIREMENTS

During power-up of the SRAM devices, the power supply voltages will transverse through voltage ranges where the device is not guaranteed to operate before reaching final levels. Since some circuits on the device may operate at lower voltage levels than others, the device may power-up in an unknown state. To eliminate this with most power-up situations, the device employs an on-chip power-on-reset (POR) circuit. The POR, however, requires time to complete the operation. Therefore, it is recommended that all device activity be delayed by a minimum of 100ms, after both V_{DD1} and V_{DD2} supplies have reached stable minimum operating voltage.

ABSOLUTE MAXIMUM RATINGS[1]
(Referenced to V_{SS})

SYMBOL	PARAMETER	LIMITS
V_{DD1}	DC supply voltage (Core)	-0.3 to 2.1V
V_{DD2}	DC supply voltage (I/O)	-0.3 to 3.8V
$V_{I/O}$	Voltage on any pin	-0.3 to 3.8V
T_{STG}	Storage temperature	-65 to +150°C
P_D[2]: UT8ER1M32 UT8ER2M32 UT8ER4M32	Maximum package power dissipation permitted @ Tc = +105°C	 4W 2W 1.3W
T_J	Maximum junction temperature	+150°C
Θ_{JC}[3]: UT8ER1M32 UT8ER2M32 UT8ER4M32	Thermal resistance, junction-to-case[2]	 6°C/W 10°C/W 15°C/W
I_I	DC input current	±10 mA

Notes:
1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.
2. Per MIL-STD-883, Method 1012, Section 3.4.1, $P_D = \frac{(T_J(max) - Tc\ (max))}{\Theta_{JC}}$
3. Θ_{JC} varies with density due to stacked die configuration.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS
V_{DD1}	DC supply voltage (Core)	1.7 to 2.0V
V_{DD2}	DC supply voltage (I/O)	2.3 to 3.6V
T_C	Case temperature range	-55 to +105°C
V_{IN}	DC input voltage	0V to V_{DD2}

DC ELECTRICAL CHARACTERISTICS (Pre and Post-Radiation)*

(V_{DD1} = 1.7V to 2.0V, V_{DD2} = 2.3V to 3.6V; Unless otherwise noted, Tc is per the temperature range ordered)

SYMBOL	PARAMETER	CONDITION		MIN	MAX	UNIT
V_{IH}	High-level input voltage			2.2		V
V_{IL}	Low-level input voltage				0.8	V
V_{OL1}	Low-level output voltage	I_{OL} = 8mA, 3.0V≤V_{DD2} ≤ 3.6V			0.4	V
V_{OL2}	Low-level output voltage	I_{OL} = 6mA, 2.3V≤V_{DD2} ≤ 2.7V			0.2*V_{DD2}	
V_{OH1}	High-level output voltage	I_{OH} = -4mA,3.0V≤ V_{DD2} ≤ 3.6V		0.8*V_{DD2}		V
V_{OH2}	High-level output voltage	I_{OL} = -2mA, 2.3V≤V_{DD2} ≤ 2.7V		0.8*V_{DD2}		V
I_{IN}	Input leakage current	V_{IN} = V_{DD2} and V_{SS}		-2	2	µA
I_{OZ}[3]	Three-state output leakage current	V_O = V_{DD2} and V_{SS} V_{DD2} = V_{DD2} (max), $\overline{G}$ = V_{DD2} (max)		-2	2	µA
I_{OS}[4, 5]	Short-circuit output current	V_{DD2} = V_{DD2} (max), V_O = V_{DD2} V_{DD2} = V_{DD2} (max), V_O = V_{SS}		-100	+100	mA
$I_{DD1}(OP_1$[6,8])	V_{DD1} Supply current operating @ 1MHz, EDAC enabled @ default Scrub Rate Period (see table 5).	Inputs: V_{IL} = V_{SS} + 0.2V, V_{IH} = V_{DD2} -0.2V, I_{OUT} = 0 V_{DD1} = V_{DD1} (max), V_{DD2} = V_{DD2} (max)	V_{DD1} = 2.0V		14	mA
			V_{DD1} = 1.9V		10	mA
$I_{DD1}(OP_2$[6,8])	V_{DD1} Supply current operating @ 50MHz, EDAC enabled @ default Scrub Rate Period (see table 5).	Inputs: V_{IL} = V_{SS} + 0.2V, V_{IH} = V_{DD2} -0.2V, I_{OUT} = 0 V_{DD1} = V_{DD1} (max), V_{DD2} = V_{DD2} (max)	V_{DD1} = 2.0V		225	mA
			V_{DD1} = 1.9V		210	mA
$I_{DD2}(OP_1$[6,8])	V_{DD2} Supply current operating @ 1MHz, EDAC enabled @ default Scrub Rate Period (see table 5).	Inputs : V_{IL} = V_{SS} + 0.2V, V_{IH} = V_{DD2} -0.2V, I_{OUT} = 0 V_{DD1} = V_{DD1} (max), V_{DD2} = V_{DD2} (max)			2	mA
$I_{DD2}(OP_2$[6,8])	V_{DD2} Supply current operating @ 50MHz, EDAC enabled @ default Scrub Rate Period (see table 5).	Inputs : V_{IL} = V_{SS} + 0.2V, V_{IH} = V_{DD2} -0.2V, I_{OUT} = 0 V_{DD1} = V_{DD1} (max), V_{DD2} = V_{DD2} (max)			5	mA

SYMBOL	PARAMETER	CONDITION		MIN	MAX	UNIT
$I_{DD1}(SB)^{7,9}$	Supply current standby @ 0Hz, EDAC disabled (per die)	CMOS inputs, I_{OUT} = 0 $\overline{En}$ = V_{DD2} -0.2 V_{DD1} = V_{DD1} (max), V_{DD2} = V_{DD2} (max)	-55°C and 25°C		15	mA
			105°C		35	mA
$I_{DD2}(SB)^{9}$	Supply current standby @ 0Hz, EDAC disabled (per die)	CMOS inputs, I_{OUT} = 0 $\overline{En}$ = V_{DD2} -0.2 V_{DD1} = V_{DD1} (max), V_{DD2} = V_{DD2} (max)			3	mA
$I_{DD1}(SB)^{2,7,9}$	Supply current standby A(16:0) @ 50MHz, EDAC disabled (per die)	CMOS inputs , I_{OUT} = 0 $\overline{En}$ = V_{DD2} - 0.2 V_{DD1} = V_{DD1} (max), V_{DD2} = V_{DD2} (max)	-55°C and 25°C		15	mA
			105°C		35	mA
$I_{DD2}(SB)^{2,9}$	Supply current standby A(16:0) @ 50MHz, EDAC disabled (per die)	CMOS inputs, I_{OUT} = 0 $\overline{En}$ = V_{DD2} - 0.2 V_{DD1} = V_{DD1} (max), V_{DD2} = V_{DD2} (max)			3	mA

CAPACITANCE

SYMBOL	PARAMETER	CONDITION	UT8ER1M32		UT8ER2M32		UT8ER4M32		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
C_{IN}^{2}	Input capacitance	*f* = 1MHz @ 0V		18		TBD		TBD	pF
C_{IO}^{2}	Bidirectional I/O capacitance	*f* = 1MHz @ 0V		15		TBD		TBD	pF

Notes:

* For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.
1. The $\overline{SCRUB}$ and $\overline{BUSY}$ pins for UT8ER1M32M, UT8ER2M32M and UT8ER4M32M (master) are tested functionally for VOL specification.
2. Measured only for initial qualification and after process or design changes that could affect this parameter.
3. The $\overline{SCRUB}$ and $\overline{BUSY}$ pins for UT8ER1M32M, UT8ER2M32M and UT8ER4M32M (master) are guaranteed by design, but neither tested nor characterized.
4. Supplied as a design limit but not guaranteed or tested.
5. Not more than one output may be shorted at a time for maximum duration of one second.
6. EDAC enabled. Default Scrub Rate Period applicable to master device only.
7. Post radiation limits are the 105°C temperature limit when specified.
8. Operating current limit does not include standby current.
9. V_{IH} = V_{DD2} (max), V_{IL} = 0V.

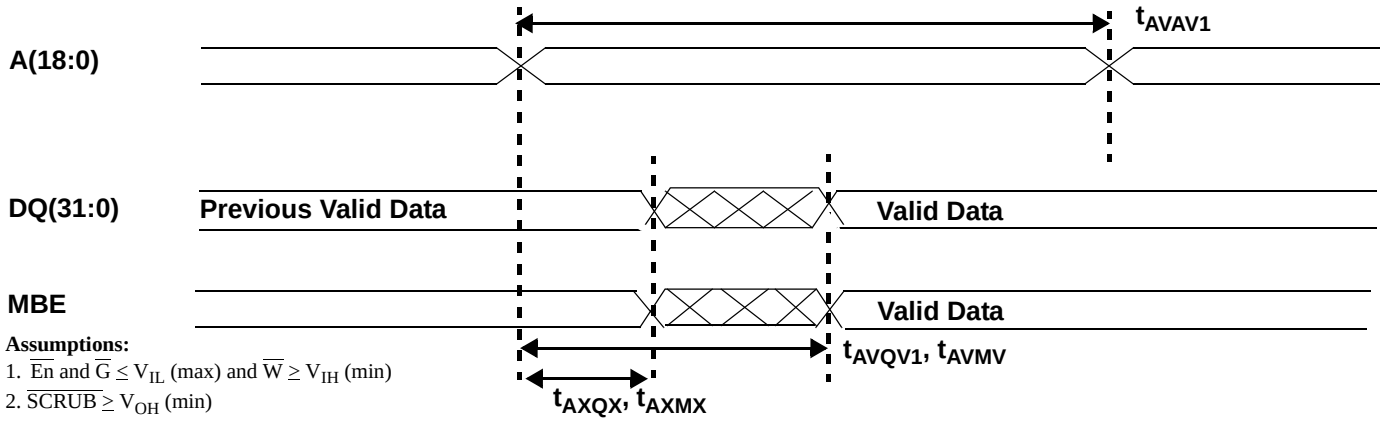
AC CHARACTERISTICS READ CYCLE (Pre and Post-Radiation)*

(V_{DD1} = 1.7V to 2.0V, V_{DD2} = 2.3V to 3.6V); Unless otherwise noted, Tc is per the temperature range ordered

SYMBOL	PARAMETER	UT8ER1M32		UT8ER2M32		UT8ER4M32		UNIT	FIGURE
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{AVAV1}[1]	Read cycle time	20		20		20		ns	3a
t_{AVQV1}	Address to data valid from address change		20		20		20	ns	3c
t_{AXQX}[2]	Output hold time	1.5		1.5		1.5		ns	3a
t_{GLQX}[1,2]	$\overline{G}$-controlled output enable time	1		1		1		ns	3c
t_{GLQV}	$\overline{G}$-controlled output data valid		10		10		10	ns	3c
t_{GHQZ1}[2]	$\overline{G}$-controlled output three-state time	1	8	1	8	1	8	ns	3c
t_{ETQX}[2]	E-controlled output enable time	4		4		4		ns	3b
t_{ETQV}	E-controlled access time		20		20		20	ns	3b
t_{EFQZ}[2]	E-controlled output three-state time[2]	2	9	2	9	2	9	ns	3b
t_{AVMV}	Address to error flag valid		22		22		22	ns	3a
t_{AXMX}[2]	Address to error flag hold time from address change	1.5		1.5		1.5		ns	3a
t_{GLMX}[2]	$\overline{G}$-controlled error flag enable time	0		0		0		ns	3c
t_{GLMV}	$\overline{G}$-controlled error flag valid		8		8		8	ns	3c
t_{ETMX}[2]	E-controlled error flag enable time	4		4		4		ns	3b
t_{ETMV}	E-controlled error flag time		22		22		22	ns	3b
t_{GHMZ}[2]	G-controlled error flag three-state time	1	9	1	9	1	9	ns	3b

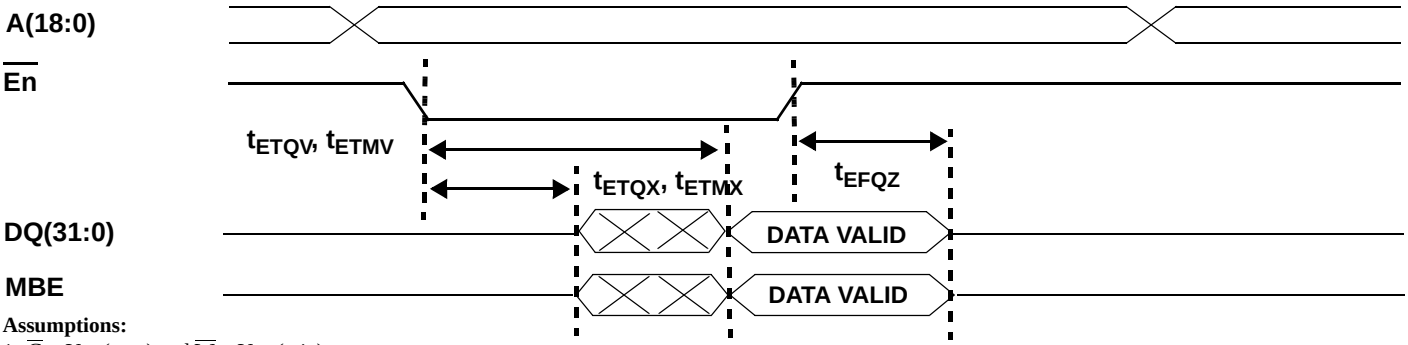
Notes:

* For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.
1. Guaranteed by characterization, but not tested.
2. Three-state is defined as a 300mV change from steady-state output voltage.



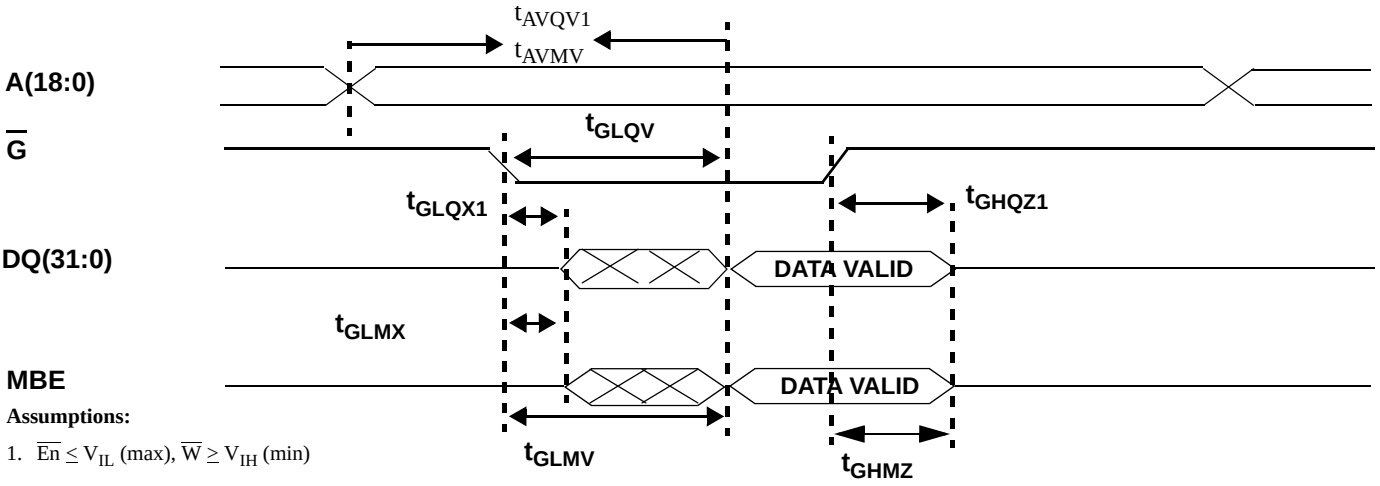
Assumptions:
1. $\overline{En}$ and $\overline{G} \leq V_{IL}$ (max) and $\overline{W} \geq V_{IH}$ (min)
2. $\overline{SCRUB} \geq V_{OH}$ (min)
3. Reading uninitialized addresses may cause MBE to be asserted.

Figure 3a. SRAM Read Cycle 1: Address Access



Assumptions:
1. $\overline{G} \leq V_{IL}$ (max) and $\overline{W} \geq V_{IH}$ (min)
2. $\overline{SCRUB} \geq V_{OH}$ (min)
3. Reading uninitialized addresses may cause MBE to be asserted.

Figure 3b. SRAM Read Cycle 2: Chip Enable Access



Assumptions:
1. $\overline{En} \leq V_{IL}$ (max), $\overline{W} \geq V_{IH}$ (min)
2. $\overline{SCRUB} \geq V_{OH}$ (min)
3. Reading uninitialized addresses may cause MBE to be asserted.

Figure 3c. SRAM Read Cycle 3: Output Enable Access

AC CHARACTERISTICS WRITE CYCLE (Pre and Post-Radiation)*

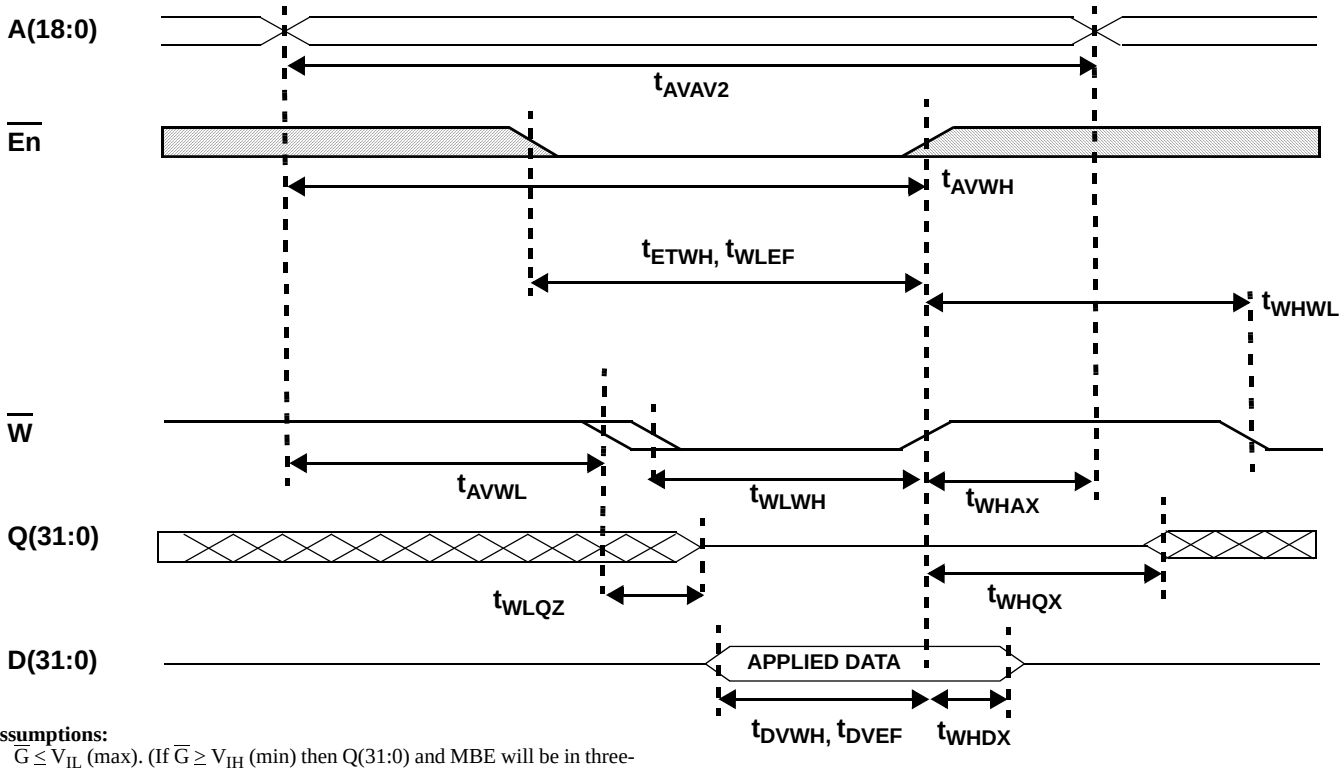
(V_{DD1} = 1.7V to 2.0V, V_{DD2} = 2.3V to 3.6V); Unless otherwise noted, Tc is per the temperature range ordered

SYMBOL	PARAMETER	UT8ER1M32		UT8ER2M32		UT8ER4M32		UNIT	FIGURE
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{AVAV2}[1]	Write cycle time	10		10		10		ns	4a/4b
t_{ETWH}	Device enable to end of write	10		10		10		ns	4a
t_{AVET}	Address setup time for write ($\overline{En}$- controlled)	0		0		0		ns	4b
t_{AVWL}	Address setup time for write ($\overline{W}$ - controlled)	0		0		0		ns	4a
t_{WLWH}[1]	Write pulse width	8		8		8		ns	4a
t_{WHAX}	Address hold time for write ($\overline{W}$ - controlled)	0		0		0		ns	4a
t_{EFAX}	Address hold time for device enable ($\overline{En}$- controlled)	0		0		0		ns	4b
t_{WLQZ}[2]	$\overline{W}$ - controlled three-state time		9		9		9	ns	4a/4b
t_{WHQX}[2]	$\overline{W}$ - controlled output enable time	0		0		0		ns	4a
t_{ETEF}	Device enable pulse width ($\overline{En}$ - controlled)	10		10		10		ns	4b
t_{DVWH}	Data setup time	5		5		5		ns	4a
t_{WHDX}	Data hold time	0		0		0		ns	4a
t_{WLEF}[1]	Device enable controlled write pulse width	8		8		8		ns	4b
t_{DVEF}	Data setup time	5		5		5		ns	4a/4b
t_{EFDX}	Data hold time	0		0		0		ns	4b
t_{AVWH}	Address valid to end of write	10		10		10		ns	4a
t_{WHWL}[1]	Write disable time	1		1		1		ns	4a

Notes:

* For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

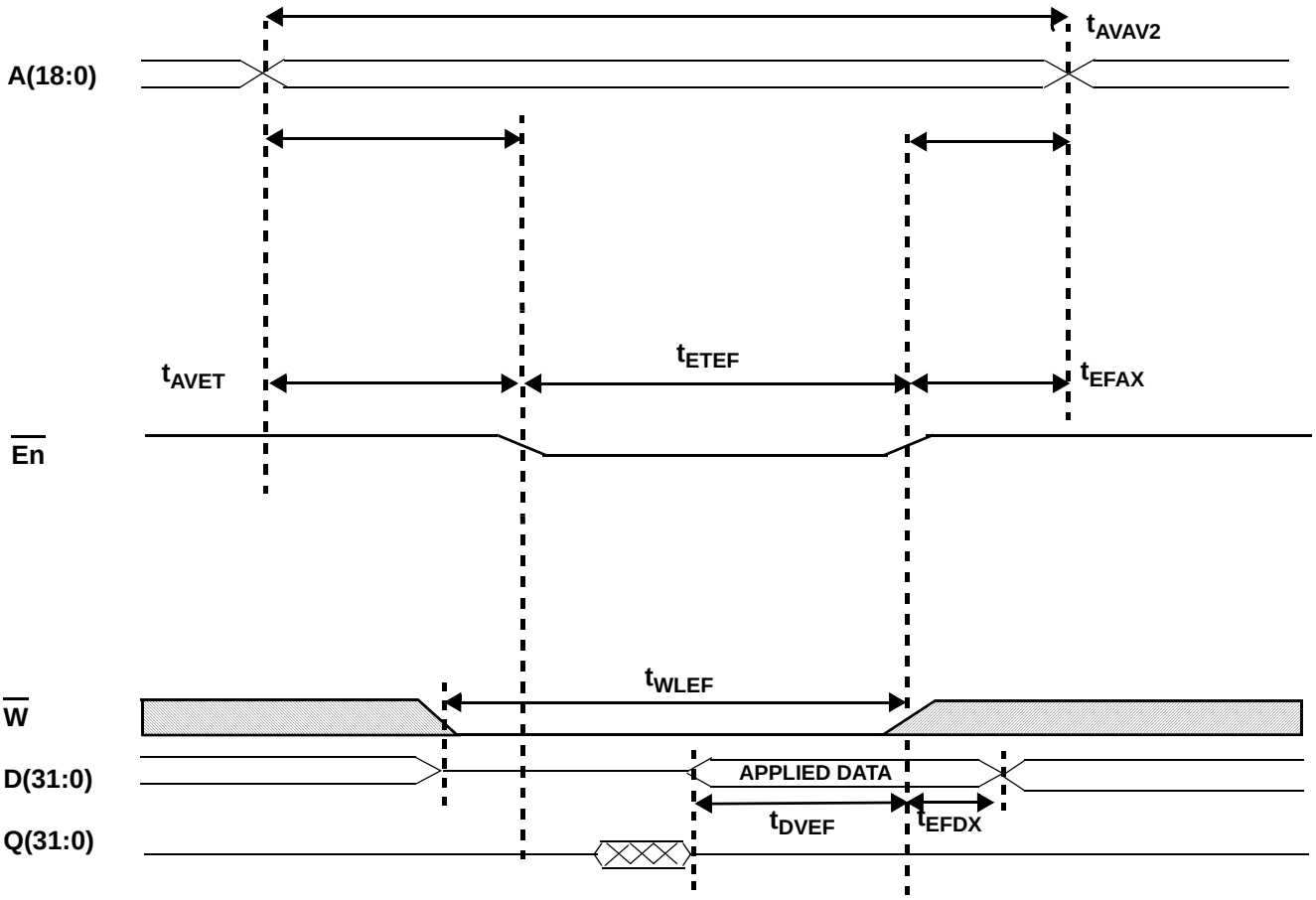
1. Tested with $\overline{G}$ high.
2. Three-state is defined as 300mV change from steady-state output voltage.



Assumptions:
1. $\overline{G} \leq V_{IL}$ (max). (If $\overline{G} \geq V_{IH}$ (min) then Q(31:0) and MBE will be in three-state for the entire cycle.)

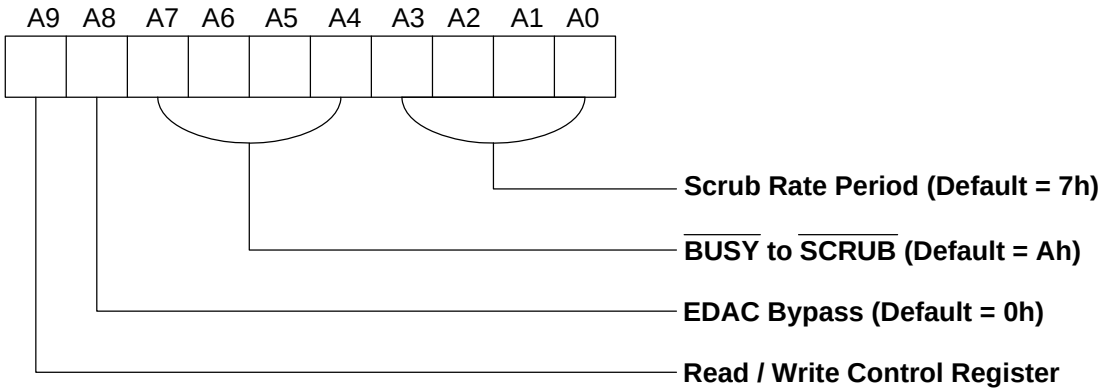
2. $\overline{SCRUB} \geq V_{OH}$ (min)

Figure 4a. SRAM Write Cycle 1: $\overline{W}$ - Controlled Access



Assumptions & Notes:
1. $\overline{G} \leq V_{IL}$ (max). (If $\overline{G} \geq V_{IH}$ (min) then Q(31:0) and MBE will be in three-state for the entire cycle.)
2. $\overline{Busy} \geq V_{OH}$ (min)

Figure 4b. SRAM Write Cycle 2: Enable - Controlled Access



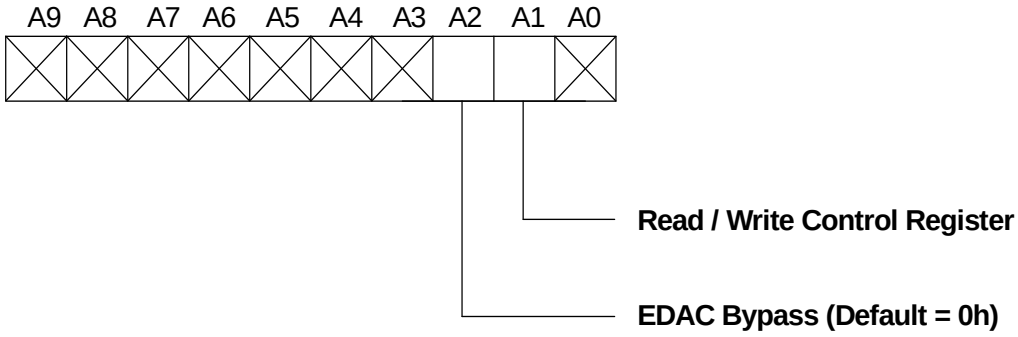
Note:
1. See Table 5 for Control Register Definitions

Figure 5. (Odd Die Numbers ($\overline{E1}$, $\overline{E3}$, $\overline{E5}$, $\overline{E7}$ Chip Enables) EDAC Control Register

Table 5: (Odd Die Numbers ($\overline{E1}$, $\overline{E3}$, $\overline{E5}$, $\overline{E7}$ Chip Enables) EDAC Programming Configuration Table

ADDR BIT	PARAMETER	VALUE	FUNCTION
A (3-0)	Scrub Rate Period[1,2,3]	3-15 Note: 0-2 reserved	As Scrub Rate Period changes from 0 - 15, then the interval between Scrub cycles will change as follows: 3 = 600 ns 8 = 13.0 us 12 = 205 us 4 = 1000 ns 9 = 25.8 us 13 = 409.8 us[4] 5 = 1800 ns 10 = 51.4 us 14 = 819.4 us[4] 6 = 3400 ns 11 = 102.6 us 15 = 1.64 ms[4] 7 = 6600 ns
A (7-4)	$\overline{BUSY}$ to $\overline{SCRUB}$[1,3,5]	0-15	If $\overline{BUSY}$ to $\overline{SCRUB}$ changes from 0 - 15, then the interval t_{BLSL} between $\overline{SCRUB}$ and BUSY will change as follows: 0 = 0 ns 6 = 300 ns 11 = 550 ns 1 = 50 ns 7 = 350 ns 12 = 600 ns 2 = 100 ns 8 = 400 ns 13 = 650 ns 3 = 150 ns 9 = 450 ns 14 = 700 ns 4 = 200 ns 10 = 500 ns 15 = 750 ns 5 = 250ns
A (8)	Bypass EDAC Bit[6,7]	0, 1	If 0, then normal EDAC operation will occur. If 1, then EDAC will be bypassed and no memory scrubbing will occur.
A (9)	Read / $\overline{Write}$ Control Register	0, 1	0 = A8 to A0 will be written to the control register. 1 = Control register will be asserted to the data bus DQ[8:0] respectively.

Notes:
1. Values based on minimum specifications. For guaranteed ranges of Scrub Rate Period (t_{SCRT}) and $\overline{BUSY}$ to $\overline{SCRUB}$ (t_{BLSL}), reference the Master Mode AC Characteristic.
2. Default Scrub Rate Period is 6600 ns.
3. Scrub Rate Period and $\overline{BUSY}$ to $\overline{SCRUB}$ applicable to the master devices die #1 ($\overline{E1}$ chip enable) only.
4. Period below test capability.
5. The default for t_{BLSL} is 500 ns.
6. The default state for A8 is 0.
7. The EDAC bypass option is provided for memory accesses when error correction is not desired (i.e. device and system testing).



Note:
X = Not applicable for even die.
1. See Table 6 for Control Register Definitions

Figure 6. Even Die Numbers ($\overline{E2}$, $\overline{E4}$, $\overline{E6}$, $\overline{E8}$ Chip Enables) EDAC Control Register

Table 6: Even Die Numbers ($\overline{E2}$, $\overline{E4}$, $\overline{E6}$, $\overline{E8}$ Chip Enables) EDAC Programming Configuration Table

ADDR BIT	PARAMETER	VALUE	FUNCTION
A (2)	Bypass EDAC Bit[1,2]	0, 1	If 0, then normal EDAC operation will occur. If 1, then EDAC will be bypassed and no memory scrubbing will occur.
A (1)	Read / $\overline{\text{Write}}$ Control Register	0, 1	0 = A2 will be written to the control register 1 = Control register will be asserted to the data bus DQ18

Notes:
1. The default state for A2 is 0.
2. The EDAC bypass option is provided for memory accesses when error correction is not desired (i.e. device and system testing).

EDAC CONTROL REGISTER AC CHARACTERISTICS (Pre and Post-Radiation)*

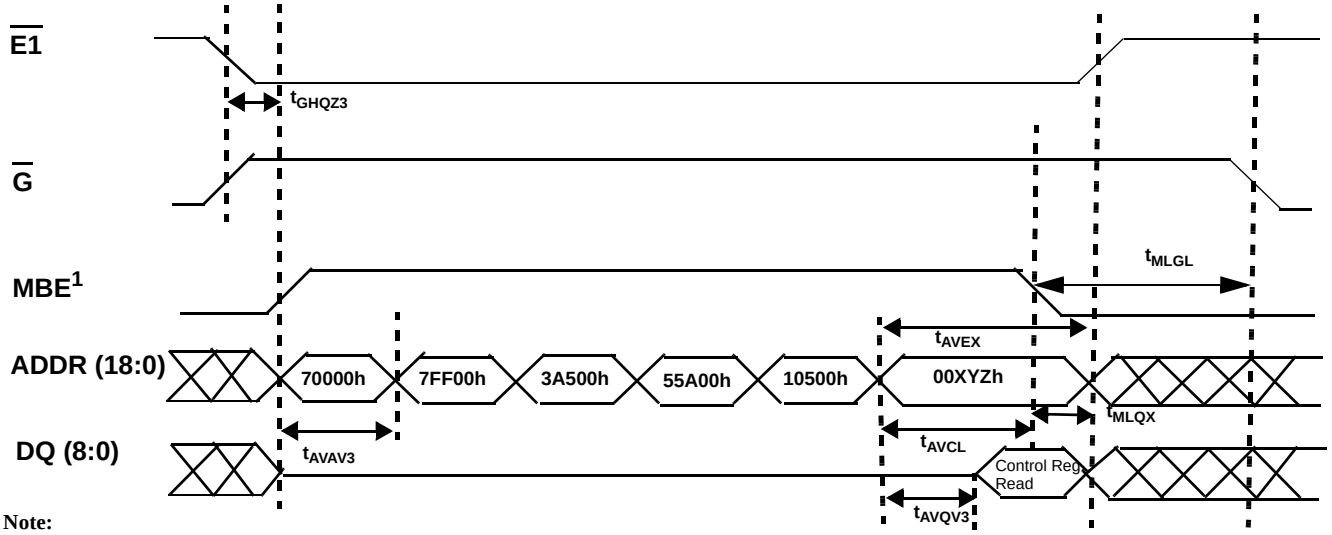
(V_{DD1} = 1.7V to 2.0V, V_{DD2} = 2.3V to 3.6V); Unless otherwise noted, Tc is per the temperature range ordered

SYMBOL	PARAMETER	UT8ER1M32 UT8ER2M32 UT8ER4M32		UNIT	FIGURE
		MIN	MAX		
t_{AVAV3}	Address valid to address valid for control register cycle	200		ns	7a
t_{AVCL}	Address valid to control low	200		ns	7a
t_{AVEX}	Address valid to enable valid	200		ns	7a
t_{AVQV3}	Address to data valid control register read		400	ns	7a
t_{MLQX}[1]	MBE control EDAC disable time	3		ns	7a
t_{GHQZ3}[1]	Output tri-state time	2	9	ns	7a
t_{MLGL}[2]	MBE low to output enable	85		ns	7a

Notes:

* For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

1. Three-state is defined as 300mV change from steady-state output.
2. Guaranteed by design neither tested or characterized.



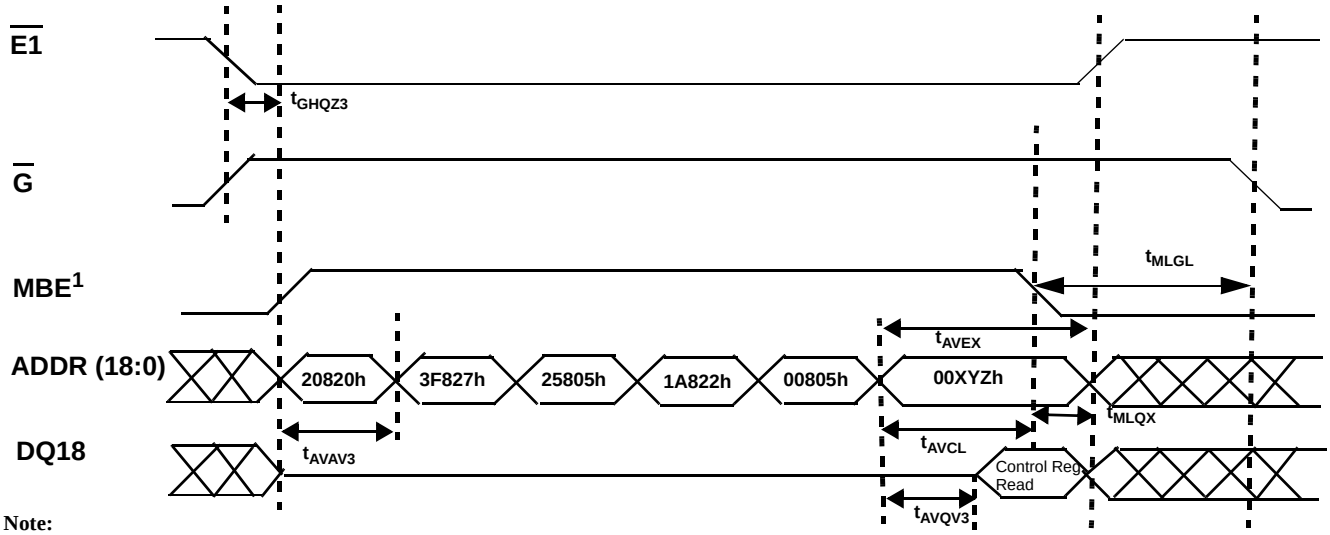
Note:

1. MBE is driven high by the user.
2. Lower 9 bits of the last address are used to read or configure the control register (ref Control Register Write/Read Cycles page 9 and Table 5).

Assumptions:

1. $\overline{SCRUB} \geq V_{OH}$ before the start of the configuration cycle. Ignore $\overline{SCRUB}$ during configuration cycle.

Figure 7a. Odd Die Numbers ($\overline{E1}$, $\overline{E3}$, $\overline{E5}$, $\overline{E7}$ Chip Enables) EDAC Control Register Cycle



Note:
1. MBE is driven high by the user.
2. A2 and A1 of the last address are used to read or configure the control register (ref Control Register Write/Read Cycles page 9 and Table 6).

Assumptions:
1. $\overline{SCRUB} \geq V_{OH}$ before the start of the configuration cycle. Ignore $\overline{SCRUB}$ during configuration cycle.

Figure 7b. Even Die Numbers ($\overline{E2}$, $\overline{E4}$, $\overline{E6}$, $\overline{E8}$ Chip Enables) EDAC Control Register Cycle

MASTER MODE AC CHARACTERISTICS (Pre and Post-Radiation)*

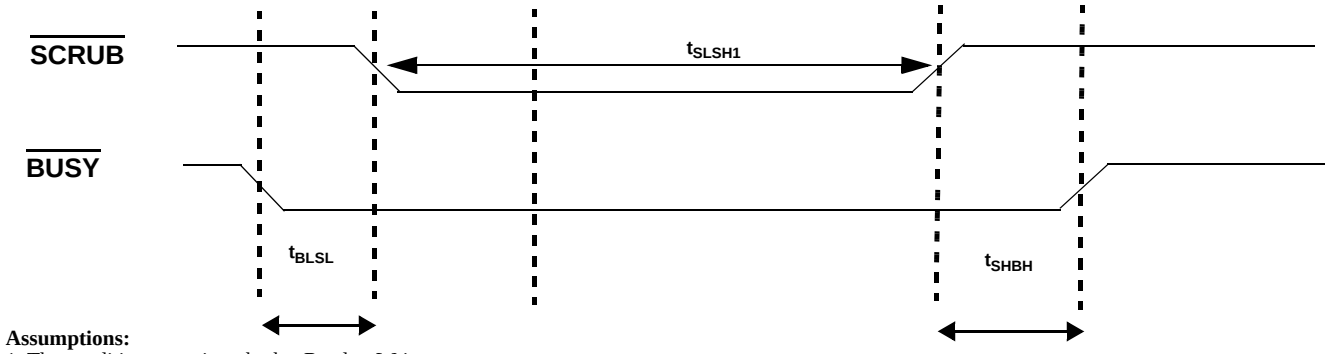
V_{DD1} = 1.7V to 2.0V, V_{DD2} = 2.3V to 3.6V); Unless otherwise noted, Tc is per the temperature range ordered

SYMBOL	PARAMETER	MIN	MAX	UNIT	FIGURE
t_{BLSL}[1]	User Programmable - $\overline{BUSY}$ low to $\overline{SCRUB}$	50*n	(90*n)+1	ns	7b
t_{SLSH1}	$\overline{SCRUB}$ low to $\overline{SCRUB}$ high	200	350	ns	7b
t_{SHBH}	$\overline{SCRUB}$ high to $\overline{BUSY}$ high	50	85	ns	7b
t_{SCRT}[2]	Scrub Rate Period	2^n*50+200	2^n*90+350	ns	7b

Notes:

* For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

1. See Table 5 for User Programmable information. The value "n" is decimal equivalent of hexidecimal value 0x0 through 0xF programmed into control register address bits A_4-A_7 by user. Default value "n" = 10.
2. See Table 5 for User Programmable information. The value "n" is decimal equivalent of hexidecimal value 0x3 through 0xF programmed into control register address bits A_0-A_3. Default value is "n" = 7.



Assumptions:
1. The conditions pertain to both a Read or Write.

Figure 7c. Master Mode Scrub Cycle

SLAVE MODE AC CHARACTERISTICS (Pre and Post-Radiation)*

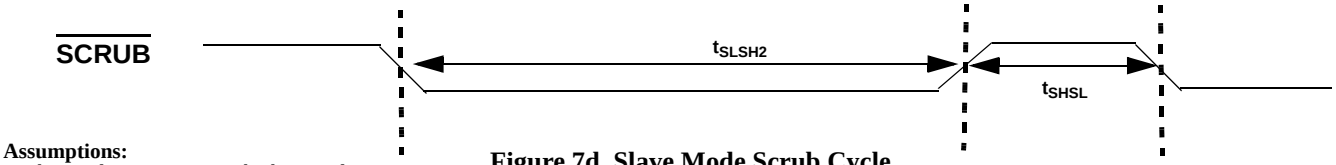
V_{DD1} = 1.7V to 1.9V, V_{DD2} = 2.3V to 3.6V)Unless otherwise noted, Tc is per the temperature range ordered

SYMBOL	PARAMETER	MIN	MAX	UNIT	FIGURE
t_{SLSH2}	$\overline{SCRUB}$ low to $\overline{SCRUB}$ high (slave)	200		ns	7c
t_{SHSL}[1]	$\overline{SCRUB}$ high to $\overline{SCRUB}$ low (slave)	400		ns	7c

Notes:

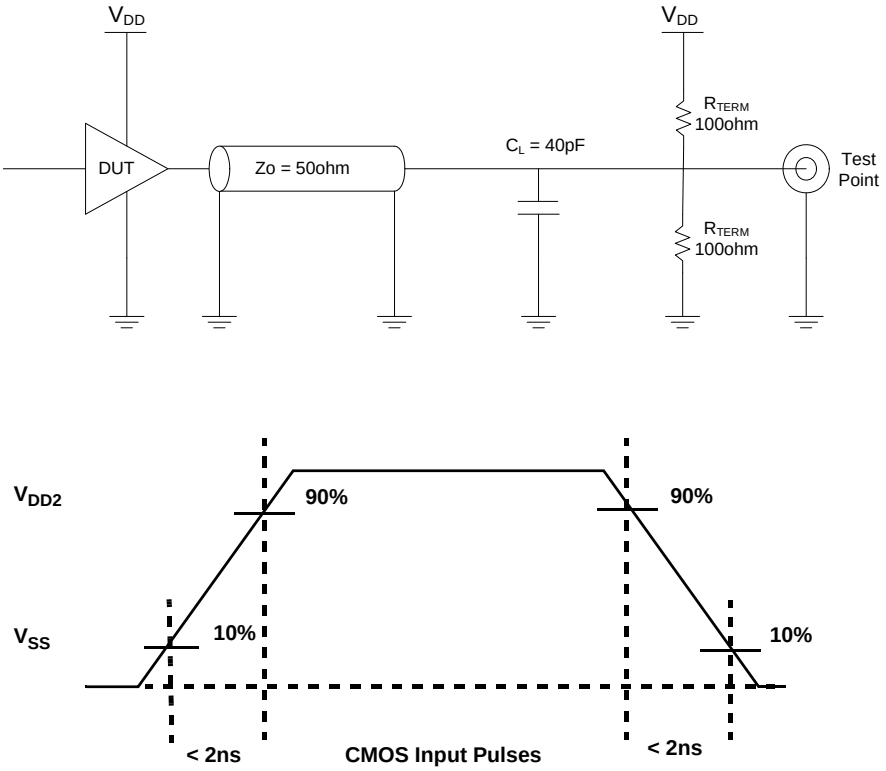
* For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

1. Guaranteed by design, neither tested nor characterized.



Assumptions:
1. The conditions pertain to both a Read or Write.

Figure 7d. Slave Mode Scrub Cycle



Notes:
1. Measurement of data output occurs at the low to high or high to low transition mid-point (i.e., CMOS input = $V_{DD2}/2$)

Figure 8. AC Test Loads and Input Waveforms

PACKAGING

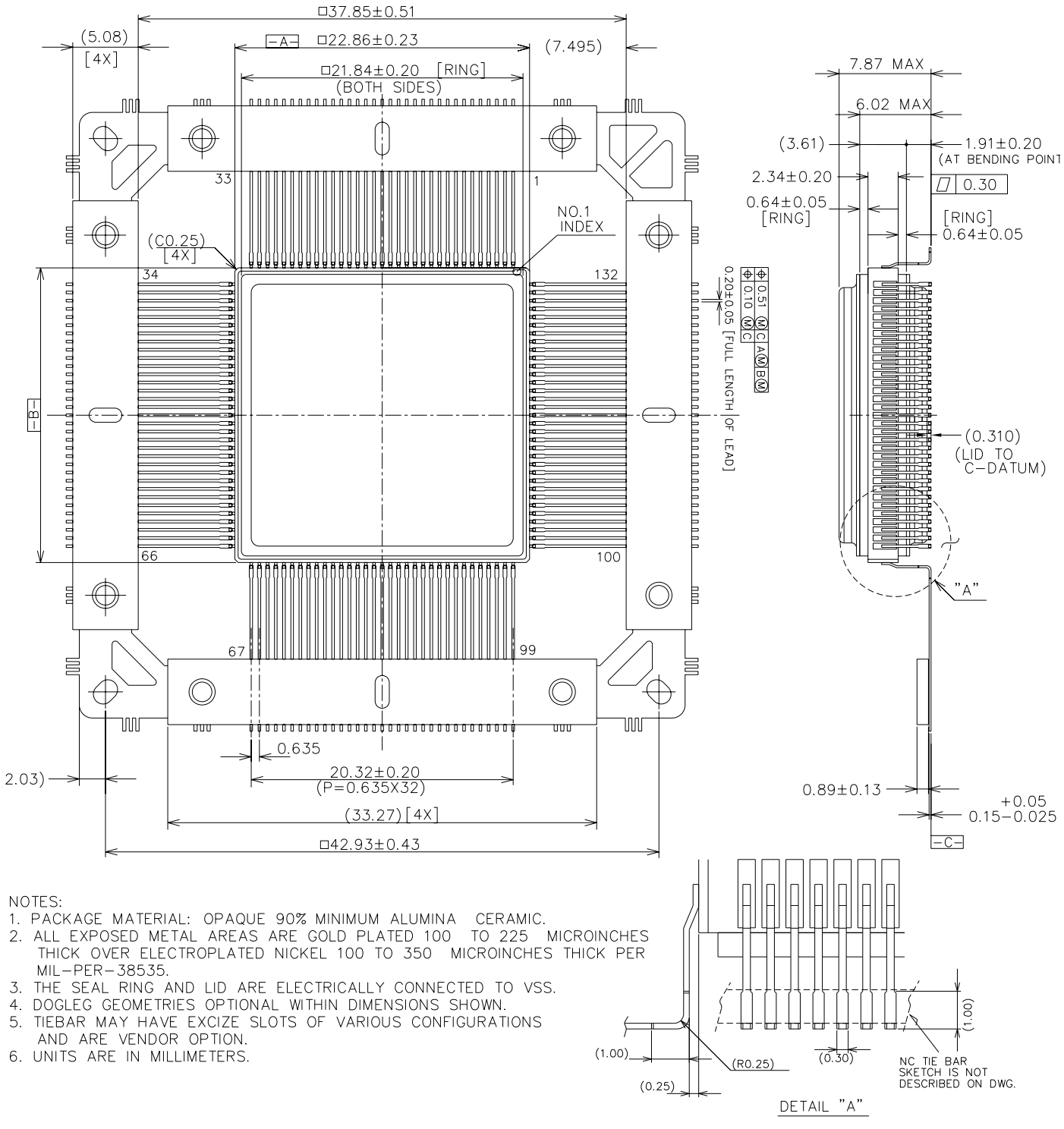
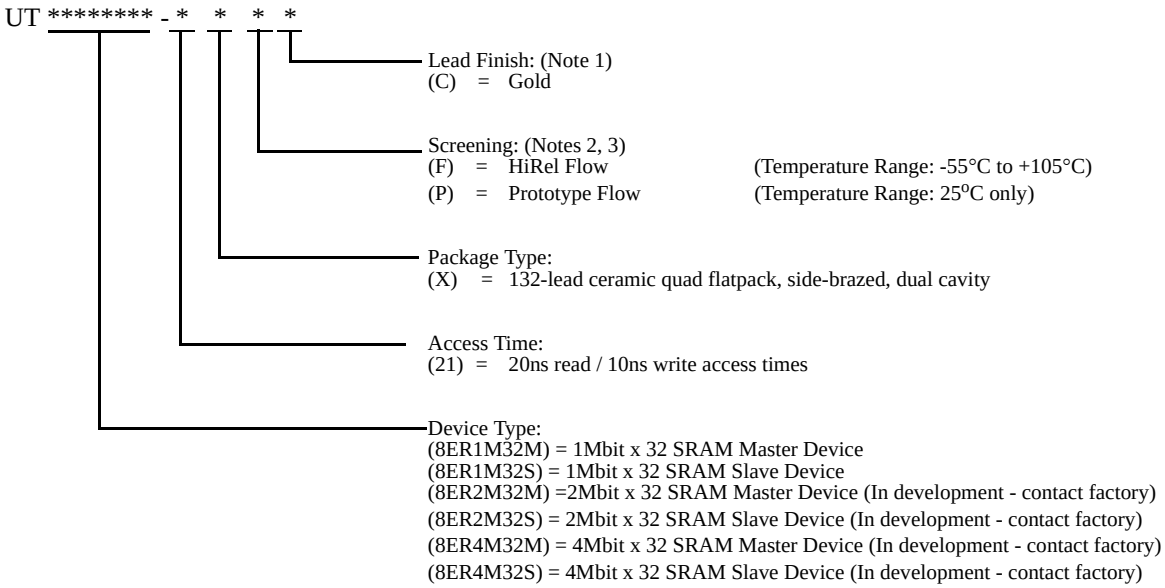


Figure 9. 132-lead Ceramic Quad Flatpack

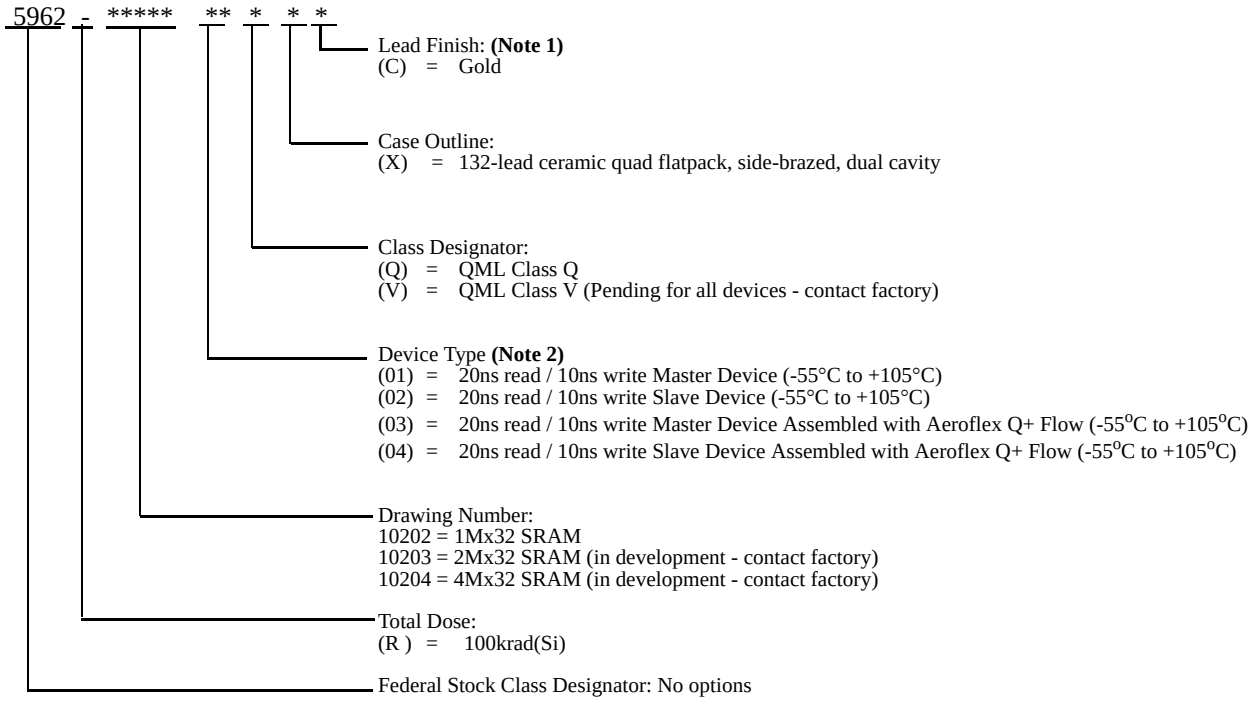
ORDERING INFORMATION

1M x 32 SRAM
2M x 32 SRAM
4M x 32 SRAM



Notes:
1. Lead finish is "C" (Gold) only.
2. Prototype Flow per Aeroflex Manufacturing Flows Document. Devices are tested at 25°C only. Lead finish is GOLD "C" only. Radiation is neither tested nor guaranteed.
3. HiRel flow per Aeroflex Manufacturing Flows Document. Radiation is neither tested nor guaranteed.

1M x 32 SRAM: SMD
2M x 32 SRAM: SMD
4M x 32 SRAM: SMD



Notes:

1.Lead finish is "C" (Gold) only.

2.Aeroflex's Q+assembly flow, as defined in section 4.2.2.d of the SMD, provides QML-Q product through the SMD that is manufactured with Aeroflex's standard QML-V flow.

Aeroflex Colorado Springs - Datasheet Definition

Advanced Datasheet - Product In Development

Preliminary Datasheet - Shipping Prototype

Datasheet - Shipping QML & Reduced Hi-Rel

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AEROFLEX
A passion for performance.

Our passion for performance is defined by three attributes represented by these three icons: solution-minded, performance-driven and customer-focused