8292-A,F,W•8293-A,F,W

## DESCRIPTION

The 8292 Decade Counter and 8293 Binary Counter are low power devices providing a wide variety of counter/storage register applications with a minimum number of packages.

The 8292 Decade Counter can be connected in the familiar BCD counting mode, in a divide-by-two and divide-by-five configuration or in the Bi-Quinary mode. The Bi-Quinary mode produces a square wave output which is particularly useful in frequency synthesizer applications.

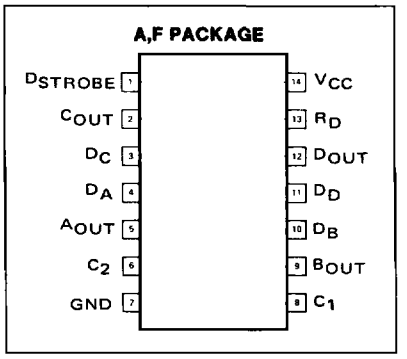
The 8293 Binary Counter may be connected as a divide-by-two, four, eight, or sixteen counter.

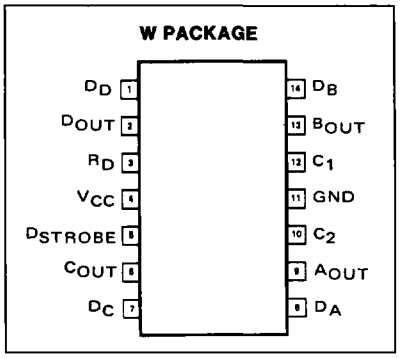
Both devices have strobed parallel-entry capability so that the counter may be set to any desired output state, A "1" or "0" at a data input will be transferred to the associated output when the strobe input is put at the "0" level. For additional flexibility, both units are provided with a reset input which is common to all four bits. A "0" on the reset line produces "0" at all four outputs.

The counting operation is performed on the falling (negative-going) edge of the input clock pulse.

Triggering requirements are compatible with any of the 8000 Series elements.

## PIN CONFIGURATION




## TRUTH TABLE

| | 8292 | | | | | | | | 8293 | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | BI QUINARY (5-2) | | | | DECADE(BCD) | | | | BINARY | | | |
| Input | $B_0$ | $C_0$ | $D_0$ | $A_0$ | $A_0$ | $B_0$ | $C_0$ | $D_0$ | $A_0$ | $B_0$ | $C_0$ | $D_0$ |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 2 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| 3 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 4 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 5 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 6 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |
| 7 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 |
| 8 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 9 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| 10 | | | | | | | | | 0 | 1 | 0 | 1 |
| 11 | | | | | | | | | 1 | 1 | 0 | 1 |
| 12 | | | | | | | | | 0 | 0 | 1 | 1 |
| 13 | | | | | | | | | 1 | 0 | 1 | 1 |
| 14 | | | | | | | | | 0 | 1 | 1 | 1 |
| 15 | | | | | | | | | 1 | 1 | 1 | 1 |

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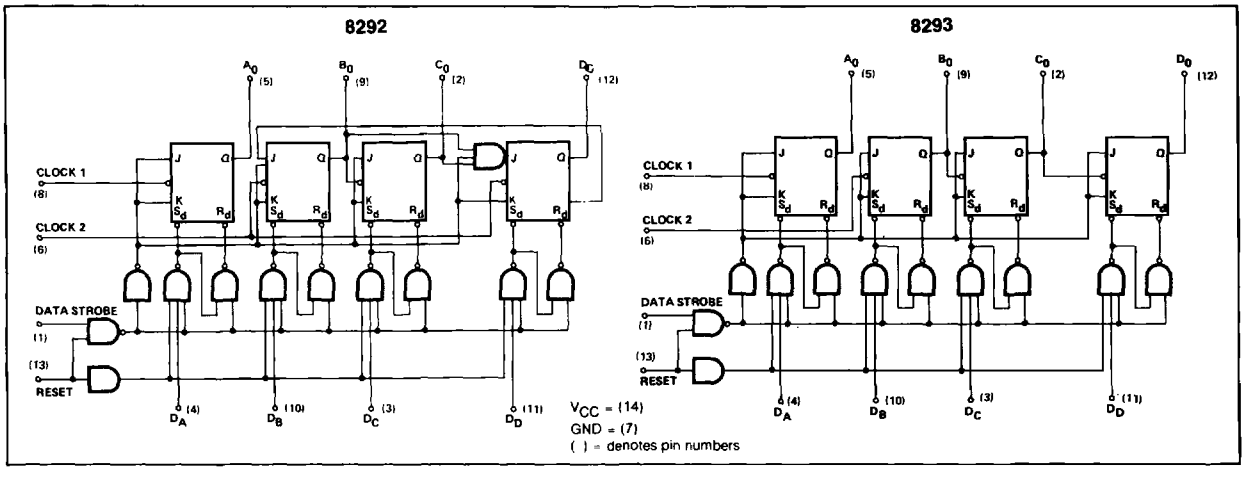
## SWITCHING CHARACTERISTICS $T_A$=25°C, $V_{CC}$ = 5V

| PARAMETER | | TEST CONDITIONS | LIMITS MIN | LIMITS TYP | LIMITS MAX | UNIT |
|---|---|---|---|---|---|---|
| Propagation delay time | | | | | | |
| $t_{on}$ | Turn-on time | | | | | |
| | Clock mode | All bits | | 37 | 55 | ns |
| | Strobed data | | | 80 | 100 | |
| $t_{off}$ | Turn-off time | | | | | |
| | Clock mode | All bits | | 32 | 55 | ns |
| | Strobed data | | | 80 | 100 | |
| $-t_w$ | Input pulse width | $V_{IN}$ = 0.8V: reset, clock 1 = 2V: clock 2 = $A_{out}$ | | 60 | 75 | ns |
| | Strobe | | | | | |
| | Reset | $V_{in}$, reset clock 1 = 2V: clock 2 = $A_{out}$ | | 45 | 60 | |
| $t_{release}$ | Release time | | | | | |
| | Strobe/reset | clock 2 = $A_{out}$ | | 80 | | |
| Toggle rate | | | 5 | 10 | | MHz |

NOTES:
1. This test guarantees the device will reliably trigger on a pulse with 75ns fall-time.

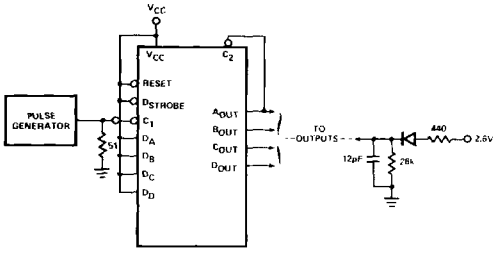
## LOGIC DIAGRAM

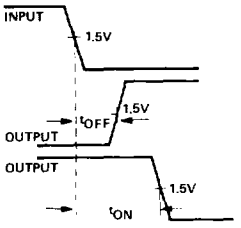



LOGIC

## AC TEST FIGURES AND WAVEFORMS

### CLOCK MODE $t_{on}/t_{off}$ DELAY

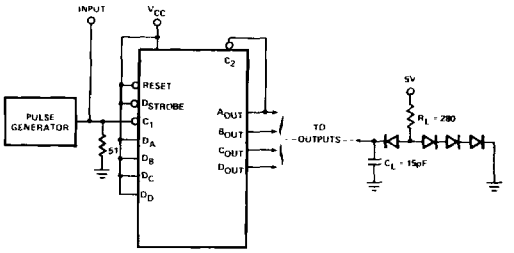



Input pulse.
Amplitude = 2.6V
P.W. = 30ns, 50% to 50%
$t_r = t_f$ = 5ns
PRR = 1MHz

NOTE:
1 $t_{on}$ and $t_{off}$ are measured from the clock input of each binary to the Q output of that binary.

### CLOCK MODE SWITCHING TEST

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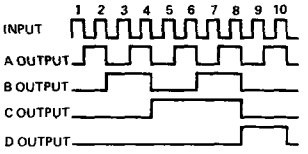
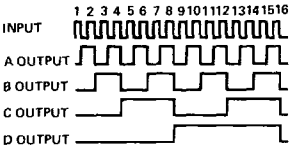
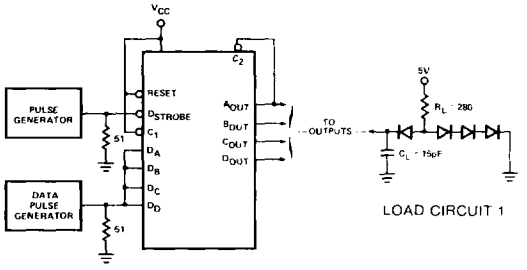



**8293**

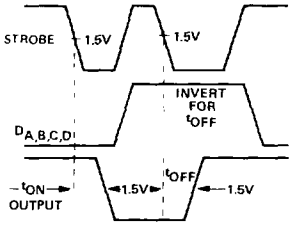



Input pulse.
Amplitude = 3.4V
P.W. = 100ns, 50% to 50%
PRR = 2.5MHz
$t_r$ = 20ns
$t_f$ = 75ns

### STROBED DATA $t_{on}/t_{off}$ DELAY



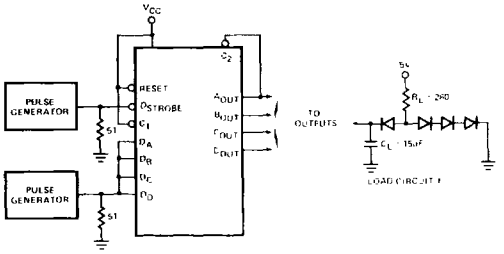

LOAD CIRCUIT 1

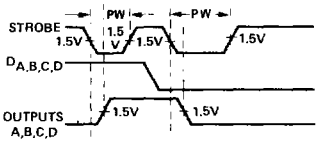



Strobe,
P.A. = 2.6V
P.W. = 300ns, 50% to 50%
PRR = 1MHz
$t_r$ $t_f$ 5ns

Data
P.A. = 2.6V
P.W. = 500ns, 50% to 50%
PRR = 500KHz
$t_r = t_f$ = 5ns

### MINIMUM STROBE PULSE WIDTH

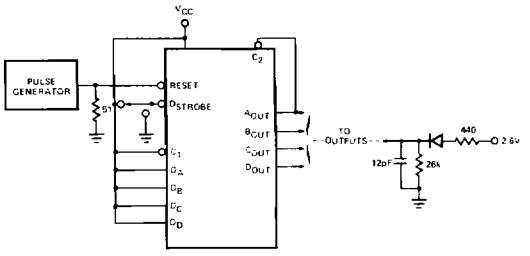


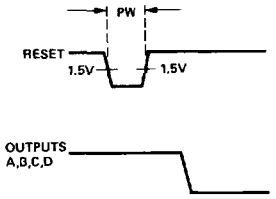




Input pulse
Amplitude = 2.6V
$t_r = t_f$ = 5ns max

## AC TEST FIGURES AND WAVEFORMS (CONT'D.)

### MINIMUM RESET PULSE WIDTH

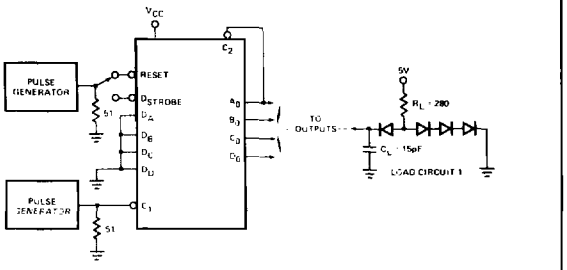


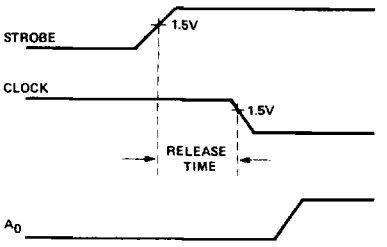




Input pulse
Amplitude 2.6V
$t_r = t_f = 5ns$ max

NOTE outputs must be previously brought high by placing a "Q" on the D strobe light.
A pulse generator may be substituted for the switch

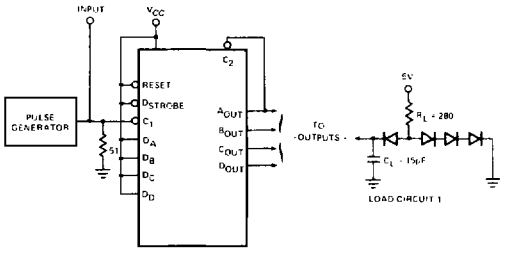
### STROBE/RESET RELEASE TIME




Clock, strobe/reset
Amplitude = 2.6V
PRR = 1MHz, 50% duty cycle
$t_r = t_f = 5ns$ max.

### TOGGLE RATE

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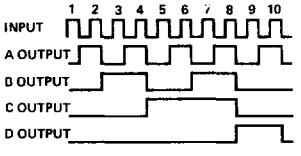
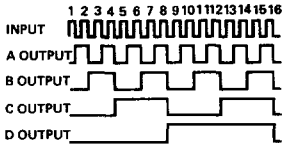



**8293**




Input pulse:
Amplitude = 2.6V
PRR = 5MHz, 50% duty cycle
$t_r = t_f = 5ns$ max.

NOTES:
1. All resistor values are in ohms
2. All capacitance values are in picofarads and include jig and probe capacitance
3. All diodes are 1N916.

LOGIC