MQ402-01

EPSON

Application Manual

Real Time Clock Module

RX-4591CF

Model	Product Number
RX-4591CF	Q414591A0000200

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Miniature Serial Interface RTC Module

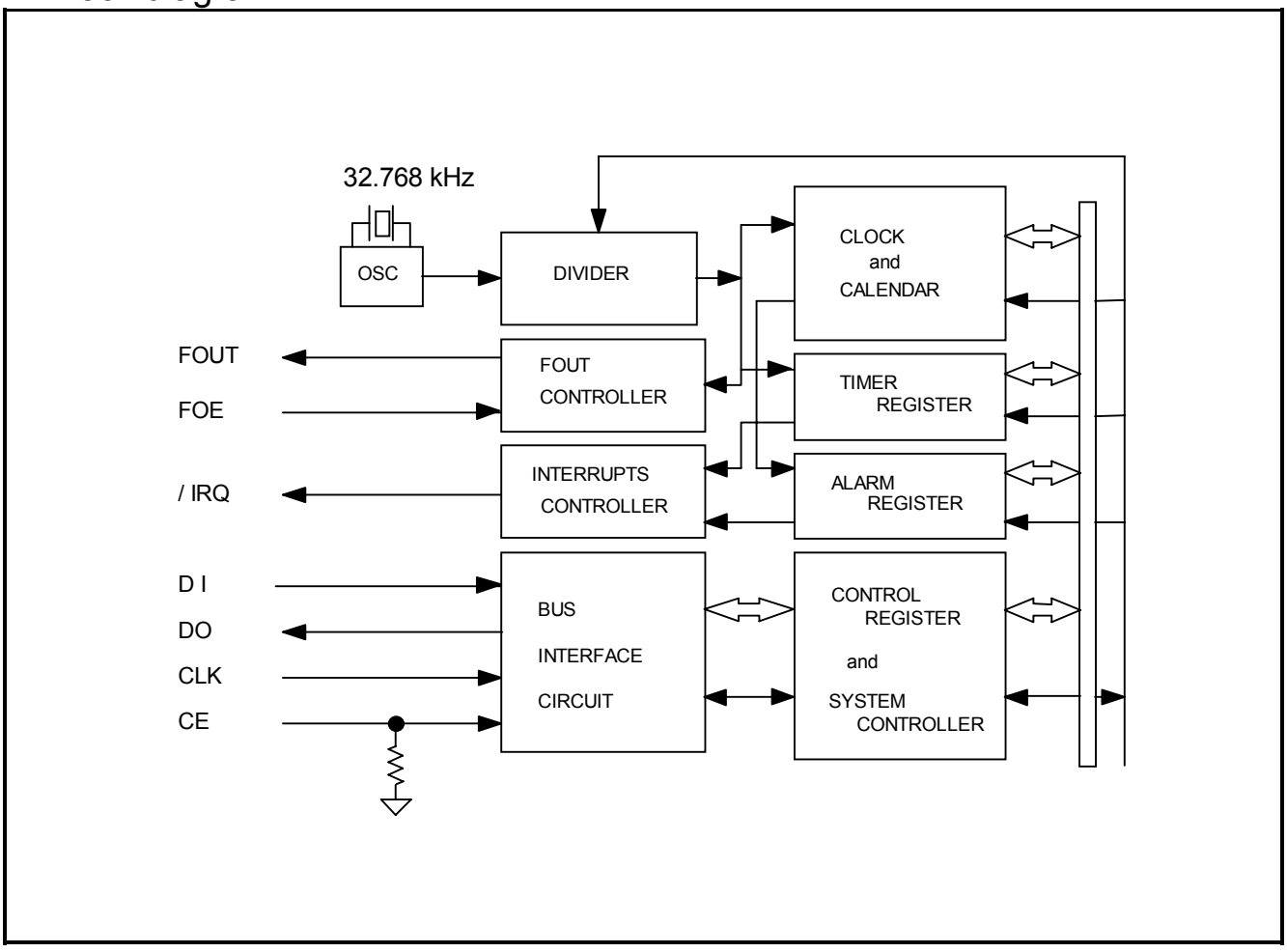
RX - 4591 CF

- Built-in 32.768 kHz crystal oscillator with frequency adjusted
- Serial interface in 4 lines form
  (possible to make it to 3 lines by wired-OR connecting DI and DO pins)
- Alarm interrupt function for day of the week, day, hour, and minute (/IRQ pin)
- Timer interrupt function (/IRQ pin)
- Time update interrupt function (second·minute, /AIRQ pin)
- OE function 32.768 kHz output (FOE, FOUT pins)
- Automatic adjustment for leap year (supports from year 2000 to 2099)
- Wide range of interface voltage between 1.6 V and 5.5 V
- Wide range of clock (retained) voltage between 1.2 V and 5.5 V
- Low current consumption at 0.3 μA / 3 V (Typ.)
- Available as small package (CF : SON−10 pin PKG.)

1. Overview

This module is a real-time clock with serial interface in 4 lines form (or 3 lines form). It has a built-in crystal oscillator. The module offers many functions such as Clock & Calendar circuitry with automatic leap year adjustment, interval timer, time update interrupt, and other rich functions like 32.768 kHz output. Because it is available in small package SON-22 pin in high density mounting, it is ideally suited for applications such as mobile phone, handy terminals and other small electronic systems.

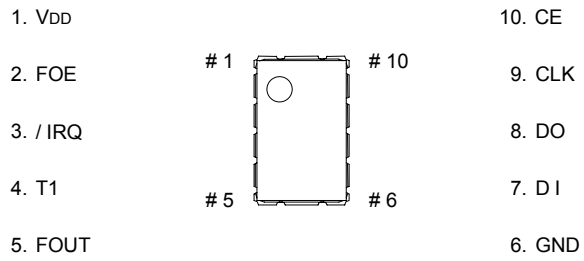
2. Block diagram



3. Terminal description

3.1. Terminal connections

RX - 4591 CF



SON - 10pin

3.2. Pin functions

Signal name	I / O	Signal description
CE	Input	This is a chip enabled input pin with the builit-in pull- down resistor. When the CE pin is "H" level, access to this RTC is possible. Also, when the chip is not selected, the DO pin is at the high impedance level, and the CLK and DI pins would not accept input.
CLK	Input	This is the shift clock input pin for serial data transfer. In the write mode, it takes in data from the DI pin using the CLK signal rise edge. In the read mode, it outputs data from the DO pin using the fall edge.
D I	Input	This is the data input pin for serial data transfer.
DO	Output	This is the data output pin for serial data transfer.
FOUT	Output	This is the C-MOS output pin with output control provided via the FOE pin. When FOE = "H" (high level), this pin outputs a 32.768-kHz signal. When output is stopped, the FOUT pin = "L" (low level).
FOE	Input	This is an input pin used to control the output mode of the FOUT pin. When this pin's level is high, the FOUT pin is in output mode. When it is low, output via the FOUT pin is stopped.
/ IRQ	Output	This is an open drain output pin for alarm and additional counter interrupt.
T1	–	This pin is used by the manufacturer for testing. Be sure to connect this pin to GND.
VDD	–	This pin connects to the plus side of the power.
GND	–	This pin connects to the minus side (ground) of the power.

Note: Be sure to connect a bypass capacitor rated at least 0.1 µF between VDD and GND.

4. Absolute maximum ratings

GND=0 V

Item	Symbol	Condition	Rating	Unit
Power voltage	V_{DD}	Between V_{DD} and GND	–0.3 to +6.5	V
Input voltage	V_{IN}	Input pin	GND–0.3 to V_{DD}+0.3	V
Output voltage (1)	V_{OUT1}	DO, FOUT pins	GND–0.3 to V_{DD}+0.3	V
Output voltage (2)	V_{OUT2}	/ IRQ pin	GND–0.3 to +6.5	V
Storage temperature	T_{STG}	Stored bare product after unpacking	–55 to +125	°C

5. Recommended operating functions

GND=0 V

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating power voltage	V_{DD}	–	1.6	3.0	5.5	V
Clock power voltage	V_{CLK}	–	1.2	3.0	5.5	V
Operating temperature	T_{OPR}	No condensation	–40	+25	+85	°C

6. Frequency characteristics

GND=0 V

Item	Symbol	Condition	Rating	Unit
Frequency precision	$\Delta f / f$	Ta= +25 °C, V_{DD}=3.0 V	5 ± 23 (*1) (*2)	$\times 10^{-6}$
Frequency voltage characteristics	f / V	Ta= +25 °C, V_{DD}=2.0 V to 5.0 V	± 2 Max.	$\times 10^{-6}$ / V
Frequency temperature characteristics	Top	Ta= –20 °C to +70 °C, V_{DD}= 3.0 V ; reference at +25 °C	+10 / –120	$\times 10^{-6}$
Oscillation start up time	t_{STA}	Ta= +25 °C, V_{DD}=3.0 V	3 Max.	s
Aging	fa	Ta= +25 °C, V_{DD}=3.0 V ; first year	± 5 Max.	$\times 10^{-6}$ / year

*1) This difference is 1 minute by 1 month. (excluding offset)

*2) Also,This precision includes shift of frequency by the solder handling of reflow.

7. Electrical characteristics

*If not specifically indicated, GND=0 V, V_{DD}=1.6 V to 5.5 V, Ta= –40 °C to +85 °C

7.1. DC electrical characteristics

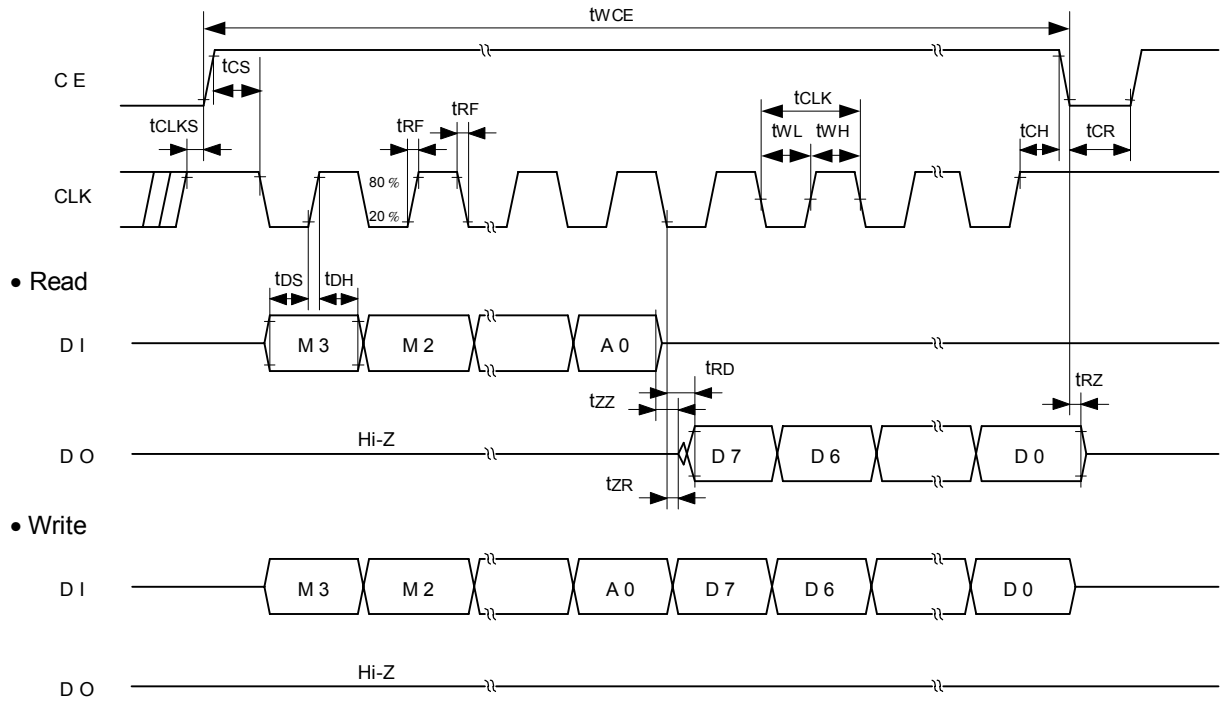
Item	Symbol	Condition			Min.	Typ.	Max.	Unit
Current consumption (1)	I_{DD1}	CE = GND /IRQ = V_{DD} FOUT ; Output OFF (low level)		V_{DD}=5 V		0.4	0.9	µA
Current consumption (2)	I_{DD2}			V_{DD}=3 V		0.3	0.8	
"H" input voltage	V_{IH1}	Input pin			0.70 × V_{DD}		V_{DD} + 0.3	V
	V_{IH2}	Input pin (5 V ± 10 %)			0.75 × V_{DD}		V_{DD} + 0.3	V
" L " input voltage	V_{IL1}	Input pin			GND – 0.3		0.30 × V_{DD}	V
	V_{IL2}	Input pin (5 V ± 10 %)			GND – 0.3		0.25 × V_{DD}	V
"H" Output voltage	V_{OH1}	DO pin	V_{DD} = 5 V, I_{OH} = –1 mA		4.5		5.0	V
	V_{OH2}		V_{DD} = 3 V, I_{OH} = –1 mA		2.2		3.0	
	V_{OH3}		V_{DD} = 3 V, I_{OH} = –100 µA		2.9		3.0	
	V_{OH4}	FOUT pin	V_{DD} = 5 V, I_{OH} = –1 mA		4.75		5.0	
	V_{OH5}		V_{DD} = 3 V, I_{OH} = –1 mA		2.6		3.0	
"L" Output voltage	V_{OL1}	DO pin	V_{DD} = 5 V, I_{OL} = 1 mA		GND		GND+0.5	V
	V_{OL2}		V_{DD} = 3 V, I_{OL} = 1 mA		GND		GND+0.8	
	V_{OL3}		V_{DD} = 3 V, I_{OL} = 100 µA		GND		GND+0.1	
	V_{OL4}	FOUT, /IRQ pins	V_{DD} = 5 V, I_{OL} = 1 mA		GND		GND+0.25	
	V_{OL5}		V_{DD} = 3 V, I_{OL} = 1 mA		GND		GND+0.4	
Input resistance (1)	R_{DWN1}	CE pin V_{IN} = V_{DD}	V_{DD}=5 V		75	150	300	kΩ
Input resistance (2)	R_{DWN2}		V_{DD}=3 V		150	300	600	
Input leakage current	I_{LK}	Input pin other than CE V_{IN} = V_{DD} or GND			–0.5		0.5	µA
Output leakage current	I_{OZ}	Output pin, V_{OUT} = V_{DD} or GND			–0.5		0.5	µA
Power supply detection voltage	V_{DET}	V_{DD} pin			1.6	1.8	2.0	V
	V_{LOW}	V_{DD} pin			1.1	1.2	1.4	

7.2. AC electrical characteristics

∗If not specifically indicated, GND=0 V, Ta= –40 °C to +85 °C

Item	Symbol	Condition	V_{DD} = 3 V ±10%		V_{DD} = 5 V ±10%		Unit
			Min.	Max.	Min.	Max.	
CLK clock cycle	t_{CLK}		500		350		ns
CLK H pulse width	t_{WH}		250		175		ns
CLK L pulse width	t_{WL}		250		175		ns
CLK rise and fall time	t_{RF}			100		50	ns
CLK setup time	t_{CLKS}		50		25		ns
CE setup time	t_{CS}		200		150		ns
CE hold time	t_{CH}		200		100		ns
CE recovery time	t_{CR}		300		200		ns
CE enable time	t_{WCE}			0.95		0.95	s
Write data setup time	t_{DS}		100		50		ns
Write data hold time	t_{DH}		100		50		ns
Read data delay time	t_{RD}	C_L=50 pF		200		150	ns
DO output switching time	t_{ZR}			50		25	ns
DO output disable time	t_{RZ}	C_L=50 pF R_L=10 kΩ		200		100	ns
DI/DO conflict avoiding time	t_{ZZ}		0		0		ns

Timing chart



∗ If DI and DO pins are wired-OR connected to make it to 3 lines form, secure tzz to avoid bus conflict.

8. How to use

8.1. Register table

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	note
0	SEC	○	40	20	10	8	4	2	1	∗3
1	MIN	○	40	20	10	8	4	2	1	∗3
2	HOUR	○	○	20	10	8	4	2	1	∗3
3	WEEK	○	6	5	4	3	2	1	0	∗3
4	DAY	○	○	20	10	8	4	2	1	∗3
5	MONTH	○	○	○	10	8	4	2	1	∗3
6	YEAR	80	40	20	10	8	4	2	1	–
7	RAM	•	•	•	•	•	•	•	•	∗4
8	MIN Alarm	AE	40	20	10	8	4	2	1	∗6
9	HOUR Alarm	AE	•	20	10	8	4	2	1	∗4, ∗6
A	WEEK Alarm	AE	6	5	4	3	2	1	0	∗4, ∗6
	DAY Alarm		•	20	10	8	4	2	1	
B	Timer Counter 0	128	64	32	16	8	4	2	1	∗7
C	Timer Counter 1	•	•	•	•	2048	1024	512	256	∗4, ∗7
D	Extension Register	**TEST1**	WADA	USEL	TE	○	**TEST3**	TSEL1	TSEL0	∗3, ∗5
E	Flag Register	VDET	VLOW	UF	TF	AF	ICNT	VLF	PON	∗1, ∗2
F	Control Register	**TEST2**	○	UIE	TIE	AIE	○	STOP	RESET	∗3, ∗5

Note When after the initial power-up or when the result of read out the VLF bit is "1" , initialize all registers, before using the module.
Be sure to avoid entering incorrect date and time data, as clock operations are not guaranteed when the data or time data is incorrect.

∗1) During the initial power-up, the VLF bit is set to "1".
And, all register values are undefined, so be sure to initialize all registers.

∗2) Only the writes clear to "0" is possible for UF,TF,AF, and VLF.

∗3) All bits marked with ' ○ ' are read-only bits. Their value when read is always "0".

∗4) Any bit marked with ' • ' is a RAM bit that can be used to read or write any data.

∗5) TEST1, TEST2, TEST3 bits are used by manufacture for testing. Be sure to set it to "0" before use.

∗6) When alarm is not used, addresses between 8 and A can be used as RAM (AIE = "0").

∗7) When the timer counter (addresses B and C) is read, the data value preset previously can be read.
When the timer is not used, addresses B and C can be used as RAM (TE,TIE = "0").

∗8) The first 4 bits that sets mode code in the serial communication specify R/W for Bank 0 and Bank 1.
(For details, see the [8.3. Read/Write of data] section.)

Mode	Setup Code
Read	8 h
Write	0 h

8.2. Register description

8.2.1. Clock and calendar registers (Reg-0 to Reg-6)

- Data format

  Data is in the BCD format. For example, if the SEC register is set to "0101 1001", this means 59 seconds. The time measurement is in 24-hour format (fixed).

- YEAR register and leap year

  The YEAR register becomes year 00 after year 99.

  Divide the YEAR register's 2-digit BCD by four, and if the remainder is 0, then this year is determined as the leap year. (Year 00 is processed as a leap year. This calendar expires in year 2099.)

- Day of the WEEK register

  The day of the WEEK register is made of 7 bits from 0 to 6. The bits are assigned as shown in the following table.

  Be sure not to set multiple days of week to "1".

bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Day of the week
0	0	0	0	0	0	**1**	Sunday
0	0	0	0	0	**1**	0	Monday
0	0	0	0	**1**	0	0	Tuesday
0	0	0	**1**	0	0	0	Wednesday
0	0	**1**	0	0	0	0	Thursday
0	**1**	0	0	0	0	0	Friday
1	0	0	0	0	0	0	Saturday

8.2.2. Alarm registers (Reg-8 to Reg-A)

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
8	MIN alarm	AE	40	20	10	8	4	2	1
9	HOUR alarm	AE	•	20	10	8	4	2	1
A	WEEK alarm	AE	6	5	4	3	2	1	0
	DAY alarm		•	20	10	8	4	2	1

You can set the day of the week, day, hour and minute for alarm. The WADA bit specifies which alarm of the WEEK alarm or the DAY alarm assign to the register A.

Bit 7 is the AE (Alarm Enable) bit for all the alarm registers. By using this bit, you can easily set the hourly alarm and the daily alarm. The day of the week alarm can be set to any multiple days of week.

When the AE bit is set to "0", the appropriate register and the clock register are compared; when the AE bit is set to "1" ("don't care"), the two registers are not compared because they are considered to have the same value.

When the alarm goes off, the AF (Alarm Flag) bit of Reg-E is set to "1"; if at this moment the AIE (Alarm Interrupt Enable) bit of Reg-F has been set to "1", the /IRQ pin is set to the low level and the interrupt signal occurs. If the AIE bit has been set to "0", the alarm interrupt output from the /IRQ pin is prohibited.

If alarm interrupt is not used, then addresses 8 to A can be used as memory registers. In this case, set the AIE bit to "0" to prohibit usage of the alarm and alarm interrupt.

- The relationship between the day of the week alarm bit and each day of the week

bit	bit 6	bit 5	Bit 4	bit 3	bit 2	bit 1	bit 0
Day of the week	Saturday	Friday	Thursday	Wednesday	Tuesday	Monday	Sunday

8.2.3. Timer counter (Reg-B and Reg-C)

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
B	Timer counter 0	128	64	32	16	8	4	2	1
C	Timer counter 1	•	•	•	•	2048	1024	512	256

This register controls 12 bits of internal preset-able down counter used for timer interrupt.
TSEL0 and TSEL1 of Reg-D specify the count cycle of the down counter (source clock). Timer counter 0 and timer counter 1 specify the preset value of the down counter.

When the TE bit of Reg-D is set to "0, The presetable counter loads the written data to the timer counter (It is initial value.), and then stops the count down. Afterwards, when the TE bit set to 1, count down starts.

Using a source clock cycle, the down counter continues the countdown. When the data becomes zero, the TF (Timer Flag) of Reg-E is set to "1". At this moment, if the TIE bit (Timer Interrupt Enable) of Reg-F was set to 1 beforehand, the /IRQ pin is asserted low for generate the interrupt signal.
When the TIE bit is set to "0", output from the /IRQ pin is prohibited.

Next, it reloads the data of timer counter register and restarts the countdown (repeat operation).
But, even if write 1 to the TE bit, and write 0 to the timer counter, timer interrupt from the /TIRQ pin is not generated. In order to operate timer expectedly, you should set the TE bit and the TIE bit adequately.

If timer interrupt is not used, then addresses B and C may be used as memory registers. In this case, set TE bit and TIE bit to "0", to prohibit timer operation and timer interrupts.

• Timer interrupt and source clock selection

TSEL1	TSEL0	Source clock
0	0	4096 Hz
0	1	64 Hz
1	0	1 Hz
1	1	Update in minutes

• Timer interrupt interval

Timer counter setting value	Source clock			
	4096 Hz	64 Hz	1 Hz	Update in minutes
0	–	–	–	–
1	244.14 μs	15.625 ms	1 s	1 min
2	488.28 μs	31.25 ms	2 s	2 min
⋮	⋮	⋮	⋮	⋮
41	10.010 ms	640.63 ms	41 s	41 min
82	20.020 ms	1.281 s	82 s	82 min
128	31.250 ms	2.000 s	128 s	128 min
192	46.875 ms	3.000 s	192 s	192 min
205	50.049 ms	3.203 s	205 s	205 min
320	78.125 ms	5.000 s	320 s	320 min
410	100.10 ms	6.406 s	410 s	410 min
640	156.25 ms	10.000 s	640 s	640 min
820	200.20 ms	12.813 s	820 s	820 min
1229	300.05 ms	19.203 s	1229 s	1229 min
1280	312.50 ms	20.000 s	1280 s	1280 min
1920	468.75 ms	30.000 s	1920 s	1920 min
2048	500.00 ms	32.000 s	2048 s	2048 min
2560	625.00 ms	40.000 s	2560 s	2560 min
3200	0.7813 s	50.000 s	3200 s	3200 min
3840	0.9375 s	60.000 s	3840 s	3840 min
⋮	⋮	⋮	⋮	⋮
4095	0.9998 s	63.984 s	4095 s	4095 min

8.2.4. Control register and flag register (between Reg-D and Reg-F)

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
D	Extension register	TEST	WADA	USEL	TE	○	○	TSEL1	TSEL0
E	Flag register	VDET	VLOW	UF	TF	AF	ICNT	VLF	PON
F	Control register	TEST	○	UIE	TIE	AIE	○	STOP	RESET

- TEST bit: This bit is used by manufacture for testing.
  Be sure to set this bit to "0". Be careful not to set this bit to "1" when writing to other bits of Reg-D.
  When CE pin goes to L, TEST is cleared .

- WADA bit (WEEK Alarm / DAY Alarm)
  This bit sets either the WEEK alarm or the DAY alarm. When this bit is 0, the Reg-A is re-assigned to the WEEK alarm register. And when this bit is 1, the Reg-A is re-assigned to the DAY alarm register.

- USEL bit (Update Interrupt Select)
  Specify the occurrence timing of time update interrupt.
  [Selection of timing for time update interrupt]

USEL	Timing	Auto recovery time
0	Update in seconds	7.813 ms
1	Update in minutes	7.813 ms

- TE bit (Timer Enable)
  When the TE bit is 0, The presetable counter loads the written data to the timer counter (It is initial value.), and then stops the count down. And when the TE bit is 1, count down starts.

- VDET (Voltage Detect)
  When power supply is higher than VDET voltage, this bit shows 0. And when power supply is lower than VDETvoltage, this bit shows 1. But in this case, this bit continues keeping 1 till it is cleared by 0.
  This bit is not affected by another bits (STOP, RESET).

- VLOW (Voltage Low)

  When power supply is higher than VLOW voltage, this bit shows 0. And when power supply is lower than VLOW voltage, this bit shows 1. But in this case, this bit continues keeping 1 till it is cleared by 0.
  This bit is not affected by another bits (STOP, RESET).

- AF bit, TF bit, and UF bit (Alarm Flag, Timer Flag, Update Flag)
  When the alarm occurs , the AF bit is set to 1. When the data is just zero, the TF (Timer Flag) of Reg-E is set to 1. At the end of time update, the UF bit is set. These data 1 is retained until writing over them with 0. You cannot write "1" over these bits.

- AIE bit, TIE bit, and UIE bit (Alarm, Timer, Update Interrupt Enable)
  These bits control whether or not to generate interrupt signal from IRQpin, when alarm, timer, or time update interrupt event occurs. AIE corresponds to alarm interrupt, TIE corresponds to timer interrupt, and UIE corresponds to time update interrupt.

- ICNT (Invalid Counter Data)

  When crystal oscillation is stopped by for example down of supply voltage, this bit shows 1.
  But in this case, this bit continues keeping 1 till it is cleared by 0.
  This bit is not affected by another bits (STOP, RESET).

- VLF (Voltage Low Flag)
  This bit shows the logic sum of each bit (VLOW, ICNT, PON). In this case, this bit continues keeping 1 till it is cleared by 0. This bit is not affected by another bits (STOP, RESET).

- PON bit (Power On Reset)

  When the initial power-up occurs, or device returns from a blackout or such as, this bit shows 1.
  And this case, this bit continues keeping 1 till it is cleared by 0.
  This bit is not affected by another bits (STOP, RESET).

- STOP bit
  When this bit is set to "1", the operation of counting up the seconds in the Clock & Calendar circuitry is stopped, which stops the clock. When this bit is set to "0", the clock resumes its operation.

- RESET bit
  When this bit is set 1, clock update was stop and clock data (except seconds digits) is reset for 00 year January 1day Sunday 00hour 00minutes. When CE terminal turned into L, this bit is cleared automatically. After using the RESET function, set the all clock and calendar data.

8.3. Read/Write of data

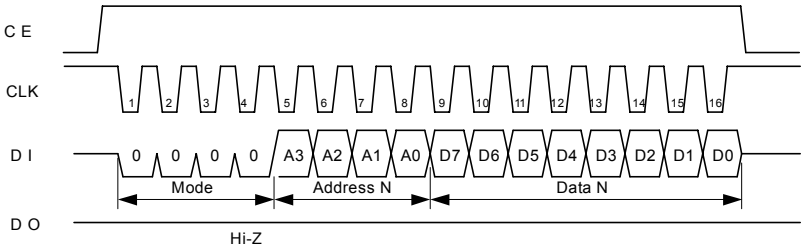
For both read and write, first set up chip condition (internally CE="H") to CE0="H" and CE1="H", then specify the 4-bits address, and finally read or write in 8-bits units.

Both read and write use MSB-first. In continuous operation, objected address is auto incremented.

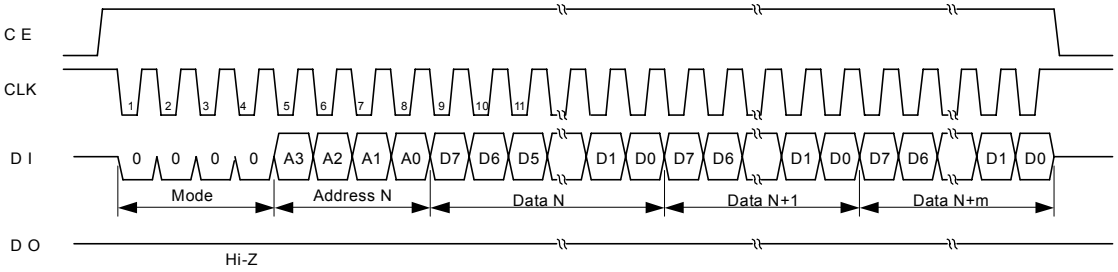
Auto incrementing of the address is cyclic, so address "F" is followed by address "0".

8.3.1. Write of data

1) One-shot writing



2) Continuous writing

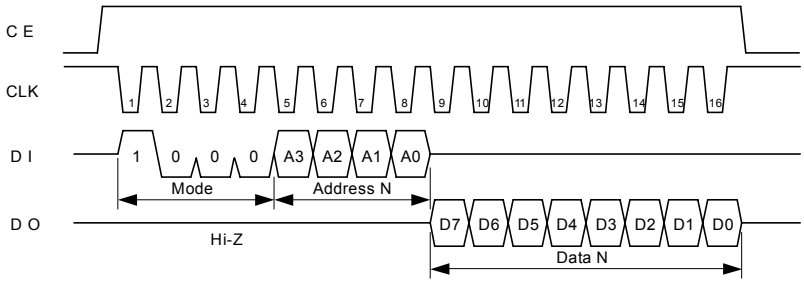


*When writing data, the data needs to be entered in 8-bits units.

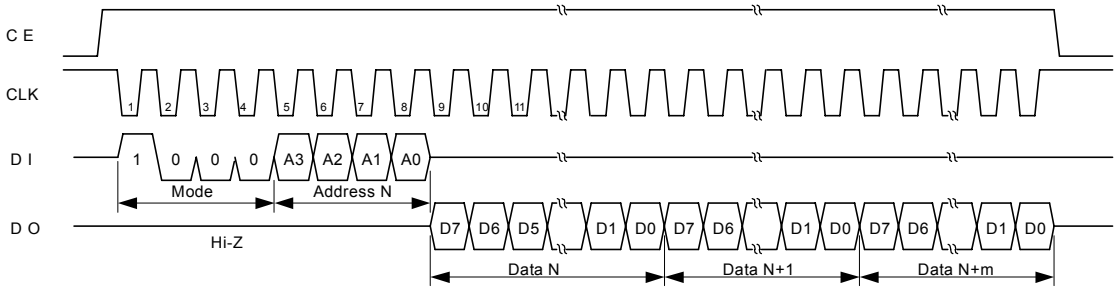
If the input of data in 8-bits unit is not completed before CE input falls, the 8-bits data will not be written properly at the time CE input falls.

8.3.2. Read of data

1) One-shot reading



2) Continuous reading



8.3.3. Write/Read mode setting code for each bank

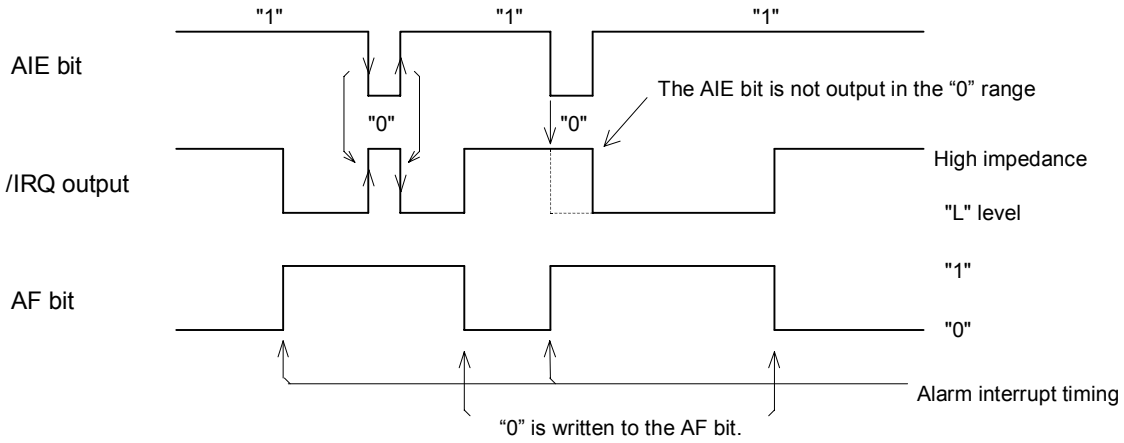
Mode	Setup Code
Read	8 h
Write	0 h

*In the mode setting code, if a value other than those listed is used, the subsequent data will be ignored and the DO pin remains in the Hi-z state.

8.4. Alarm interrupt / Timer interrupt

80.4.1. Alarm interrupt

When the alarm matches and AIE=1, the /IRQ pin outputs "L"; when AIE=0, the /IRQ pin is at the high impedance level. Alarm data is compared when update occurs just in minutes digits.



- How to use

The day of the week, day, hour and minute can be set.
WADA bit sets either the WEEK alarm or the DAY alarm. For the day of the week, multiple days can be set at one time. To avoid unintended hardware interrupt during the alarm setup, it is recommended that AIE bit be initially set to "0".
Then, set up the alarm data, and apply zero clear to the AF flag in order to initialize (with certainty) the alarm circuitry. Afterward, set the AIE bit to "1". If you desire no hardware interrupt, set the AIE bit to "0", and monitor the AF bit with software as required.

- Usage example

1) Set the alarm to go off at 6 pm tomorrow.

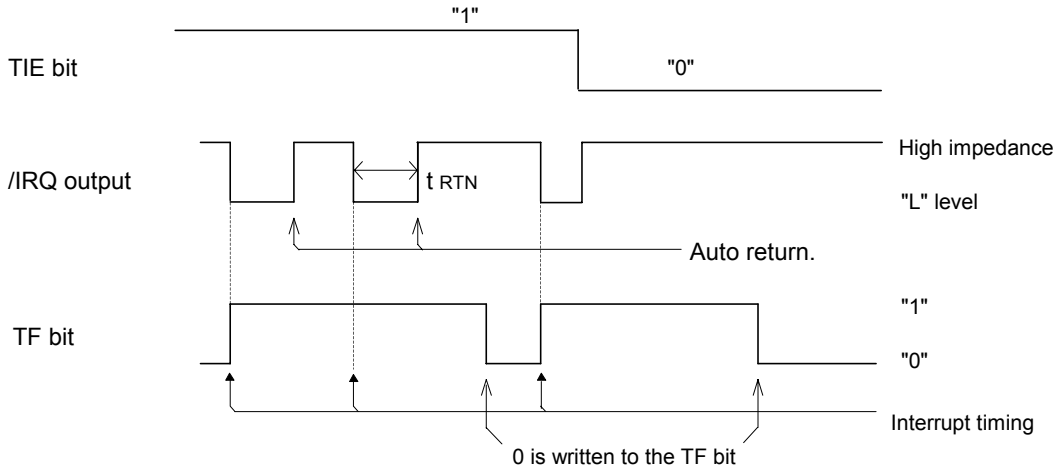
· Write "0" to the AIE bit.
· Write "00h" to the MIN alarm register.
· Write "18h" to the HOUR alarm register.
·· Write tomorrow’s date to the WEEK/DAY alarm register.
· Write "1" to the WADA bit (selecting the DAY alarm).
· Clear the AF bit to zero.
· Write "1" to the AIE bit.

2) Set the alarm to go off at 6 am every morning except Saturdays and Sundays.

· Write "0" to the AIE bit.
· Write "00h" to the MIN alarm register.
· Write "06h" to the HOUR alarm register.
· Write "3Eh" to the WEEK/DAY alarm register.
· Write "0" to the WADA bit (selecting the WEEK alarm).
· Clear the AF bit to zero.
· Write "1" to the AIE bit.

8.4.2. Timer interrupt

· If TIE="1" when interrupt occurs, the /IRQ pin outputs "L".
· If TIE="0" when interrupt occurs, the /IRQ pin enters the high impedance state and the TF bit becomes "1", and remains so.



∗ Automatic return

The automatic return time (tRTN) is determined by the source clock specified in Reg-D.

Source clock	Automatic return time (tRTN)
4096 Hz	122 μs
64 Hz	7.813 ms
1 Hz	7.813 ms
Update in minutes	7.813 ms

• Timer measurement error

Because the timer error is +0/-1 cycle time of the selected source clock, the timer time is following range.

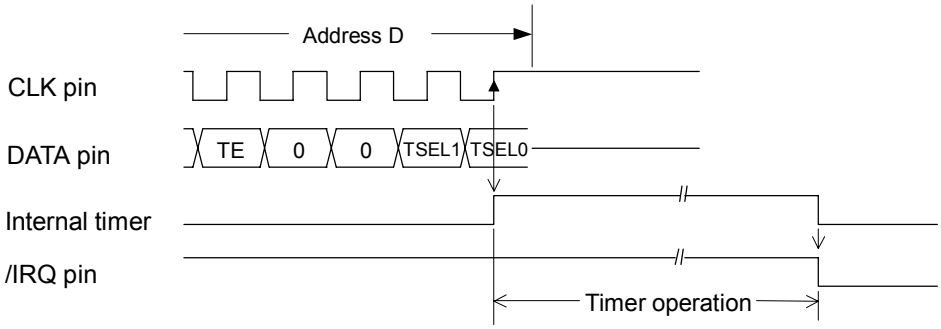
(Timer time(∗). – Source clock period time) to (Timer time.)

∗) Timer time = Source clock cycle × Value of the timer counter.

Now, the actual time of the timer is the above time, plus the communication duration of the serial data transfer clock.

• Timer start timing

In the data write mode, the timer starts counting from the rise edge of the CLK when writing to address D as shown in the following time chart.

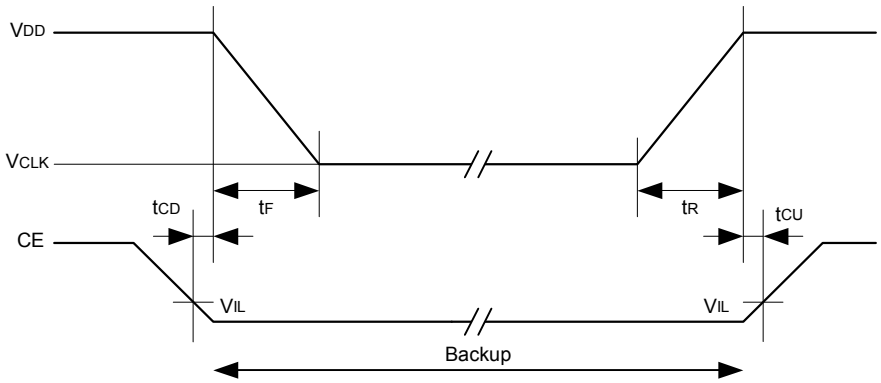


• How to use the /IRQ pin is asserted low for generate the interrupt signal.

At the cycle (source clock) specified in the timer interrupt setup register, the countdown starts from the value of the timer counter. When the data becomes zero, the /IRQ pin is asserted "L" for generate the interrupt signal. It can be used as an interval timer between a minimum of 1/4096 second to a maximum of 4095 minutes. To avoid unintended hardware interrupt during the timer setup, setting both TF bit and TIE bit, in the beginning, is recommended.

If you do not want to use any timer interrupt, set TIE bit to "0", and monitor the TF bit with software as required.

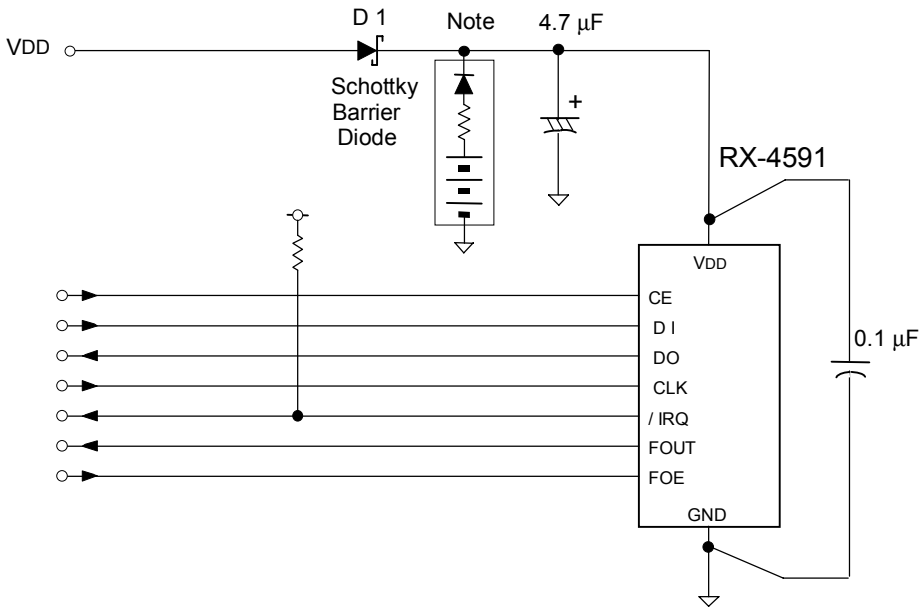
8.6. Shifting to backup and returning



Item	Symbol	Condition	Min.	Typ.	Max.	Unit
CE time before power drop	tCD	-	0			µs
Power drop time	tF	-	2			µs/ V
Power rise time	tR	-	1			µs/ V
CE time after power rise	tCU	-	0			µs

* When RTC switch into the backup-mode, CE keeps low level sure and, set the RTC into a disable state.

8.7. External connection example



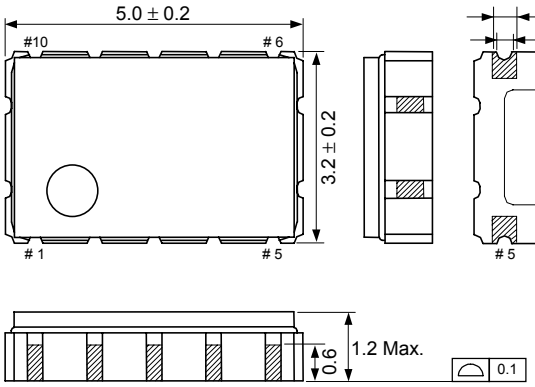
Note :
Use the secondary battery or a lithium battery. If using the secondary battery, a diode is not necessary. If using a lithium battery, a diode is necessary. For information on resistance value, please consult the battery manufacturer.

9. External dimension / Marking layout

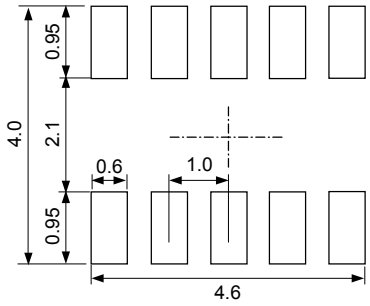
9.1. External dimensions

RX - 4591 CF (SON-10pin)

• External dimensions



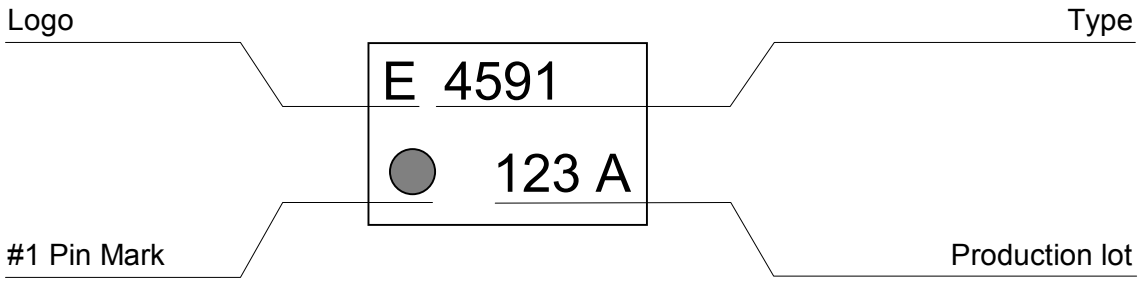
• Recommended soldering pattern



Unit : mm

9.2. Marking layout

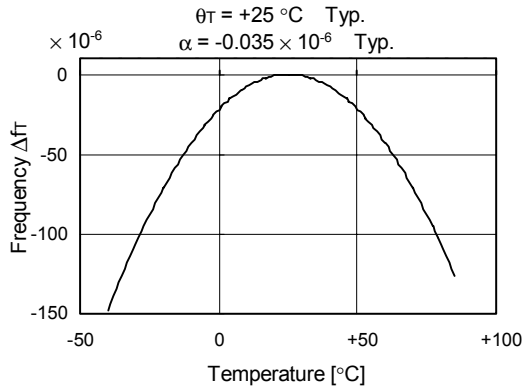
RX - 4591 CF (SON-10pin)



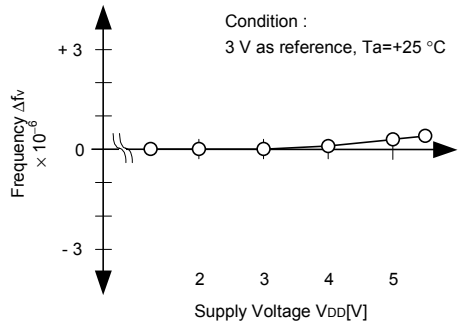
∗ Contents displayed indicate the general markings and display, but are not the standards for the fonts, sizes and positioning.

10. Reference data

(1) Example of frequency and temperature characteristics



(2) Example of frequency and voltage characteristics



[Finding the frequency stability]

1. Frequency and temperature characteristics can be approximated using the following equations.

$\Delta f_T = \alpha (\theta_T - \theta_X)^2$

Δf_T		Frequency deviation in any temperature
α	/ °C^2)	Coefficient of secondary temperature $(-0.035 \pm 0.005) \times 10^{-6}$ / °C^2
θ_T	°C)	Ultimate temperature (+25±5 °C)
θ_X	°C)	Any temperature

2. To determine overall clock accuracy, add the frequency precision and voltage characteristics.

$\Delta f/f = \Delta f/fo + \Delta f_T + \Delta f_V$

$\Delta f/f$	Clock accuracy (stable frequency) in any temperature and voltage
$\Delta f/fo$	Frequency precision
Δf_T	Frequency deviation in any temperature
Δf_V	Frequency deviation in any voltage

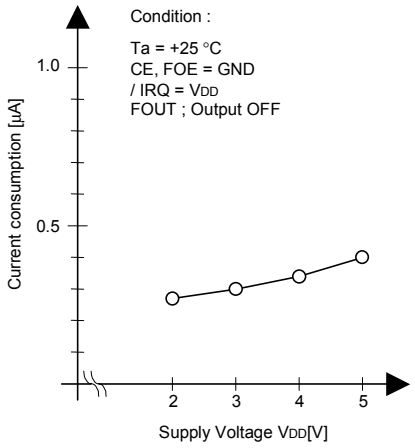
3. How to find the date difference

Date difference = $\Delta f/f \times 86400$ (seconds)

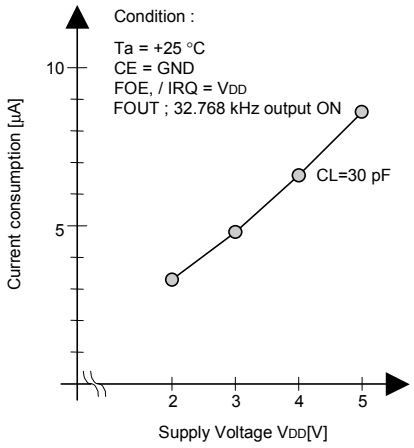
* For example: $\Delta f/f = 11.574 \times 10^{-6}$ is an error of approximately 1 second/day.

(3) Current and voltage consumption characteristics

(3-1) Current consumption when non-accessed (i) when FOUT=OFF



(3-2) Current consumption when non-accessed (ii) when FOUT=32.768 kHz



11. Application notes

1) Notes on handling

This module uses a C-MOS IC to realize low power consumption. Carefully note the following cautions when handling.

(1) Static electricity

While this module has built-in circuitry designed to protect it against electrostatic discharge, the chip could still be damaged by a large discharge of static electricity. Containers used for packing and transport should be constructed of conductive materials. In addition, only soldering irons, measurement circuits, and other such devices which do not leak high voltage should be used with this module, which should also be grounded when such devices are being used.

(2) Noise

If a signal with excessive external noise is applied to the power supply or input pins, the device may malfunction or "latch up." In order to ensure stable operation, connect a filter capacitor (preferably ceramic) of greater that 0.1F as close as possible to the power supply pins (between VDD and GNDs). Also, avoid placing any device that generates high level of electronic noise near this module.

* Do not connect signal lines to the shaded area in the figure shown in Fig. 1 and, if possible, embed this area in a GND land.

(3) Voltage levels of input pins

When the input pins are at the mid-level, this will cause increased current consumption and a reduced noise margin, and can impair the functioning of the device. Therefore, try as much as possible to apply the voltage level close to VDD or GND.

(4) Handling of unused pins

Since the input impedance of the input pins is extremely high, operating the device with these pins in the open circuit state can lead to unstable voltage level and malfunctions due to noise. Therefore, pull-up or pull-down resistors should be provided for all unused input pins.

2) Notes on packaging

(1) Soldering heat resistance.

If the temperature within the package exceeds +260 °C, the characteristics of the crystal oscillator will be degraded and it may be damaged. The reflow conditions within our reflow profile is recommended. Therefore, always check the mounting temperature and time before mounting this device. Also, check again if the mounting conditions are later changed.

* See Fig. 2 profile for our evaluation of Soldering heat resistance for reference.

(2) Mounting equipment

While this module can be used with general-purpose mounting equipment, the internal crystal oscillator may be damaged in some circumstances, depending on the equipment and conditions. Therefore, be sure to check this. In addition, if the mounting conditions are later changed, the same check should be performed again.

(3) Ultrasonic cleaning

Depending on the usage conditions, there is a possibility that the crystal oscillator will be damaged by resonance during ultrasonic cleaning. Since the conditions under which ultrasonic cleaning is carried out (the type of cleaner, power level, time, state of the inside of the cleaning vessel, etc.) vary widely, this device is not warranted against damage during ultrasonic cleaning.

(4) Mounting orientation

This device can be damaged if it is mounted in the wrong orientation. Always confirm the orientation of the device before mounting.

(5) Leakage between pins

Leakage between pins may occur if the power is turned on while the device has condensation or dirt on it. Make sure the device is dry and clean before supplying power to it.

Fig. 1 : Example GND Pattern

RX - 4591 CF

(SON - 10pin)

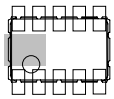
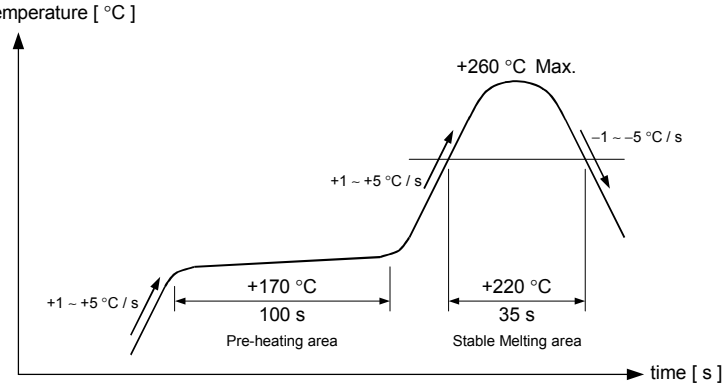


Fig. 2 : Reference profile for our evaluation of Soldering heat resistance.



* In addition, please confirm the Notes of an individual specification.

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