TMS4132 TI
C 21026

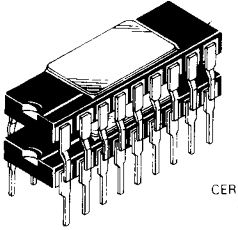
MOTOROLA

MCM4132

MOS

(N-CHANNEL, SILICON-GATE)

32,768-BIT DYNAMIC RANDOM ACCESS MEMORY



L SUFFIX
SIDEBRAZE
CERAMIC PACKAGE
CASE 749-01

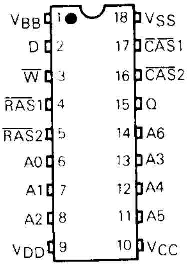
32,768 × 1 BIT DYNAMIC RAM

The MCM4132 is a 32,768-bit high-speed Dynamic Random Access Memory designed for high-performance, low-cost applications in mainframe and buffer memories and peripheral storage. Organized as 32,768 one-bit words and fabricated using Motorola's highly reliable N-channel double-polysilicon technology, this device optimizes speed, power, and density tradeoffs.

The MCM4132 consists of two MCM4116 16,384-bit high-speed MOS dynamic Random Access Memories, each in its own package permanently connected, pin-for-pin, one on top of the other. The lower package is referenced as Module 1, the upper as Module 2, thereby resulting in an 18-pin memory device, organized as 32,768 words of one bit each, with essentially the same characteristics of the MCM4116.

- 32,768 × 1 Organization
- ± 10% Tolerance on All Power Supplies
- All Inputs Are Fully TTL Compatible
- Three-State Fully TTL Compatible Output
- Common I/O Capability when using "Early-Write" Mode
- Flexible Timing with Read-Modify-Write, $\overline{RAS}$-Only Refresh, and Page-Mode Capability
- On-Chip Latches for Addresses and Data In
- Fast Access Time Options:
  - 150 ns – MCM4132L15
  - 200 ns – MCM4132L20
  - 250 ns – MCM4132L25
  - 300 ns – MCM4132L30

PIN ASSIGNMENT



NOTE: $\overline{RAS}_1$ and $\overline{CAS}_1$ indicate bottom device.

PIN NAMES

A0-A6	Address Inputs
$\overline{CAS}_1$	Column Address Strobe, Module 1
$\overline{CAS}_2$	Column Address Strobe, Module 2
D	Data In
Q	Data Out
$\overline{RAS}_1$	Row Address Strobe, Module 1
$\overline{RAS}_2$	Row Address Strobe, Module 2
$\overline{W}$	Read/Write Input
V_{BB}	Power (– 5 V)
V_{CC}	Power (+5 V)
V_{DD}	Power (+ 12 V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{BB}	V_{in}, V_{out}	– 0.5 to + 20	V
Operating Temperture Range	T_A	0 to + 70	°C
Storage Temperature Range	T_{stg}	– 65 to + 150	°C
Power Dissipation	P_D	1.0	W
Data Out Current	I_{out}	50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

CAPACITANCE

($f = 1.0$ MHz, $T_A = 25°C$, $V_{CC} = 5$ V, periodically sampled rather than 100% tested.)

Parameter	Symbol	Typ	Max	Unit	Notes
Input Capacitance (A0-A5), D	C_{I1}	4.0	10	pF	8
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	C_{I2}	8.0	13	pF	8
Output Capacitance (Q)	C_O	5.0	14	pF	8

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avod application of any voltage higher than maximum rated voltages to this high impedance circuit.

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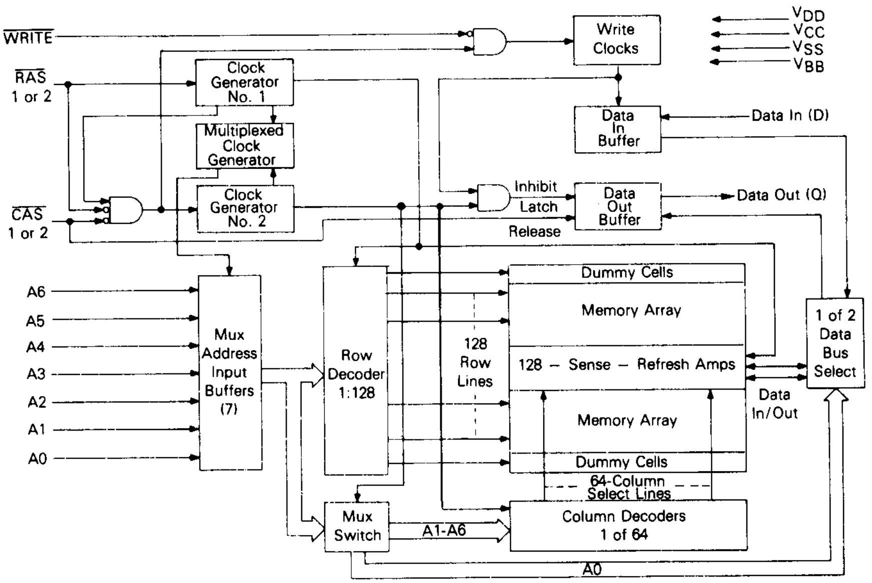
BLOCK DIAGRAM



DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage	V_{DD} V_{CC} V_{SS} V_{BB}	10.8 4.5 0 −4.5	12.0 5.0 0 −5.0	13.2 5.5 0 −5.5	V	1 1, 2 1 1
Logic 1 Voltage, All Inputs	V_{IH}	2.4	–	7.0	V	1
Logic 0 Voltage, All Inputs	V_{IL}	−1.0	–	0.8	V	1

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit	Notes
1 Chip Selected					
Average V_{DD} Power Supply Current	I_{DD1}	–	36.5	mA	4
V_{CC} Power Supply Current	I_{CC}	–	–	mA	5
Average V_{BB} Power Supply Current	$I_{BB1,3}$	–	300	μA	
Standby V_{BB} Power Supply Current	I_{BB2}	–	200	μA	
Standby V_{DD} Power Supply Current	I_{DD2}	–	3	mA	6
Average V_{DD} Power Supply Current During "$\overline{RAS}$ Only" Cycles	I_{DD3}	–	28.5	mA	4
Input Leakage Current (Any Input)	$I_{I(L)}$	–	10	μA	
Output Leakage Current	$I_{O(L)}$	–	10	μA	6, 7
Output Logic 1 Voltage @ $I_{out} = -5$ mA	V_{OH}	2.4	–	V	2
Output Logic 0 Voltage @ $I_{out} = 4.2$ mA	V_{OL}	–	0.4	V	
2 Chip Selected (17)					
Average V_{DD} Power Supply Current	I_{DD1}	–	70	mA	4
V_{CC} Power Supply Current	I_{CC}	–	–	mA	5
Average V_{BB} Power Supply Current	$I_{BB1,3}$	–	400	μA	
Standby V_{BB} Power Supply Current	I_{BB2}	–	200	μA	
Standby V_{DD} Power Supply Current	I_{DD2}	–	3	mA	6
Average V_{DD} Power Supply Current During "$\overline{RAS}$ Only" Cycles	I_{DD3}	–	54	mA	4
Input Leakage Current (Any Input)	$I_{I(L)}$	–	10	μA	
Output Leakage Current	$I_{O(L)}$	–	10	μA	6, 7
Output Logic 1 Voltage @ $I_{out} = -5$ mA	V_{OH}	2.4	–	V	2
Output Logic Voltage @ $I_{out} = 4.2$ mA	V_{OL}	–	0.4	V	

AC OPERATING CONDITIONS AND CHARACTERISTICS

(See Notes 3, 9, 14)

(V_{DD} = 12 V ± 10%, V_{CC} = 5.0 V ± 10%, V_{BB} = −5.0 V ± 10%, V_{SS} = 0 V, T_A = 0 to 70°C)

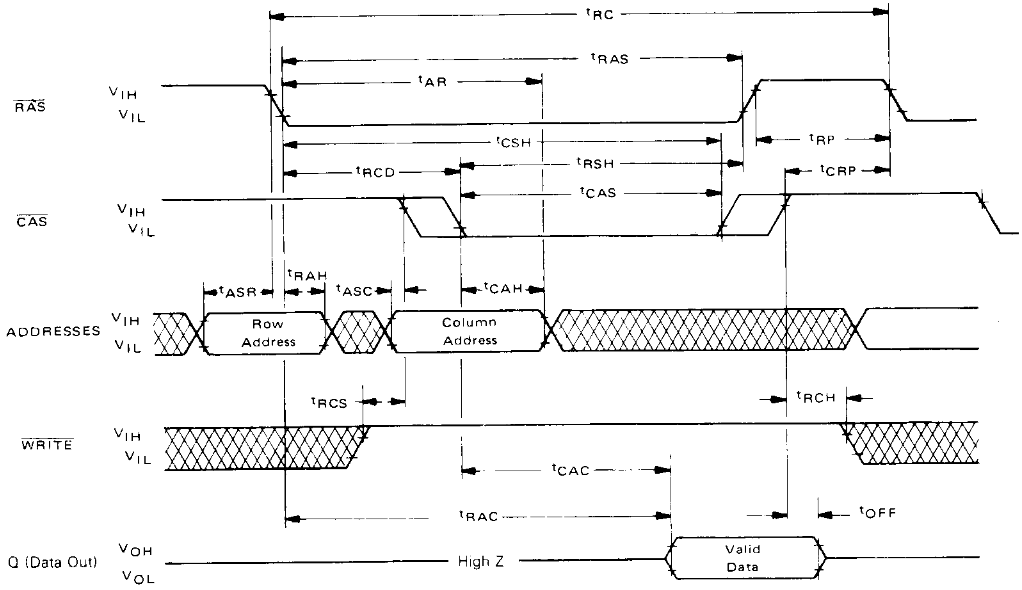
READ, WRITE, AND READ-MODIFY-WRITE CYCLES

Parameter	Symbol	MCM4132-15		MCM4132-20		MCM4132-25		MCM4132-30		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	375	–	375	–	410	–	480	–	ns	
Read Write Cycle Time	t_{RWC}	375	–	375	–	515	–	660	–	ns	
Access Time from Row Address Strobe	t_{RAC}	–	150	–	200	–	250	–	300	ns	10, 12
Access Time from Column Address Strobe	t_{CAC}	–	100	–	135	–	165	–	200	ns	11, 12
Output Buffer and Turn-off Delay	t_{OFF}	0	50	0	50	0	60	0	60	ns	
Row Address Strobe Precharge Time	t_{RP}	100	–	120	–	150	–	180	–	ns	
Row Address Strobe Pulse Width	t_{RAS}	150	10,000	200	10,000	250	10,000	300	10,000	ns	
Column Address Strobe Pulse Width	t_{CAS}	100	10,000	135	10,000	165	10,000	200	10,000	ns	
Row to Column Strobe Lead Time	t_{RCD}	20	50	25	65	35	85	60	100	ns	13
Row Address Setup Time	t_{ASR}	0	–	0	–	0	–	0	–	ns	
Row Address Hold Time	t_{RAH}	20	–	25	–	35	–	60	–	ns	
Column Address Setup Time	t_{ASC}	−10	–	−10	–	−10	–	−10	–	ns	
Column Address Hold Time	t_{CAH}	45	–	55	–	75	–	100	–	ns	
Column Address Hold Time Referenced to $\overline{\text{RAS}}$	t_{AR}	95	–	120	–	160	–	200	–	ns	
Transition Time (Rise and Fall)	t_T	3.0	35	3.0	50	3.0	50	3.0	50	ns	14
Read Command Setup Time	t_{RCS}	0	–	0	–	0	–	0	–	ns	
Read Command Hold time	t_{RCH}	0	–	0	–	0	–	0	–	ns	
Write Command Hold Time	t_{WCH}	45	–	55	–	75	–	100	–	ns	
Write Command Hold Time Referenced to $\overline{\text{RAS}}$	t_{WCR}	95	–	120	–	160	–	200	–	ns	
Write Command Pulse Width	t_{WP}	45	–	55	–	75	–	100	–	ns	
Write Command to Row Strobe Lead Time	t_{RWL}	60	–	80	–	100	–	180	–	ns	
Write Command to Column Strobe Lead Time	t_{CWL}	60	–	80	–	100	–	180	–	ns	
Data in Setup Time	t_{DS}	0	–	0	–	0	–	0	–	ns	15
Data in Hold Time	t_{DH}	45	–	55	–	75	–	100	–	ns	15
Data in Hold Time Referenced to $\overline{\text{RAS}}$	t_{DHR}	95	–	120	–	160	–	200	–	ns	
Column to Row Strobe Precharge Time	t_{CRP}	−20	–	−20	–	−20	–	−20	–	ns	
$\overline{\text{RAS}}$ Hold Time	t_{RSH}	100	–	135	–	165	–	200	–	ns	
Refresh Period	t_{RFSH}	–	2.0	–	2.0	–	2.0	–	2.0	ms	
$\overline{\text{WRITE}}$ Command Setup Time	t_{WCS}	−20	–	−20	–	−20	–	−20	–	ns	
$\overline{\text{CAS}}$ to $\overline{\text{WRITE}}$ Delay	t_{CWD}	70	–	95	–	125	–	180	–	ns	16
$\overline{\text{RAS}}$ to $\overline{\text{WRITE}}$ Delay	t_{RWD}	120	–	160	–	210	–	280	–	ns	16
$\overline{\text{CAS}}$ Precharge Time (Page Mode Cycle Only)	t_{CP}	60	–	80	–	100	–	100	–	ns	
Page Mode Cycle Time	t_{PC}	170	–	225	–	275	–	325	–	ns	
$\overline{\text{CAS}}$ Hold Time	t_{CSH}	150	–	200	–	250	–	300	–	ns	

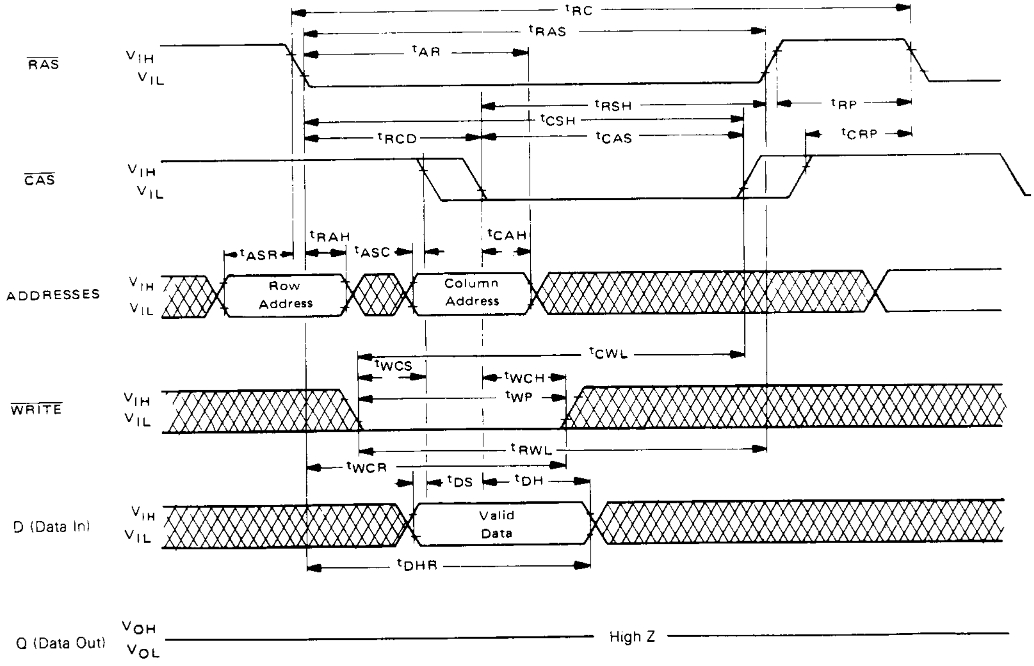
NOTES:

1. All voltages referenced to V_{SS}. V_{BB} must be applied before and removed after other supply voltages.
2. Output voltage will swing from V_{SS} to V_{CC} under open circuit conditions. For purposes of maintaining data in power-down mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations. V_{OH} (min) specification is not guaranteed in this mode.
3. Several cycles are required after power-up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate.
4. Current is proportional to cycle rate, maximum current is measured at the fastest cycle rate.
5. I_{CC} depends upon output loading. The V_{CC} supply is connected to the output buffer only.
6. Output is disabled (open-circuit) when $\overline{\text{CAS}}$ is at a logic 1.
7. $0\ V \le V_{out} \le +5.5\ V$.
8. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\Delta T/\Delta V$.
9. AC measurements assume $t_T = 5.0$ ns
10. Assumes that $t_{RCD} \le t_{RCD}$ (max).
11. Assumes that $t_{RCD} \ge t_{RCD}$ (max).
12. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
13. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (Max) limit, then access time is controlled exclusively by t_{CAC}.
14. V_{IH} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} or V_{IH} and V_{IL}.
15. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in random write cycles and to $\overline{\text{WRITE}}$ leading edge in delayed write or read-modify-write cycles.
16. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: If $t_{WCS} \ge t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \ge t_{CWD}$ (min) and $t_{RWD} \ge t_{RWD}$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
17. Two chips selected is only applicable for $\overline{\text{RAS}}$ only refresh on the 32K module.

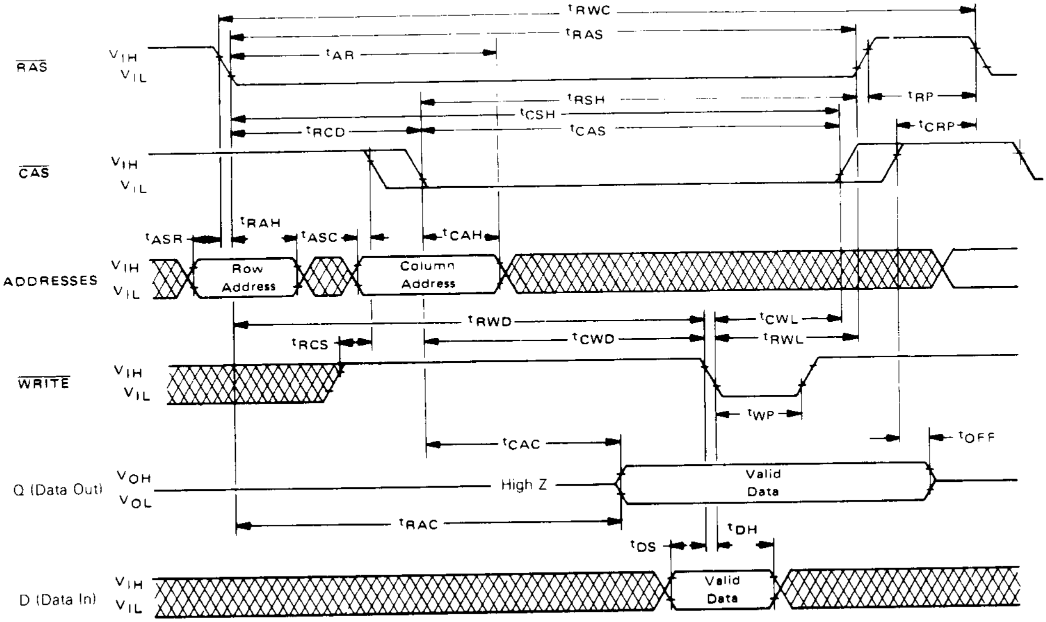
READ CYCLE TIMING



WRITE CYCLE TIMING

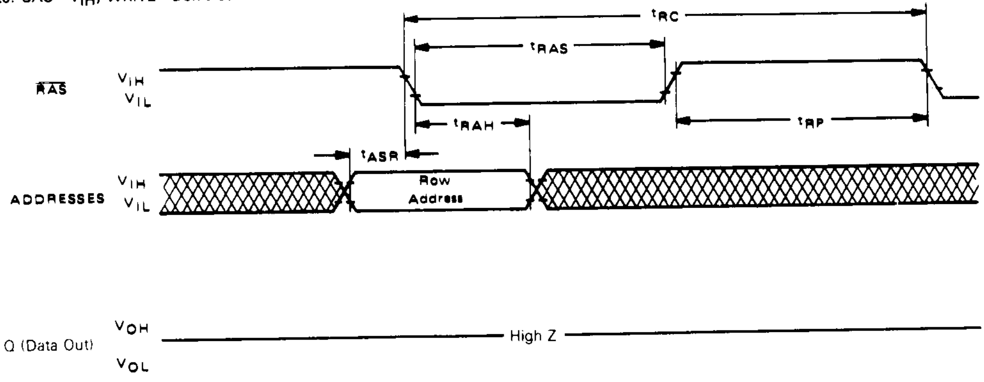


READ-WRITE/READ-MODIFY-WRITE CYCLE



RAS ONLY REFRESH TIMING

Note: $\overline{CAS} = V_{IH}$, $\overline{WRITE}$ = Don't Care



*During a read or write cycle, one 16K segment is selected. Depending on segment being addressed, $\overline{RAS_1}/\overline{CAS_1}$ or $\overline{RAS_2}/\overline{CAS_2}$ is deselected.