High Performance 4096x8 PROM TiW PROM Family

53/63S3281
53/63S3281A

Features/Benefits

- **40 ns maximum access time**
- **32768-bit memory**
- **Reliable titanium-tungsten fuses (TiW)**
- **Pin-compatible with standard Schottky PROMs**
- **PNP inputs for low input current**

Applications

- **Microprogram control stores**
- **Microprocessor program store**
- **Look-up table**
- **Character generator**
- **Code converter**
- **Programmable Logic Element (PLE™) 12 inputs, 4096 product terms, 8 outputs**

Description

The 53/63S3281 is a high-speed 4Kx8 PROM which uses *industry standard pin out.*

The family features low-current PNP inputs, full Schottky clamping and three-state outputs. The Titanium-Tungsten fuses store a logical low and are programmed to the high state.

Special on-chip circuitry and extra fuses provide preprogramming testing which assure high programming yields and high reliability.

The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military ranges.

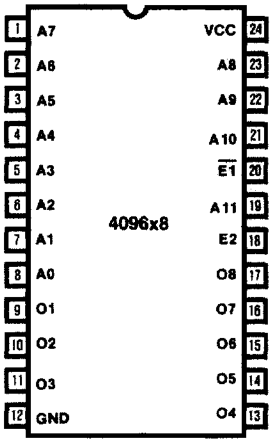
Programming

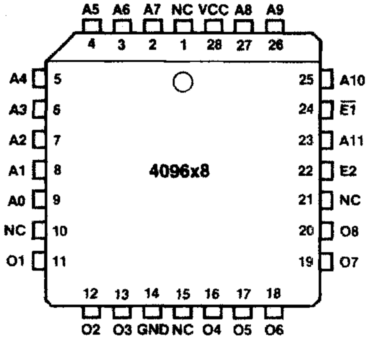
The 53/63S3281 PROM is programmed with the same programming algorithm as all other Monolithic Memories' generic TiW PROMs. For details contact the factory.

Selection Guide

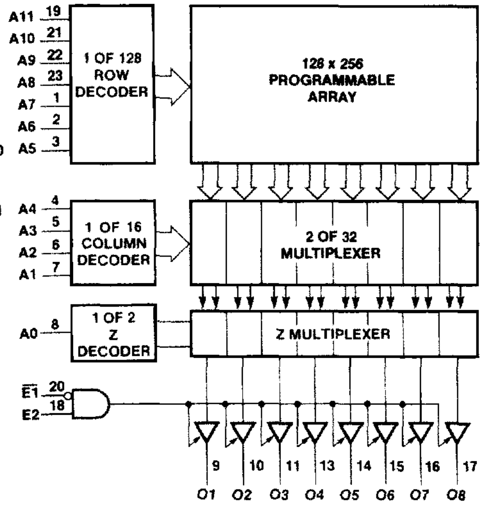
MEMORY			PACKAGE		PERFORMANCE	PART NUMBER	
SIZE	ORGANIZATION	OUTPUT	PINS	TYPE		0°C to +75°C	-55°C to +125°C
32K	4096x8	TS	24 (28)	N,J, (NL),(L), W	Standard	63S3281	53S3281
					Enhanced	63S3281A	53S3281A

Pin Configurations





Block Diagram



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Absolute Maximum Ratings

	Operating	Programming
Supply voltage V_{CC}	−0.5 V to 7 V	12 V
Input voltage	−1.5 V to 7 V	7 V
Input current	−30 mA to +5 mA	
Off-state output voltage	−0.5 V to 5.5 V	12 V
Storage temperature	−65°C to +150°C	

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY NOM	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL NOM	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	−55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION			MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18 mA				−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4 V				−0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = V_{CC} MAX				40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 16 mA	MIL			0.5	V
				COM			0.45	
V_{OH}	High-level output voltage	V_{CC} = MIN	MIL I_{OH} = −2 mA		2.4			V
			COM I_{OH} = −3.2 mA					
I_{OZL}	Off-state output current	V_{CC} = MAX	V_O = 0.4 V				−40	μA
I_{OZH}			V_O = 2.4 V				40	
I_{OS}	Output short-circuit current*	V_{CC} = 5 V	V_O = 0 V		−20		−90	mA
I_{CC}	Supply current	V_{CC} = MAX. All inputs grounded. All outputs open.				150	190	mA

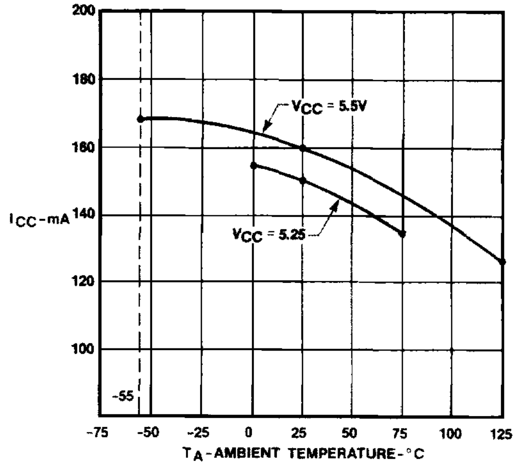
Switching Characteristics Over Operating Conditions (See standard test load)

OPERATING CONDITIONS	DEVICE TYPE	t_{AA} (ns) ADDRESS ACCESS TIME		t_{EA} AND t_{ER} (ns) ENABLE ACCESS TIME RECOVERY TIME		UNIT
		TYP†	MAX	TYP†	MAX	
COMMERCIAL	63S3281A	31	40	18	20	ns
	63S3281	31	50	18	30	
MILITARY	53S3281A	31	50	18	35	
	53S3281	31	60	18	35	

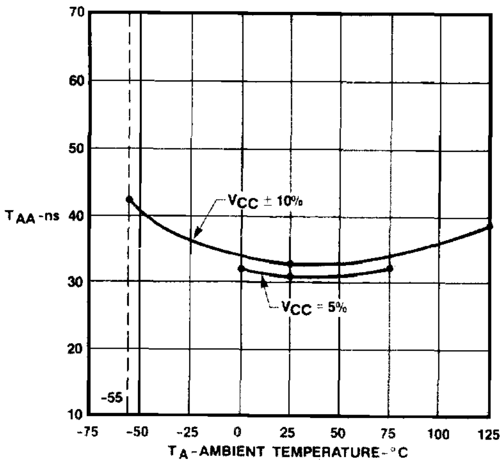
* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

† Typical at 5.0 V V_{CC} and 25°C T_A.

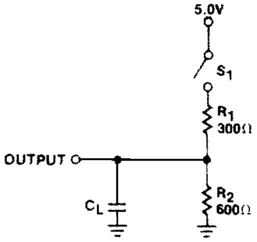
Typical I_{CC} vs Temperature



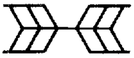
Typical T_{AA} vs Temperature



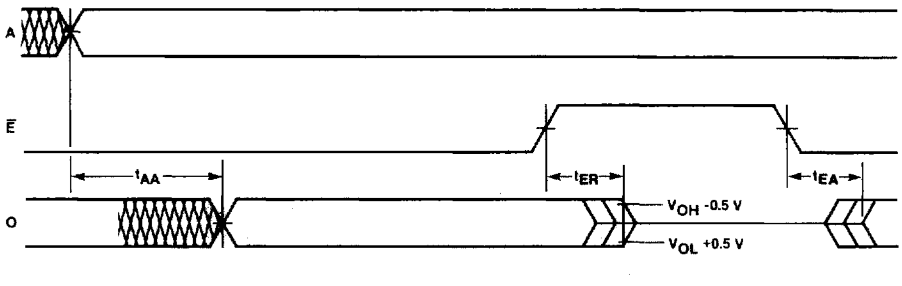
Switching Test Load



Definition of Timing Diagram

WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE; CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	NOT APPLICABLE	CENTER LINE IS HIGH IMPEDANCE STATE
	MUST BE STEADY	WILL BE STEADY

Definition of Waveforms



NOTES: 1. Input pulse amplitude 0 V to 3.0 V.

2. Input rise and fall times 2-5 ns from 0.8 V to 2.0 V.

3. Input access measured at the 1.5 V level.

4. t_{AA} is tested with switch S_1 closed. C_L = 30 pF and measured at 1.5V output level.

5. t_{EA} is measured at the 1.5 V output level with C_L = 30 pF. S_1 is open for high impedance to "1" test, and closed for high impedance to "0" test. t_{ER} is tested with C_L = 5 pF. S_1 is open for "1" to high impedance test, measured at V_{OH} - 0.5 output level: S_1 is closed for "0" to high impedance test measured at V_{OL} + 0.5V output level.

Commercial Programmers

Monolithic Memories PROMs are designed and tested to give a programming yield greater than 98%. If your programming yield is lower, check your programmer. It may not be properly calibrated.

Programming is final manufacturing — it must be quality-controlled. Equipment must be calibrated as a regular routine, ideally under the actual conditions of use. Each time a new board or a new programming module is inserted, the whole system should be checked. Both timing and voltages must meet published specifications for the device.

Remember — The best PROMs available can be made unreliable by improper programming techniques.

PROM PROGRAMMING EQUIPMENT INFORMATION

SOURCE AND LOCATION

Data I/O Corp.
10525 Willows Rd. N.E.
Redmond, WA 98073

Kontron Electronics, Inc.
630 Price Ave.
Redwood City, CA 94063

Digelec Inc.
586 Weddell Dr. Suite 1
Sunnyvale, CA 94089

Stag Microsystems Inc.
528-5 Weddell Dr.
Sunnyvale, CA 94089

Metal Mask Layout