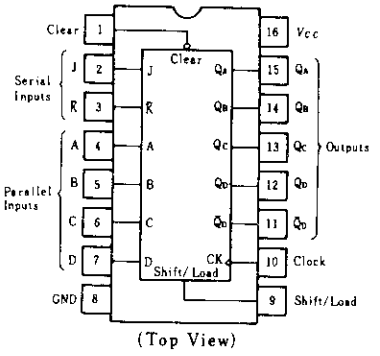
HD74HC195 ● 4-bit Parallel-Access Shift Register

This shift register features parallel inputs, parallel outputs, J-$\overline{K}$ serial inputs, Shift/Load control input, and a direct overriding clear. This shift register can operate in two modes: Parallel load; Shift from Q_A towards Q_D.

Parallel loading is accomplished by applying the four bits of data, and taking the Shift/Load control Input low. The data is loaded into the associated flip-flops and appears at the outputs after the positive transition of the clock input. During parallel loading, serial data flow is inhibited. Serial shifting occurs synchronously when the Shift/Load control input is high. Serial data for this mode is entered at the J-$\overline{K}$ inputs. These inputs allow the first stage to perform as a J-$\overline{K}$ or toggle flip-flop as shown in the function table.

■ PIN ARRANGEMENT

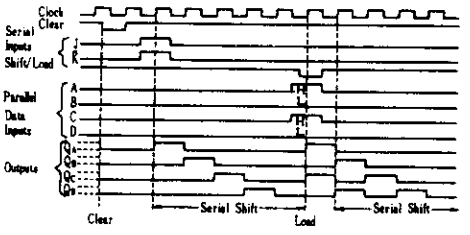


(Top View)

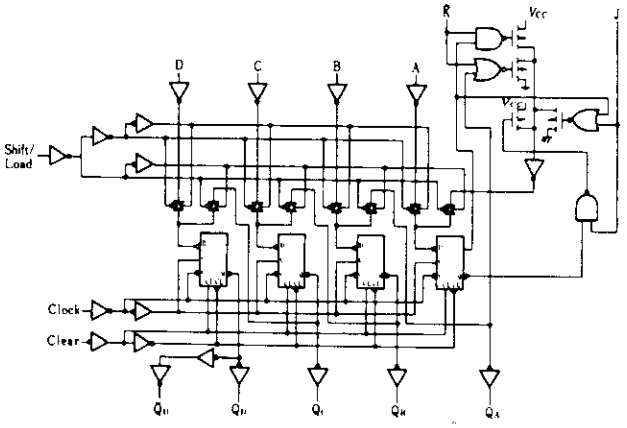
■ FEATURES

- High Speed Operation: t_{pd} (Clock to Q) = 13ns typ. (C_L = 50pF)
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: Vcc = 2 ~ 6V
- Low Input Current: 1μA max.
- Low Quiescent Supply Current: Icc (static) = 4μA max. (Ta = 25°C)

■ TIMING DIAGRAM



■ LOGIC DIAGRAM



■ FUNCTION TABLE

Clear	Shift/ Load	Clock	Inputs: Serial J	Inputs: Serial $\overline{K}$	Inputs: Parallel A	B	C	D	Outputs: Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
L	×	×	×	×	×	×	×	×	L	L	L	L	H
H	L	↑	×	×	a	b	c	d	a	b	c	d	$\overline{d}$
H	H	L	×	×	×	×	×	×	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\overline{Q}_{D0}$
H	H	↑	L	H	×	×	×	×	Q_{A0}	Q_{A0}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	L	L	×	×	×	×	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	H	×	×	×	×	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	L	×	×	×	×	Q_{An}	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$

H = high level (steady state)
L = low level (steady state)
× = don't care
↑ = transition from low to high level
a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively.

Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.

Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the most-recent ↑ transition of the clock.

■ DC CHARACTERISTICS

Item	Symbol	V_{CC}(V)	Test Conditions		$Ta=25°C$ min	$Ta=25°C$ typ	$Ta=25°C$ max	$Ta=-40\sim+85°C$ min	$Ta=-40\sim+85°C$ max	Unit
Input Voltage	V_{IH}	2.0			1.5	—	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	
		6.0			4.2	—	—	4.2	—	
	V_{IL}	2.0			—	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	
Output Voltage	V_{OH}	2.0	$V_{in}=V_{IH}$ or V_{IL}	$I_{OH}=-20\mu A$	1.9	2.0	—	1.9	—	V
		4.5			4.4	4.5	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	
		4.5		$I_{OH}=-4mA$	4.18	—	—	4.13	—	
		6.0		$I_{OH}=-5.2mA$	5.68	—	—	5.63	—	
	V_{OL}	2.0	$V_{in}=V_{IH}$ or V_{IL}	$I_{OL}=20\mu A$	—	0.0	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	
		4.5		$I_{OL}=4mA$	—	—	0.26	—	0.33	
		6.0		$I_{OL}=5.2mA$	—	—	0.26	—	0.33	
Input Current	I_{in}	6.0	$V_{in}=V_{CC}$ or GND		—	—	±0.1	—	±1.0	μA
Quiescent Supply Current	I_{CC}	6.0	$V_{in}=V_{CC}$ or GND, $I_{out}=0\mu A$		—	—	4.0	—	40	μA

■ AC CHARACTERISTICS ($C_L=50pF$, Input $t_r=t_f=6ns$)

Item	Symbol	V_{CC}(V)	Test Conditions	$Ta=25°C$ min	$Ta=25°C$ typ	$Ta=25°C$ max	$Ta=-40\sim+85°C$ min	$Ta=-40\sim+85°C$ max	Unit
Maximum Clock Frequency	f_{max}	2.0		—	—	6	—	5	MHz
		4.5		—	—	30	—	24	
		6.0		—	—	35	—	28	
Propagation Delay Time	t_{PHL}	2.0	Clock to Q	—	—	140	—	175	ns
		4.5		—	13	28	—	35	
		6.0		—	—	24	—	30	
	t_{PLH}	2.0		—	—	140	—	175	
		4.5		—	13	28	—	35	ns
		6.0		—	—	24	—	30	
	t_{PHL}	2.0	Clear to Q	—	—	150	—	190	ns
		4.5		—	15	30	—	38	
		6.0		—	—	26	—	33	
Pulse Width	t_w	2.0	Clock to Clear	80	—	—	100	—	ns
		4.5		16	7	—	20	—	
		6.0		14	—	—	17	—	
Setup Time	t_{su}	2.0	A, B, C, D, J, $\overline{K}$ to Clock	100	—	—	125	—	ns
		4.5		20	6	—	25	—	
		6.0		17	—	—	21	—	
		2.0	Shift/ Load to Clock	100	—	—	125	—	
		4.5		20	13	—	25	—	
		6.0		17	—	—	21	—	
Hold Time	t_h	2.0	Any Input except Shift / Load	0	—	—	0	—	ns
		4.5		0	−3	—	0	—	
		6.0		0	—	—	0	—	

Item	Symbol	V_{CC}(V)	Test Conditions	Ta=25°C			Ta=−40~+85°C		Unit
				min	typ	max	min	max	
Removal Time	t_{rem}	2.0	Shift / Load to Clock	75	—	—	95	—	ns
		4.5		15	8	—	19	—	
		6.0		13	—	—	16	—	
		2.0	Clear inactive to Clock	25	—	—	31	—	
		4.5		5	0	—	6	—	
		6.0		4	—	—	5	—	
Output Rise / Fall Time	t_{TLH} t_{THL}	2.0		—	—	75	—	95	ns
		4.5		—	5	15	—	19	
		6.0		—	—	13	—	16	
Input Capacitance	C_{in}	—		—	5	10	—	10	pF