HARRIS SEMICONDUCTOR

HFA3765

PRELIMINARY

AGC and Quadrature IF Demodulator

February 1998

Features

- IF Operation . . . . . 10MHz to 250MHz
- I/Q Amplitude and Phase Balance . . 0.5dB, 2 Degrees
- Voltage Gain . . . . . >60dB
- AGC Range 90dB
- Output P1dB With 20pF Load 2.5Vpp
- Low LO Drive Level . . . . . -10dBm
- Power Enable/Disable Control
- Single Supply Battery Operation . . . . . 2.7 to 3.3V

Applications

- IS-95A CDMA/AMPS Dual Mode Handsets
- Wideband CDMA Handsets
- Full Duplex Transceivers
- CDMA/TDMA Packet Protocol Radios

Description

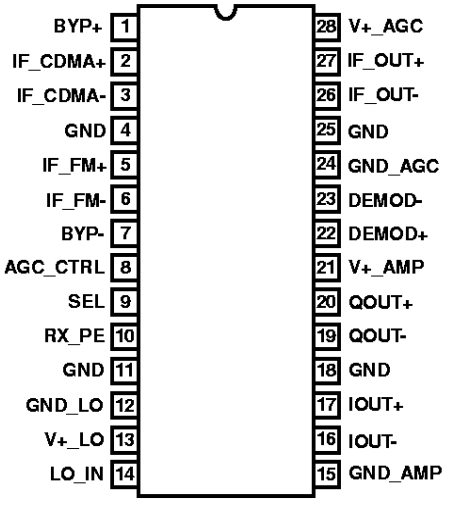
The HFA3765 is a monolithic quadrature demodulator and a gain control amplifier stage with 90dB of dynamic range for CDMA/AMPS cellular applications. Two amplifier inputs are provided for interfacing different IF input filters. A local oscillator input requires low drive levels and a divide by two phase shifter with duty cycle compensation achieves excellent phase and amplitude balance properties. The HFA3765 is one of the four chips in the PRISM™ chip set and is housed in a 28 lead SSOP package ideally suited to cellular handset applications..

Ordering Information

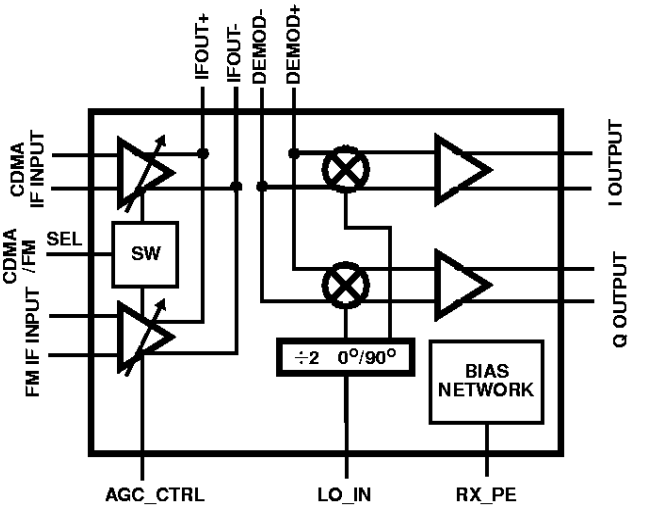
PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HFA3765IA	-40 to 85	28 Ld SSOP	M28.15
HFA3765IA96	-40 to 85	Tape and Reel	

Pinout

HFA3765
(SSOP)
TOP VIEW



Simplified Block Diagram



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CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **4300.3**

Pin Descriptions

Pin Number	NAME	DESCRIPTION
1	BYP+	DC feedback pin for the AGC amplifier. Requires good RF decoupling to a solid ground.
2	IF_CDMA+	Non-inverting analog input of the AGC amplifier, CDMA channel .Requires a DC blocking capacitor. A parallel differential DC coupled resistor setting the input impedance with its complementary input is possible.
3	IF_CDMA-	Inverting analog input of the AGC amplifier, CDMA channel. Requires a DC blocking capacitor. A parallel differential DC coupled resistor setting the input impedance with its complementary input is possible. AC couple to ground if the port is to be used single ended.
4	GND	Ground. Connect to a solid ground plane.
5	IF_FM+	Non-inverting analog input of the AGC amplifier, FM channel. Requires a DC blocking capacitor. A parallel differential DC coupled resistor setting the input impedance with its complementary input is possible.
6	IF_FM-	Inverting analog input of the AGC amplifier, FM channel. Requires a DC blocking capacitor. A parallel differential DC coupled resistor setting the input impedance with its complementary input is possible. AC couple to ground if the port is to be used single ended.
7	BYP -	DC feedback pin for the AGC amplifier. Require good RF decoupling to a solid ground.
8	AGC_CTRL	AGC current control input. Requires a 15K 1% series resistor.
9	SEL	Selects the CDMA or FM AGC Amplifier differential input. HIGH selects the CDMA input; LOW selects the FM input.
10	RX_PE	Power enable control input. HIGH for normal operation. LOW for power down.
11	GND	Ground. Connect to a solid ground plane.
12	GND_LO	LO_IN input ground return. Ground to Local Oscillator ground plane or transmission line.
13	V+_LO	LO divider network Power Supply. Use high quality RF decoupling capacitors at the pin.
14	LO_IN	Current input from the Local Oscillator. Use a 50Ω power to current converter. See applications diagram. Requires a DC blocking capacitor.
15	GND_AMP	IF output amplifiers ground return.
16	IOUT-	Negative I channel baseband output. Requires a DC blocking capacitor.
17	IOUT+	Positive I channel baseband output. Requires a DC blocking capacitor.
18	GND	Ground. Connect to a solid ground plane.
19	QOUT-	Negative Q channel baseband output. Requires a DC blocking capacitor.
20	QOUT+	Positive Q channel baseband output. Requires a DC blocking capacitor.
21	V+_AMP	IF output amplifier Power Supply.Use high quality RF decoupling capacitors at the pin.
22	DEMOD+	Positive input of the quadrature demodulator. Requires a DC blocking capacitor.
23	DEMOD -	Negative input of the quadrature demodulator. Requires a DC blocking capacitor.
24	GND_AGC	AGC amplifier main ground return.
25	GND	Ground. Connect to a solid ground plane.
26	IF_OUT-	Negative output from the AGC amplifier. Requires a DC blocking capacitor.
27	IF_OUT+	Positive output from the AGC amplifier. Requires a DC blocking capacitor.
28	V+_AGC	AGC amplifier Power Supply.Use high quality RF decoupling capacitors at the pin.

Absolute Maximum Ratings

Supply Voltage . . . . . -0.3V to +3.6V
Voltage on Any Other Pin . . . . . -0.3V to V_{CC} +0.3V

Operating Conditions

Supply Voltage Range . . . . . 2.7 to 3.3V
Operating Temperature Range . . . . . $-40^oC \le T_A \le 85^oC$

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} ($^oC/W$)
SSOP Package 88
Maximum Junction Temperature (Plastic Package) . . 150^oC
Maximum Storage Temperature Range . . . . . $-65^oC \le T_A \le 150^oC$
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	TEST CONDITONS	(Note 2) TEST LEVEL	TEMP (^oC)	MIN	TYP	MAX	UNITS
OVERALL CASCADED SPECIFICATIONS , VCC = 2.7V, IF_IN = Differential - 60dBm or higher @ 85MHz							
IF Frequency Range		B	Full	10	85	250	MHz
Baseband Frequency Range		B	Full	0	-	1	MHz
LO Frequency Range		B	Full	20	170	500	MHz
AGC Gain Control Voltage Range		A	Full	0.5	-	2.4	V
AGC Gain Control Sensitivity		A	25	-	60	-	dB/V
AGC Gain Control Slope Change		A	25	-	1.2:1	3:1	-
Insertion Phase vs AGC		B	25	-	0.1	-	deg/dB
Gain Switching Speed, Full Scale	To ±1dB Settling	B	25	-	TBD	10	µs
Amplitude Balance (Note 3)		A	Full	-0.5	0	0.5	dB
Phase Balance (Note 3)		A	Full	-2	0	+2	Degrees
Power Gain	500Ω in, 5000Ω Differential load. AGC_CTRL set for 48 +/- 0.2dB of power-gain (CDMA and FM mode)	A	Full	-	48	-	dB
Voltage Gain		A	Full	-	58	-	dB
Noise Figure (CDMA , SEL = HIGH)		B	Full	-	6.6	7.5	dB
Noise Figure (FM , SEL = LOW)		B	Full	-	6.9	8.0	dB
IP3, Output		A	Full	0.5	4.8	-	dBm
P1dB Output		A	Full	-10	-5	-	dBm
Voltage Gain	500Ω in, 5000Ω load AGC_CTRL set for 38 +/- 0.2dB of power-gain (CDMA and FM mode)	B	Full	-	48	-	dB
Noise Figure		B	Full	-	8.4	-	dB
IP3, Output		B	Full	-	4.4	-	dBm
P1dB Output		B	Full	-	-6	-	dBm

Electrical Specifications

PARAMETER	TEST CONDITONS	(Note 2) TEST LEVEL	TEMP (^{o}C)	MIN	TYP	MAX	UNITS
Voltage Gain	500Ω in, 5000Ω load AGC_CTRL set for 28 +/- 0.2dB of power-gain (CDMA and FM mode)	B	Full	-	38	-	dB
Noise Figure		B	Full	-	11	-	dB
IP3, Output		B	Full	-	3.2	_	dBm
P1dB Output		B	Full	-	-8	-	dBm
Voltage Gain	500Ω in, 5000Ω load AGC_CTRL set for 18 +/- 0.2dB of power-gain (CDMA and FM mode)	B	Full	-	28	-	dB
Noise Figure		B	Full	-	14	-	dB
IP3, Output		B	Full	-	-1.0	_	dBm
P1dB Output		B	Full	-	-11	-	dBm
Voltage Gain	500Ω in, 5000Ω load AGC_CTRL set for 8 +/- 0.2dB of power-gain (CDMA and FM mode)	B	Full	-	18	-	dB
Noise Figure		B	Full	-	20	-	dB
IP3, Output		B	Full	-	-7.2	_	dBm
P1dB Output		B	Full	-	-17	-	dBm
Voltage Gain	500Ω in, 5000Ω load AGC_CTRL set for -2 +/- 0.2dB of power-gain (CDMA and FM mode)	B	Full	-	8	-	dB
Noise Figure		B	Full	-	28	-	dB
IP3, Output		B	Full	-	-15.2	_	dBm
P1dB Output		B	Full	-	-25	-	dBm
Voltage Gain	500Ω in, 5000Ω load AGC_CTRL set for -12 +/- 0.2dB of power-gain (CDMA and FM mode)	A	Full	-	-2	-	dB
Noise Figure		B	Full	-	37	-	dB
IP3, Output		A	Full	-26	-24.2	_	dBm
P1dB Output		A	Full	-36	-33	-	dBm
Voltage Gain	500Ω in, 5000Ω load AGC_CTRL set for -25 +/- 0.2dB of power-gain (CDMA and FM mode)	A	Full	-	-15	-	dB
Noise Figure		B	Full		48	-	dB
IP3, Output		A	Full	-38	-35.2	_	dBm
P1dBOutput		A	Full	-48	-46	-	dBm
LO Current Input Impedance	Single end	C	25	-	130	-	Ω
LO Drive Level	Applications diagram	A	25	-	-10	-	dBm
LO Drive Optimal Current Range		B	25	50	200	300	µA
Baseband Differential Load resistance		B	Full	-	5000	-	Ω
Baseband Single ended Load Capac.		B	Full	-	-	20	pF
Baseband Differential Load Capacitance		B	Full	-	-	10	pF
Single end Input Impedance CDMA or FM	Measured single end	B	25	-	1500	-	Ω
Differential Input Impedance CDMA or FM	Measured differential	B	25	-	3300	-	Ω
AGC Gain Control Input Impedance	Set externally	C	25	15K	-	-	Ω
AGC Amp Output Differential Impedance		C	25	-	80	-	Ω

Electrical Specifications

PARAMETER	TEST CONDITONS	(Note 2) TEST LEVEL	TEMP (^{o}C)	MIN	TYP	MAX	UNITS
POWER SUPPLY AND LOGIC SPECIFICATIONS							
Supply Voltage Range		A	Full	2.7	-	3.3	V
Total Supply Current	VCC = 3.3V	A	Full	-	28	-	mA
Power Down Supply Current	VCC = 3.3V	A	Full	-	1	100	µA
Power Up/Down Speed		B	25	-	-	10	µs
RX_PE and SEL V_{IL}		A	Full	-	-	0.2*VCC	V
RX_PE and SEL V_{IH}		A	Full	2.0	-	-	V
RXPE and SEL Input Bias Current	VIH = 2.0V,VCC=3.3V	A	Full	-50	-	+50	µA
	VIL= 0.66V,VCC=2.7V	A	Full	-50	-	+50	µA

NOTE:

2. A = Production Tested, B = Based on Characterization, C = By Design

3. A positive frequency offset from the carrier produces the I channel leading the Q channel by 90 degrees.

Typical Applications Diagram