DRAM

16 MEG x 1 DRAM

FAST PAGE MODE: MT4C10016
STATIC COLUMN: MT4C10017

FEATURES

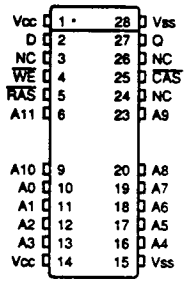
- Industry standard x1 pinout, timing, functions and packages
- High performance, CMOS silicon gate process
- Single power supply: +5V±10% or +3.3V±10%
- Low power, 3mW standby; 250mW active, typical
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{CBR}$), and HIDDEN
- 4096-cycle refresh distributed across 64ms

OPTIONS / MARKING

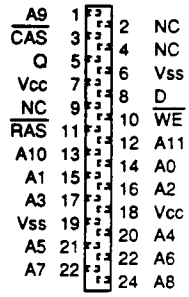
• Timing	
50ns access	-5
60ns access	-6
70ns access	-7
80ns access	-8
• Packages	
Plastic ZIP (475mil)	Z
Plastic SOJ (400mil)	DJ
Plastic TSOP (*)	TG
• Refresh Period	
4096 cycles @ 64ms	None
• Operating Temperature, T_A	
Commercial (0°C to +70°C)	None
Industrial (-40°C to +85°C)	IT
• Power Supply	
+5V±10%	None
+3.3V±10%	V

PIN ASSIGNMENT (Top View)

24-Pin SOJ (E-7)



24-Pin ZIP



*Consult factory on availablity of TSOP packages

GENERAL DESCRIPTION

The MT4C10016/7 are randomly accessed solid-state memories containing 16,777,216 bits organized in a x1 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 24 address bits, which are entered 12 bits (A0-A11) at a time. $\overline{RAS}$ is used to latch the first 12 bits and $\overline{CAS}$ the latter 12 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin remains open (High-Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after data reaches the output pin, data out (Q) is activated and retains the selected cell data as long as $\overline{CAS}$ remains LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A11) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{CBR}$), or HIDDEN REFRESH) so that all 2048/4096 combinations of $\overline{RAS}$ addresses (A0-A10/A11) are executed at least every 32ms/64ms, regardless of sequence. The CBR refresh cycle will invoke the refresh counter for automatic $\overline{RAS}$ addressing.

The MT4C10016/7 are available with either 2048 cycles or 4096 cycles of refreshing. If CBR refresh is used, the 2048-cycle version will work in either a 2048 or a 4096 cycle application.

ORDER INFORMATION

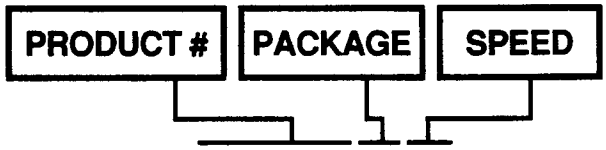
Each Micron component family is manufactured and quality-controlled in the USA at our modern Boise, Idaho, facility employing Micron's low power, high performance CMOS silicon gate process. Micron products are functionally equivalent to other manufacturers' products meeting JEDEC standards. Device functionality is consistently assured over a wider power supply, temperature range and refresh range than specified. Each unit receives continuous AMBYX™ system-level testing during many hours of accelerated burn-in prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you. Micron's quality assured policy is to offer prompt, accurate and courteous service while assuring reliability and quality.

ORDER EXAMPLES:

DRAM

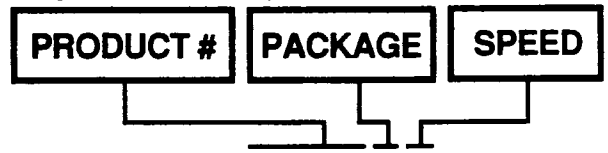
1 Meg x 1, 100ns in Plastic SOJ



MT4C1024DJ -10

DRAM MODULE

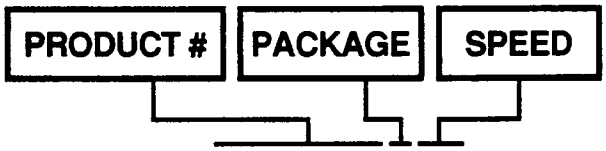
1 Meg x 8, 120ns Fast Page Mode Access, Leaded SIP



MT8D18M -8

MULTIPORT DRAM (VRAM)

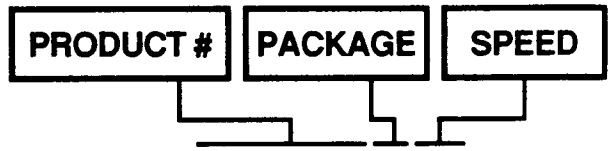
256K x 4, 100ns in ZIP



MT42C4256Z -10

CACHE DATA SRAM

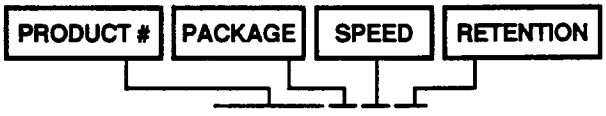
Dual 4K x 16, Single 8K x 16, 25ns in Plastic LCC



MT56C0816EJ -25

SRAM

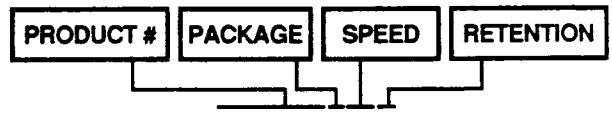
32K x 8, 45ns in Plastic SOJ



MT5C2568DJ-45

SRAM MODULE

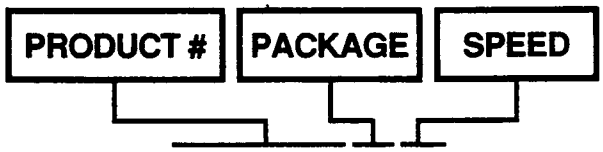
64K x 16, 25ns in DIP Module with 2V Data Retention



MT4S6416D-25L

Synchronous SRAM

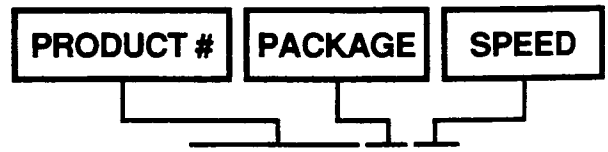
16K x 16, Clocked, Register Inputs,17ns in Plastic LCC



MT58C1616 EJ -17

FIFO

512 x 9, 15ns in 300mil DIP



MT52C9005 -15

NOTE: Call Micron for to-scale package drawings showing specific dimensions.

2805 East Columbia Road Boise, Idaho 83706 (208) 368-3900 FAX(208) 368-4431