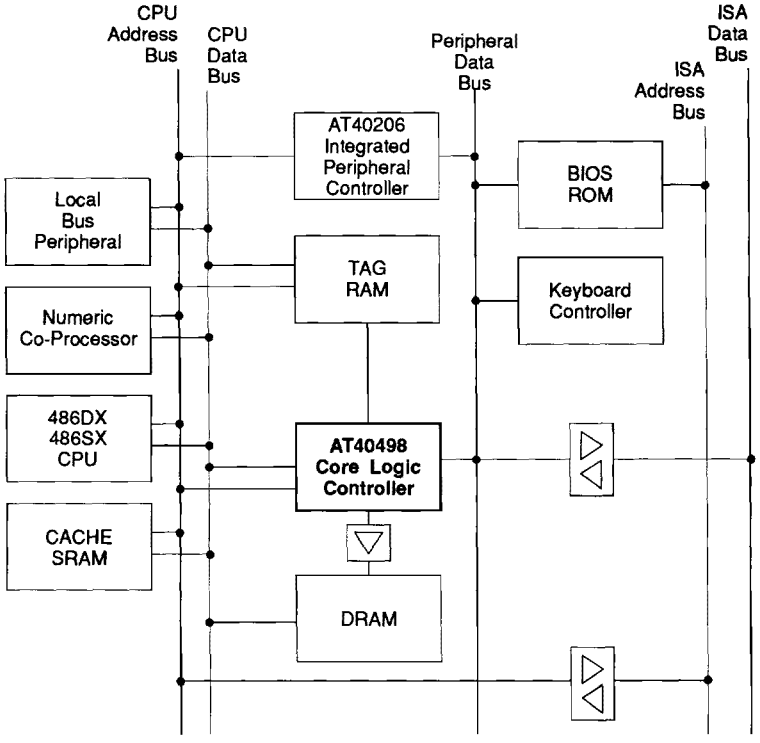
Features

- One-Chip PC/AT Compatible Core Logic Controller for 80486 Systems Operating Up to 66 MHz.
- One 208-Pin Quad Flatpack, Sub-Micron CMOS Technology
- Direct Mapped Write-Back Cache Controller with Burst Fill
- Programmable 2-1-1-1, 3-1-1-1, 2-2-2-2 and 3-2-2-2 Cache Burst Cycles
- Local Bus Peripheral Support
- Port B Register and NMI Logic
- Programmable ISA Bus Clock Generator
- Back-to-Back 16-Bit ISA Bus Cycles
- 256K, 1-Mbit and 4-Mbit DRAM Support
- Up to 64 Mbytes of Platform Memory
- Shadow RAM Support
- OS/2 Alternate Hot Reset Support

80486 Core Logic Controller

Block Diagram



Description

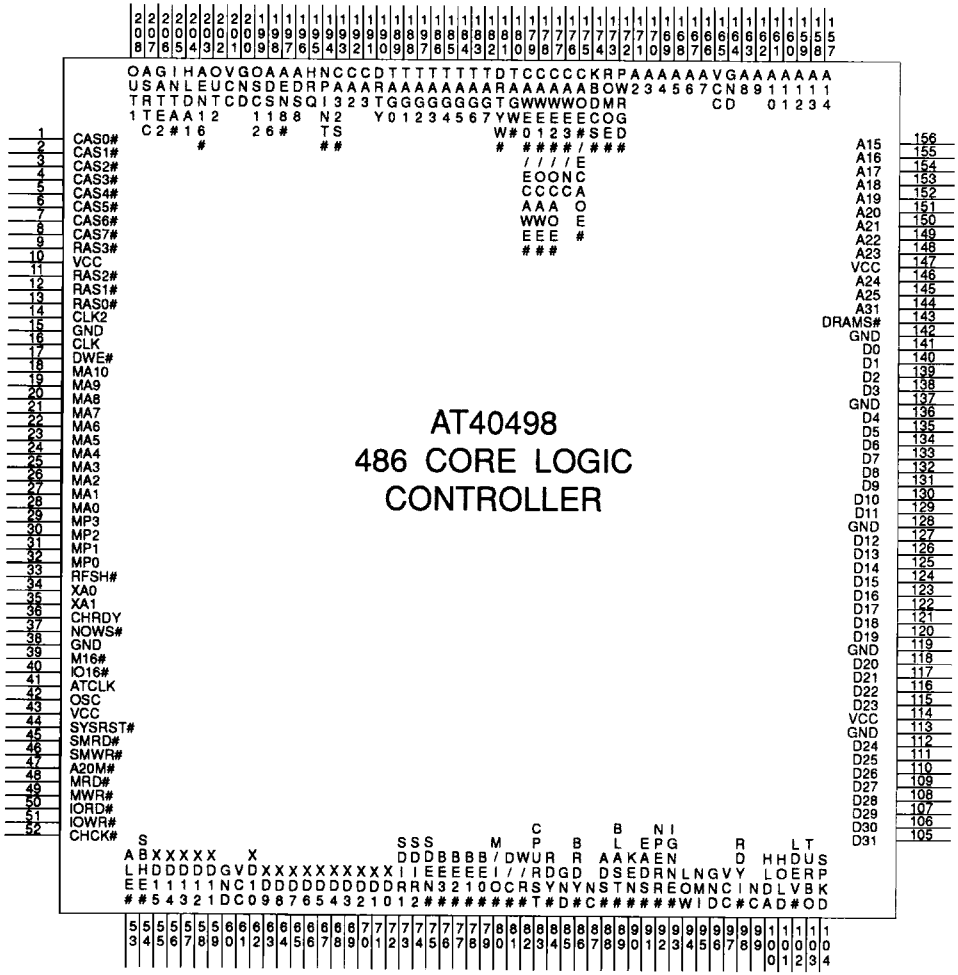
The Atmel AT40498 is a highly integrated single-chip core logic controller for 80486 PC/AT systems operating up to 66 MHz. The chip integrates system control, memory control, secondary cache control, bus arbitration functions, and data buffering and translation. In addition, the AT40498 supports local bus peripherals.

The memory controller addresses up to 64 Mbytes of main memory. The memory can consist of 256K, 1-Mbit, and 4-Mbit DRAMS. Refresh can be conventional or hidden, fast or slow.

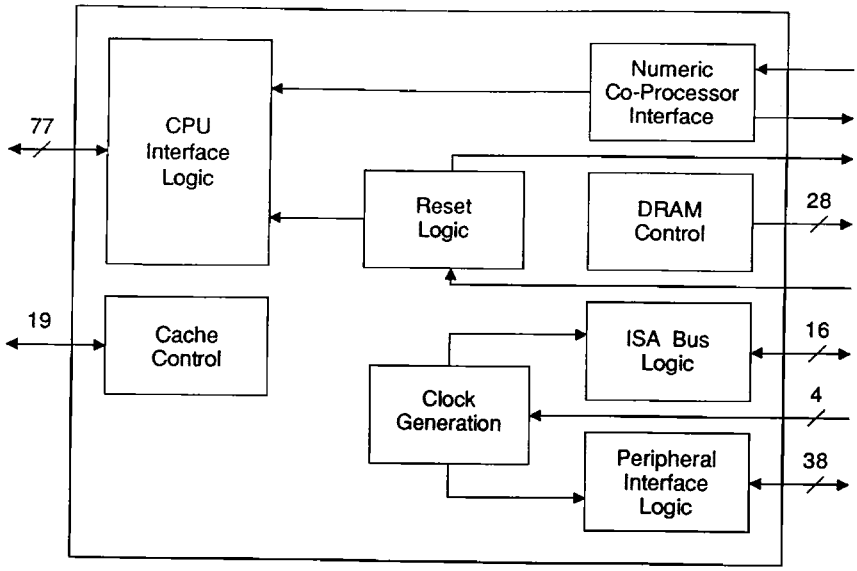
The secondary write-back cache controller supports one-bank or two-bank operation with interleaving to maximize performance. Cache sizes can range from 32 Kbytes to 512 Kbytes. Cache read and write burst cycles are programmable.

Together with a standard peripheral controller such as the AT40206 IPC and a minimum number of other components, the AT40498 implements a powerful, low-cost PC/AT compatible computer.

Pin Configuration



Core Logic Controller Block Diagram



Ordering Information

CPU Clock (MHz)	Power Supply	Ordering Code	Package	Operation Range
25	5 V ± 5%	AT40498-25	208Q	Commercial (0°C to 70°C)
33	5 V ± 5%	AT40498-33	208Q	Commercial (0°C to 70°C)
50	5 V ± 5%	AT40498-50	208Q	Commercial (0°C to 70°C)

Package Type	
208Q	208 Lead, Plastic Gull Wing Quad Flat Package (PQFP)