SYNCHRONOUS DRAM MODULE

MT8LSDT864A, MT16LSDT1664A

For the latest data sheet, please refer to the Micron Web site: www.micron.com/mti/msp/html/datasheet.html

FEATURES

- PC66-, PC100- and PC133-compliant
- JEDEC-standard 168-pin, dual in-line memory module (DIMM)
- Utilizes 100 MHz, 125 MHz and 133 MHz SDRAM components
- Unbuffered
- 64MB (8 Meg x 64) and 128MB (16 Meg x 64)
- Single +3.3V ±0.3V power supply
- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal SDRAM banks for hiding row access/precharge
- Programmable burst lengths: 1, 2, 4, 8 or full page
- Auto Precharge, includes CONCURRENT AUTO PRECHARGE, and Auto Refresh Modes
- Self Refresh Mode
- 64ms, 4,096-cycle refresh
- LVTTL-compatible inputs and outputs
- Serial Presence-Detect (SPD)

OPTIONS — MARKING

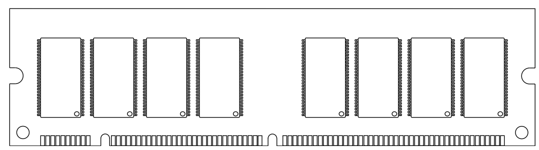
OPTIONS	MARKING
• Operating Temperature Range	
Commercial (-0°C to +70°C)	G
Extended (-40°C to +85°C)	I
• Frequency/CAS Latency	
133 MHz/CL = 2 (7.5, 133MHz SDRAMs)	-13E
133 MHz/CL = 3 (7.5ns, 133 MHz SDRAMs)	-133
100 MHz/CL = 2 (8ns, 125 MHz SDRAMs)	-10E
66 MHz/CL = 2 (10ns, 100 MHz SDRAMs)	-662

KEY SDRAM COMPONENT TIMING PARAMETERS

MODULE MARKING	SPEED GRADE	CAS LATENCY	ACCESS TIME	SETUP TIME	HOLD TIME
-13E	-7E	2	5.4ns	1.5ns	0.8ns
-133	-75	3	5.4ns	1.5ns	0.8ns
-10E	-8E	2	6ns	2ns	1ns
-662	-10	2	9ns	3ns	1ns

PIN ASSIGNMENT (Front View)
168-Pin DIMM

64MB, 66 MHz; 64MB, 100 MHz; 128MB



PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	VSS	43	VSS	85	VSS	127	VSS
2	DQ0	44	DNU	86	DQ32	128	CKE0
3	DQ1	45	S2#	87	DQ33	129	S3#*
4	DQ2	46	DQMB2	88	DQ34	130	DQMB6
5	DQ3	47	DQMB3	89	DQ35	131	DQMB7
6	VDD	48	DNU	90	VDD	132	RFU
7	DQ4	49	VDD	91	DQ36	133	VDD
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	NC	94	DQ39	136	NC
11	DQ8	53	NC	95	DQ40	137	NC
12	VSS	54	VSS	96	VSS	138	VSS
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	VDD	101	DQ45	143	VDD
18	VDD	60	DQ20	102	VDD	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	NC	104	DQ47	146	NC
21	NC	63	CKE1*	105	NC	147	NC
22	NC	64	VSS	106	NC	148	VSS
23	VSS	65	DQ21	107	VSS	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	VDD	68	VSS	110	VDD	152	VSS
27	WE#	69	DQ24	111	CAS#	153	DQ56
28	DQMB0	70	DQ25	112	DQMB4	154	DQ57
29	DQMB1	71	DQ26	113	DQMB5	155	DQ58
30	S0#	72	DQ27	114	S1#*	156	DQ59
31	DNU	73	VDD	115	RAS#	157	VDD
32	VSS	74	DQ28	116	VSS	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	VSS	120	A7	162	VSS
37	A8	79	CK2	121	A9	163	CK3
38	A10	80	NC	122	BA0	164	NC
39	BA1	81	NC/WP**	123	A11	165	SA0
40	VDD	82	SDA	124	VDD	166	SA1
41	VDD	83	SCL	125	CK1	167	SA2
42	CK0	84	VDD	126	RFU	168	VDD

*128MB version only　　**-133/-10E versions only

PART NUMBERS

PART NUMBER	CONFIG	BUS SPEED	TEMP
MT8LSDT864AG-13E_	8 Meg x 64	133 MHz	0° to +70°
MT8LSDT864AG-133_	8 Meg x 64	133 MHz	0° to +70°
MT8LSDT864AG-10E_	8 Meg x 64	100 MHz	0° to +70°
MT8LSDT864AG-662_	8 Meg x 64	66 MHz	0° to +70°
MT16LSDT1664AG-13E_	16 Meg x 64	133MHz	0° to +70°
MT16LSDT1664AG-133_	16 Meg x 64	133 MHz	0° to +70°
MT16LSDT1664AG-10E_	16 Meg x 64	100 MHz	0° to +70°
MT16LSDT1664AG-662_	16 Meg x 64	66 MHz	0° to +70°
MT8LSDT864AI-133_	8 Meg x 64	133 MHz	-40° to +85°
MT8LSDT864AI-10E_	8 Meg x 64	100 MHz	-40° to +85°
MT8LSDT864AI-662_	8 Meg x 64	66 MHz	-40° to +85°
MT16LSDT1664AI-133_	16 Meg x 64	133 MHz	-40° to +85°
MT16LSDT1664AI-10E_	16 Meg x 64	100 MHz	-40° to +85°
MT16LSDT1664AI-662_	16 Meg x 64	66 MHz	-40° to +85°

NOTE: All part numbers end with a two-place code (not shown), designating component and PCB revisions. Consult factory for current revision codes. Example: MT8LSDT864AG-10EB4.

GENERAL DESCRIPTION

The MT8LSDT864A and MT16LSDT1664A are high-speed CMOS, dynamic random-access, 64MB and 128MB memories organized in a x64 configuration. These modules use internally configured quad-bank SDRAMs with a synchronous interface (all signals are registered on the positive edge of the clock signals CK0-CK3).

Read and write accesses to the SDRAM modules are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the bank, A0-A11 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

These modules provide for programmable READ or WRITE burst lengths of 1, 2, 4 or 8 locations, or the full page, with a burst terminate option. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence.

These modules use an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the 2*n* rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one bank while accessing one of the other three banks will hide the precharge cycles and provide seamless, high-speed, random-access operation.

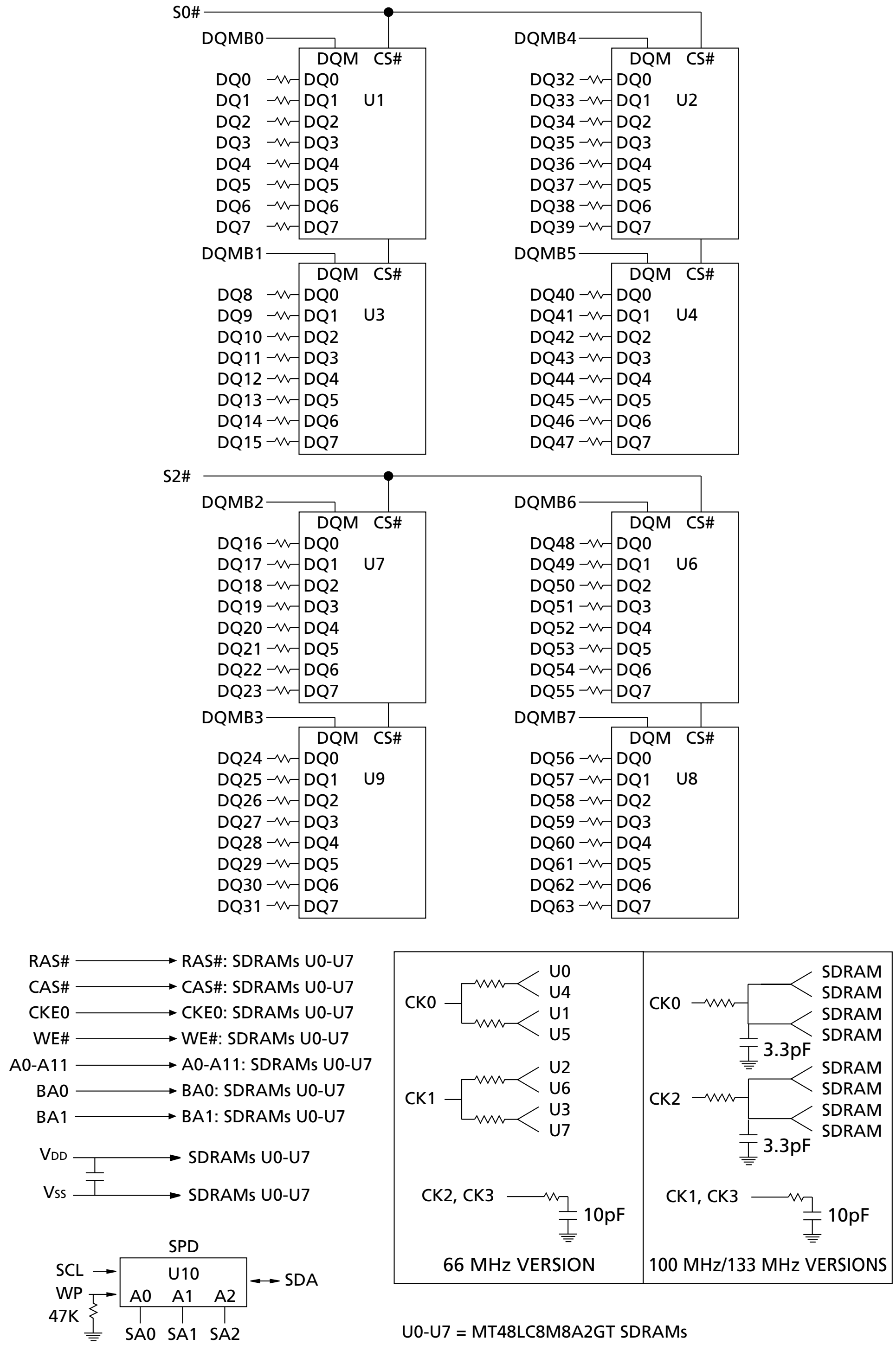
These modules are designed to operate in 3.3V, low-power memory systems. An auto refresh mode is provided, along with a power-saving, power-down mode. All inputs and outputs are LVTTL-compatible.

SDRAM modules offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks in order to hide precharge time and the capability to randomly change column addresses on each clock cycle during a burst access. For more information regarding SDRAM operation, refer to the 64Mb x4, x8, x16 SDRAM data sheet.

SERIAL PRESENCE-DETECT OPERATION

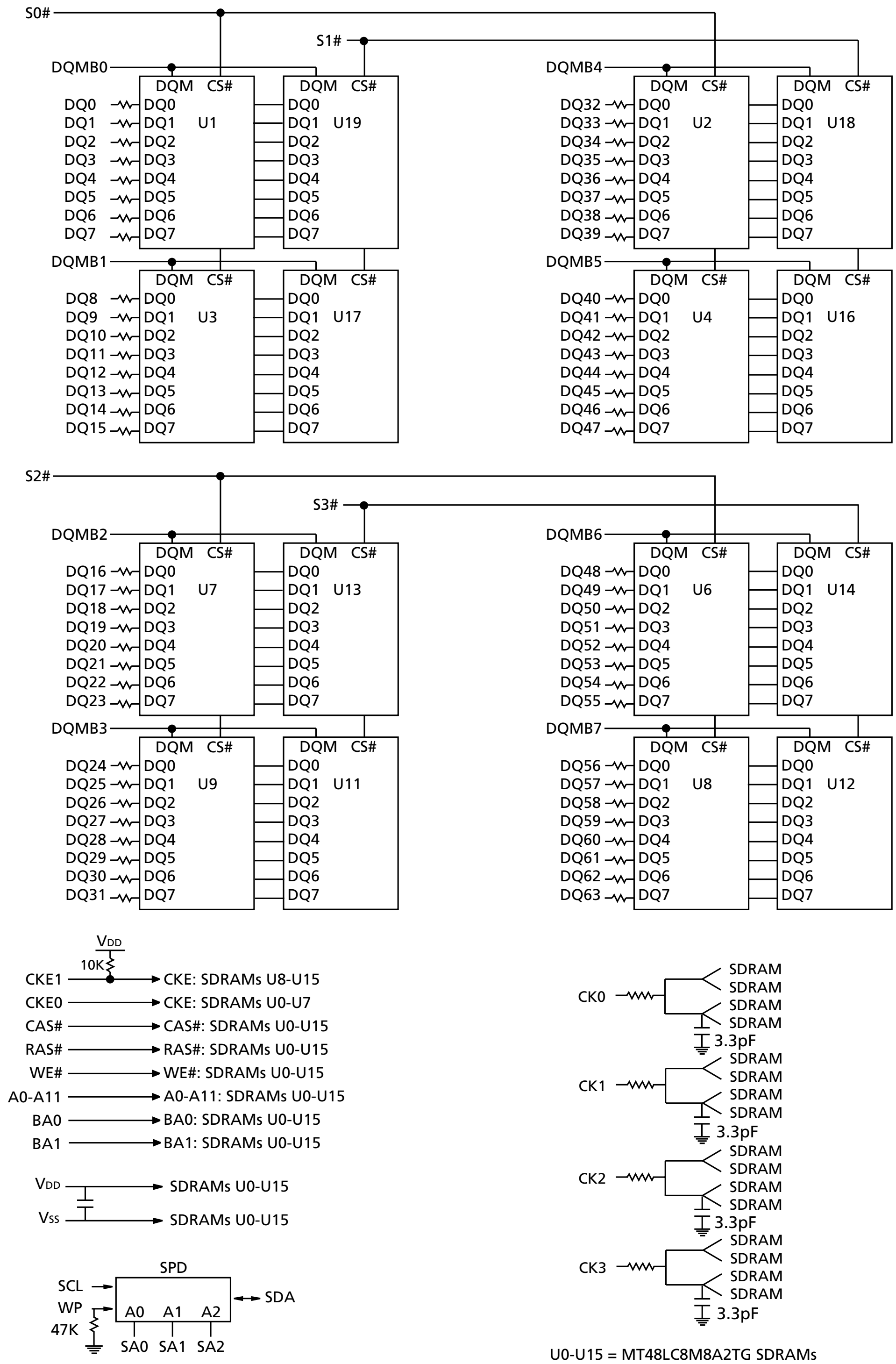
These modules incorporate serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes can be programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard IIC bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA(2:0), which provide eight unique DIMM/EEPROM addresses.

FUNCTIONAL BLOCK DIAGRAM
MT8LSDT864A (64MB)



NOTE: All resistor values are 10 ohms.

FUNCTIONAL BLOCK DIAGRAM
MT16LSDT1664A (128MB)



NOTE: All resistor values are 10 ohms unless otherwise specified.

PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
115, 111, 27	RAS#, CAS#, WE#	Input	Command Inputs: RAS#, CAS# and WE# (along with S0#-S3#) define the command being entered.
42, 79, 125, 163	CK0-CK3	Input	Clock: CK0-CK3 are driven by the system clock. All SDRAM input signals are sampled on the positive edge of CK. CK also increments the internal burst counter and controls the output registers.
63, 128	CKE1, CKE0	Input	Clock Enable: CKE0-CKE1 activate (HIGH) and deactivate (LOW) the CK0-CK3 signals. Deactivating the clock provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), ACTIVE POWER-DOWN (row ACTIVE in any bank) or CLOCK SUSPEND operation (burst access in progress). CKE0-CKE1 are synchronous except after the device enters power-down and self refresh modes, where CKE0-CKE1 become asynchronous until after exiting the same mode. The input buffers, including CK0-CK3, are disabled during power-down and self refresh modes, providing low standby power.
30, 45, 114, 129	S0#-S3#	Input	Chip Select: S0#-S3# enable (registered LOW) and disable (registered HIGH) the command decoder. All commands are masked when S0#-S3# are registered HIGH. S0#-S3# are considered part of the command code.
28-29, 46-47, 112-113, 130-131	DQMB0-DQMB7	Input	Input/Output Mask: DQMB is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked when DQMB is sampled HIGH during a WRITE cycle. The output buffers are placed in a High-Z state (two-clock latency) when DQMB is sampled HIGH during a READ cycle.
39, 122	BA0, BA1	Input	Bank Address: BA0 and BA1 define to which bank the ACTIVE, READ, WRITE or PRECHARGE command is being applied.
33-38, 117-121, 123	A0-A11	Input	Address Inputs: A0-A11 are sampled during the ACTIVE command (row-address A0-A11) and READ/WRITE command (column-address A0-A8, with A10 defining AUTO PRECHARGE) to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine if all banks are to be precharged (A10 HIGH) or bank selected by BA0, BA1 (LOW). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
81	WP	Input	Write Protect: Serial presence-detect hardware write protect. Applies to -10E/-10C versions only.
83	SCL	Input	Serial Clock for Presence-Detect: SCL is used to synchronize the presence-detect data transfer to and from the module.
165-167	SA0-SA2	Input	Presence-Detect Address Inputs: These pins are used to configure the presence-detect device.

PIN DESCRIPTIONS (continued)

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
2-5, 7-11, 13-17, 19-20, 55-58, 60, 65-67, 69-72, 74-77, 86-89, 91-95, 97-101, 103-104, 139-142, 144, 149-151, 153-156, 158-161	DQ0-DQ63	Input/ Output	Data I/Os: Data bus.
82	SDA	Input/ Output	Serial Presence-Detect Data: SDA is a bidirectional pin used to transfer addresses and data into and data out of the presence-detect portion of the module.
6, 18, 26, 40, 41, 49, 59, 73, 84, 90, 102, 110, 124, 133, 143, 157, 168	V_{DD}	Supply	Power Supply: +3.3V ±0.3V.
1, 12, 23, 32, 43, 54, 64, 68, 78, 85, 96, 107, 116, 127, 138, 148, 152, 162	V_{SS}	Supply	Ground.
126, 132	RFU	–	Reserved for Future Use: These pins should be left unconnected.
31, 44, 48	DNU	–	Do Not Use: These pins are not connected on these modules but are assigned pins on the compatible DRAM version.

SPD CLOCK AND DATA CONVENTIONS

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions (Figures 1 and 2).

SPD START CONDITION

All commands are preceded by the start condition, which is a HIGH-to-LOW transition of SDA when SCL is HIGH. The SPD device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

SPD STOP CONDITION

All communications are terminated by a stop condition, which is a LOW-to-HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the SPD device into standby power mode.

SPD ACKNOWLEDGE

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data (Figure 3).

The SPD device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a WRITE operation have been selected, the SPD device will respond with an acknowledge after the receipt of each subsequent eight bit word. In the read mode the SPD device will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to standby power mode.

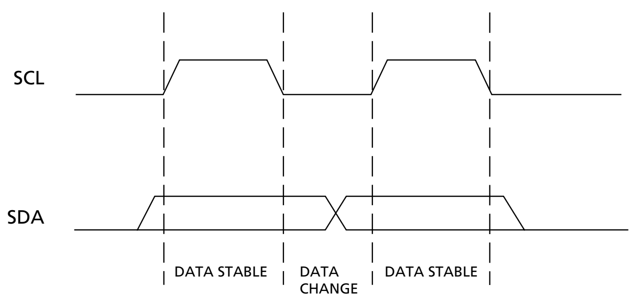


Figure 1
Data Validity

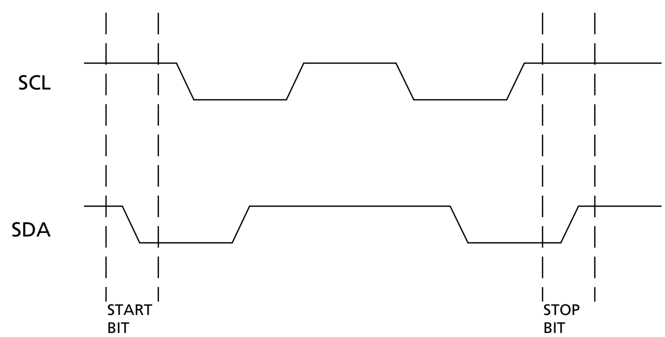


Figure 2
Definition of Start and Stop

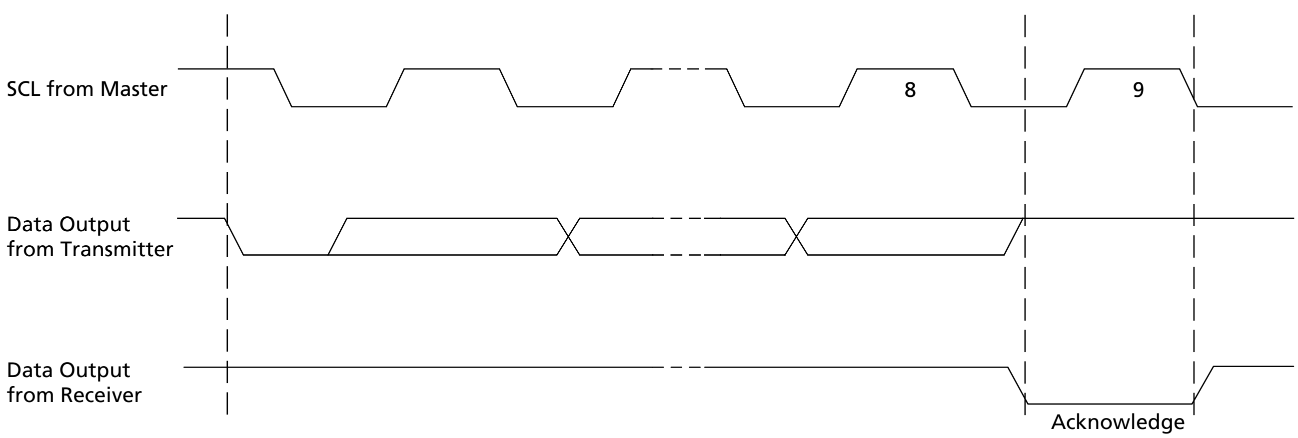


Figure 3
Acknowledge Response From Receiver

SERIAL PRESENCE-DETECT MATRIX

BYTE	DESCRIPTION	ENTRY (VERSION)	SYMBOL	MT8LSDT864A	MT16LSDT1664A
0	NUMBER OF BYTES USED BY MICRON	128		80	80
1	TOTAL NUMBER OF SPD MEMORY BYTES	256		08	08
2	MEMORY TYPE	SDRAM		04	04
3	NUMBER OF ROW ADDRESSES	12		0C	0C
4	NUMBER OF COLUMN ADDRESSES	9		09	09
5	NUMBER OF BANKS	1 or 2		01	02
6	MODULE DATA WIDTH	64		40	40
7	MODULE DATA WIDTH (continued)	0		00	00
8	MODULE VOLTAGE INTERFACE LEVELS	LVTTL		01	01
9	SDRAM CYCLE TIME (CAS LATENCY = 3)	7 (-13E) 7.5 (-133) 8 (-10E) 10 (-662)	^{t}CK	70 75 80 A0	70 75 80 A0
10	SDRAM ACCESS FROM CLOCK (CAS LATENCY = 3)	5.4 (-13E/-133) 6 (-10E) 7.5 (-662)	^{t}AC	54 60 75	54 60 75
11	MODULE CONFIGURATION TYPE	NONPARITY		00	00
12	REFRESH RATE/TYPE	15.6µs/SELF		80	80
13	SDRAM WIDTH (PRIMARY SDRAM)	8		08	08
14	ERROR-CHECKING SDRAM DATA WIDTH	NONE		00	00
15	MINIMUM CLOCK DELAY FROM BACK-TO-BACK RANDOM COLUMN ADDRESSES	1	^{t}CCD	01	01
16	BURST LENGTHS SUPPORTED	1, 2, 4, 8, PAGE		8F	8F
17	NUMBER OF BANKS ON SDRAM DEVICE	4		04	04
18	CAS LATENCIES SUPPORTED	2, 3		06	06
19	CS LATENCY	0		01	01
20	WE LATENCY	0		01	01
21	SDRAM MODULE ATTRIBUTES	UNBUFFERED		00	00
22	SDRAM DEVICE ATTRIBUTES: GENERAL	0E		0E	0E
23	SDRAM CYCLE TIME (CAS LATENCY = 2)	7.5 (-13E) 10 (-133/-10E) 15 (-662)	^{t}CK	75 A0 F0	75 A0 F0
24	SDRAM ACCESS FROM CK (CAS LATENCY = 2)	5.4 (-13E) 6 (-133/-10E) 9 (-662)	^{t}AC	54 60 90	54 60 90
25	SDRAM CYCLE TIME (CAS LATENCY = 1)	–	^{t}CK	00	00
26	SDRAM ACCESS FROM CK (CAS LATENCY = 1)	–	^{t}AC	00	00
27	MINIMUM ROW PRECHARGE TIME	15 (-13E) 20 (-133/-10E) 30 (-662)	^{t}RP	0F 14 1E	0F 14 1E
28	MINIMUM ROW ACTIVE TO ROW ACTIVE	14 (-13E) 15 (-133) 20 (-10E/-662)	^{t}RRD	0E 0F 14	0E 0F 14

NOTE: "1"/"0": Serial Data, "driven to HIGH"/"driven to LOW."

SERIAL PRESENCE-DETECT MATRIX (continued)

BYTE	DESCRIPTION	ENTRY (VERSION)	SYMBOL	MT8LSDT864A	MT16LSDT1664A
29	MINIMUM RAS# TO CAS# DELAY	15 (-13E) 20 (-133/-10E) 30 (-662)	^{t}RCD	0F 14 1E	0F 14 1E
30	MINIMUM RAS# PULSE WIDTH	37 (-13E) 44 (-133) 50 (-10E) 60 (-662)	^{t}RAS	25 2C 32 3C	25 2C 32 3C
31	MODULE BANK DENSITY	64MB		10	10
32	COMMAND AND ADDRESS SETUP TIME	1.5 (-13E/-133) 2 (-10E/-662)	^{t}AS, ^{t}CMS	15 20	15 20
33	COMMAND AND ADDRESS HOLD TIME	0.8 (-13E/-133) 1 (-10E/-662)	^{t}AH, ^{t}CMH	08 10	08 10
34	DATA SIGNAL INPUT SETUP TIME	1.5 (-13E/-133) 2 (-10E/-662)	^{t}DS	15 20	15 20
35	DATA SIGNAL INPUT HOLD TIME`	0.8(-13E/-133) 1 (-10E/-662)	^{t}DH	08 10	08 10
36-61	RESERVED			00	00
62	SPD REVISION	REV. 1.2		12	12
63	CHECKSUM FOR BYTES 0-62	(-13E) (-133) (-10E) (-662)		4F 9D E5 B8	50 9E E6 B9
64	MANUFACTURER'S JEDEC ID CODE	MICRON		2C	2C
65-71	MANUFACTURER'S JEDEC ID CODE (continued)			FF	FF
72	MANUFACTURING LOCATION			01 02 03 04 05 06 07 08 09	01 02 03 04 05 06 07 08 09
73-90	MODULE PART NUMBER (ASCII)			xx	xx
91	PCB IDENTIFICATION CODE	1 2 3 4 5		01 02 03 04 05	01 02 03 04 05

NOTE: 1. "1"/"0": Serial Data, "driven to HIGH"/"driven to LOW."
2. x = Variable Data.

SERIAL PRESENCE-DETECT MATRIX (continued)

BYTE	DESCRIPTION	ENTRY (VERSION)	SYMBOL	MT8LSDT864A	MT16LSDT1664A
91	PCB IDENTIFICATION CODE (continued)	6		06	06
		7		07	07
		8		08	08
		9		09	09
92	IDENTIFICATION CODE (continued)	0		00	00
93	YEAR OF MANUFACTURE IN BCD			xx	xx
94	WEEK OF MANUFACTURE IN BCD			xx	xx
95-98	MODULE SERIAL NUMBER			xx	xx
99-125	MANUFACTURER-SPECIFIC DATA (RSVD)			–	–
126	SYSTEM FREQUENCY	100 MHz (-13E/-133/-10E)		64	64
		66 MHz (-662)		66	66
127	SDRAM COMPONENT AND CLOCK DETAIL	(-13E/-133/-10E)		AF	FF
		(-662)		CF	FF

NOTE: 1. "1"/"0": Serial Data, "driven to HIGH"/"driven to LOW."
2. x = Variable Data.

COMMANDS

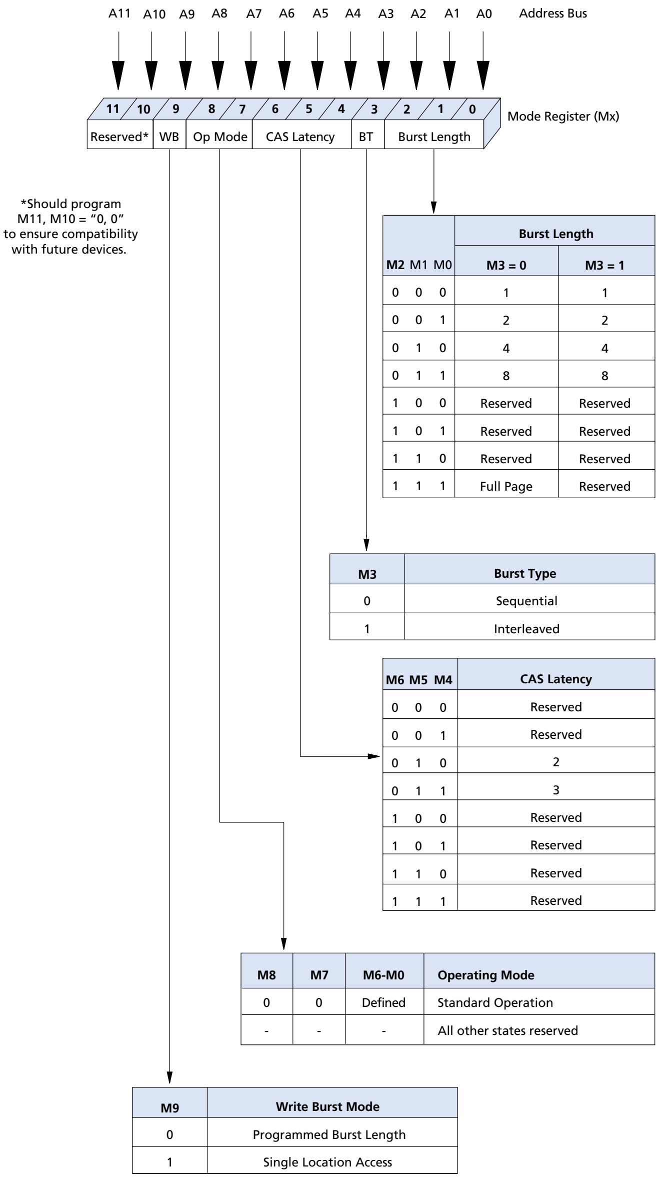
Truth Table 1 provides a general reference of available commands. For a more detailed description of commands and operations, refer to the 64Mb x4, x8, x16 SDRAM data sheet.

TRUTH TABLE 1 – COMMANDS AND DQMB OPERATION

(Note: 1)

NAME (FUNCTION)	CS#	RAS#	CAS#	WE#	DQMB	ADDR	DQs	NOTES
COMMAND INHIBIT (NOP)	H	X	X	X	X	X	X	
NO OPERATION (NOP)	L	H	H	H	X	X	X	
ACTIVE (Select bank and activate row)	L	L	H	H	X	Bank/Row	X	3
READ (Select bank and column, and start READ burst)	L	H	L	H	L/H[8]	Bank/Col	X	4
WRITE (Select bank and column, and start WRITE burst)	L	H	L	L	L/H[8]	Bank/Col	Valid	4
BURST TERMINATE	L	H	H	L	X	X	Active	
PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	X	Code	X	5
AUTO REFRESH or SELF REFRESH (Enter self refresh mode)	L	L	L	H	X	X	X	6, 7
LOAD MODE REGISTER	L	L	L	L	X	Op-Code	X	2
Write Enable/Output Enable	–	–	–	–	L	–	Active	8
Write Inhibit/Output High-Z	–	–	–	–	H	–	High-Z	8

NOTE:
1. CKE is HIGH for all commands shown except SELF REFRESH.
2. A0-A11 define the op-code written to the Mode Register.
3. A0-A11 provide row address, and BA0, BA1 determine which bank is made active.
4. A0-A8 provide column address; A10 HIGH enables the auto precharge feature (nonpersistent), while A10 LOW disables the auto precharge feature; BA0, BA1 determine which bank is being read from or written to.
5. A10 LOW: BA0, BA1 determine which bank is being precharged. A10 HIGH: all banks are precharged and BA0, BA1 are "Don't Care."
6. This command is AUTO REFRESH if CKE is HIGH, SELF REFRESH if CKE is LOW.
7. Internal refresh counter controls row addressing; all inputs and I/Os are "Don't Care" except for CKE.
8. Activates or deactivates the DQs during WRITEs (zero-clock delay) and READs (two-clock delay).



M2 M1 M0	Burst Length M3 = 0	Burst Length M3 = 1
0 0 0	1	1
0 0 1	2	2
0 1 0	4	4
0 1 1	8	8
1 0 0	Reserved	Reserved
1 0 1	Reserved	Reserved
1 1 0	Reserved	Reserved
1 1 1	Full Page	Reserved

M3	Burst Type
0	Sequential
1	Interleaved

M6 M5 M4	CAS Latency
0 0 0	Reserved
0 0 1	Reserved
0 1 0	2
0 1 1	3
1 0 0	Reserved
1 0 1	Reserved
1 1 0	Reserved
1 1 1	Reserved

M8	M7	M6-M0	Operating Mode
0	0	Defined	Standard Operation
-	-	-	All other states reserved

M9	Write Burst Mode
0	Programmed Burst Length
1	Single Location Access

Figure 4
Mode Register Definition

Table 1
Burst Definition

Burst Length	Starting Column Address			Order of Accesses Within a Burst	
				Type = Sequential	Type = Interleaved
2			A0		
			0	0-1	0-1
			1	1-0	1-0
4		A1	A0		
		0	0	0-1-2-3	0-1-2-3
		0	1	1-2-3-0	1-0-3-2
		1	0	2-3-0-1	2-3-0-1
		1	1	3-0-1-2	3-2-1-0
8	A2	A1	A0		
	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0
Full Page (y)	n = A0-A8 (location 0-y)			Cn, Cn + 1, Cn + 2 Cn + 3, Cn + 4... ...Cn - 1, Cn...	Not supported

NOTE:
1. For full-page accesses: y = 512.
2. For a burst length of two, A1-A8 select the block-of-two burst; A0 selects the starting column within the block.
3. For a burst length of four, A2-A8 select the block-of-four burst; A0-A1 select the starting column within the block.
4. For a burst length of eight, A3-A8 select the block-of-eight burst; A0-A2 select the starting column within the block.
5. For a full-page burst, the full row is selected, and A0-A8 select the starting column.
6. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.
7. For a burst length of one, A0-A8 select the unique column to be accessed, and Mode Register bit M3 is ignored.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{DD} Supply Relative to V_{SS} .... -1V to +4.6V
Voltage on Inputs, NC or I/O Pins
Relative to V_{SS} .... -1V to +4.6V
Operating Temperature, T_A (ambient) ... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +125°C
Power Dissipation 8W

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(Notes: 1,2) (V_{DD} = +3.3V ±0.3V)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
SUPPLY VOLTAGE		V_{DD}	3	3.6	V	
INPUT HIGH VOLTAGE: Logic 1; All inputs		V_{IH}	2	V_{DD} + 0.3	V	3
INPUT LOW VOLTAGE: Logic 0; All inputs		V_{IL}	-0.5	0.8	V	3
INPUT LEAKAGE CURRENT: Any input 0V ≤ V_{IN} ≤ V_{DD} (All other pins not under test = 0V)	DQMB0-DQMB7	I_{I1}	-10	10	µA	4
	CK0-CK3, S0#-S3#	I_{I2}	-20	20	µA	
	CKE0-CKE1	I_{I3}	-40	40	µA	
	RAS#, CAS#, A0-A11, BA0-BA1, WE#	I_{I4}	-80	80	µA	4
OUTPUT LEAKAGE CURRENT: DQs are disabled; 0V ≤ V_{OUT} ≤ V_{DD}	DQ0-DQ63	I_{OZ}	-10	10	µA	4
OUTPUT LEVELS: Output High Voltage (I_{OUT} = -4mA)		V_{OH}	2.4	–	V	
Output Low Voltage (I_{OUT} = 4mA)		V_{OL}	–	0.4	V	

NOTE:
1. All voltages referenced to V_{SS}.
2. An initial pause of 100µs is required after power-up, followed by two AUTO REFRESH commands, before proper device operation is ensured. The two AUTO REFRESH command wake-ups should be repeated any time the ^tREF refresh requirement is exceeded.
3. V_{IH} overshoot: V_{IH} (MAX) = V_{DD} + 2V for a pulse width ≤ 10ns, and the pulse width cannot be greater than one third of the cycle rate. V_{IL} undershoot: V_{IL} (MIN) = -2V for a pulse width ≤ 10ns, and the pulse width cannot be greater than one third of the cycle rate.
4. 64MB module values will be half of those shown.

I_{DD} SPECIFICATIONS AND CONDITIONS

(Notes: 1-4) (V_{DD} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	SIZE	MAX -13E	MAX -133	MAX -10E	MAX -662	UNITS	NOTES
OPERATING CURRENT: Active Mode; Burst = 2; READ or WRITE; $^tRC = {}^tRC$ (MIN); CAS latency = 3	I_{DD1}	64MB	1,000	920	760	720	mA	5, 6, 7, 8
		128MB	1,360	1,280	1,040	960		
STANDBY CURRENT: Power-Down Mode; CKE = LOW; All banks idle	I_{DD2}	64MB	16	16	16	24	mA	8
		128MB	32	32	32	48		
STANDBY CURRENT: Active Mode; S0#-S3# = HIGH; CKE = HIGH; All banks active after ^tRCD met; No accesses in progress	I_{DD3}	64MB	360	360	280	240	mA	5, 9, 7, 8
		128MB	720	720	560	480		
OPERATING CURRENT: Burst Mode; Continuous burst; READ or WRITE; All banks active; CAS latency = 3	I_{DD4}	64MB	1,200	1,120	960	840	mA	5, 6, 7, 8
		128MB	1,560	1,480	1,240	1,080		
AUTO REFRESH CURRENT: CKE = HIGH; S0#-S3# = HIGH — $^tRC = {}^tRC$ (MIN); CL = 3	I_{DD5}	64MB	1,840	1,680	1,520	1,360	mA	5, 6, 7, 8, 9, 10
		128MB	2,200	2,040	1,800	1,600		
AUTO REFRESH CURRENT: CKE = HIGH; S0#-S3# = HIGH — ^tRC = 15.625µs; CL = 3	I_{DD6}	64MB	24	24	24	24	mA	
		128MB	48	48	48	48		
SELF REFRESH CURRENT: CKE ≤ 0.2V	I_{DD7}	64MB	8	8	8	16	mA	11
		128MB	16	16	16	32		

NOTE:

1. All voltages referenced to V_{SS}.
2. An initial pause of 100µs is required after power-up, followed by two AUTO REFRESH commands, before proper device operation is ensured. The two AUTO REFRESH command wake-ups should be repeated any time the ^tREF refresh requirement is exceeded.
3. AC timing and I_{DD} tests have V_{IL} = 0V and V_{IH} = 3V, with timing referenced to 1.5V crossover point. If the input transition time is longer than 1ns, then the timing is referenced at V_{IL} (MAX) and V_{IL} (MIN) and no longer at the 1.5V crosspover point.
4. I_{DD} specifications are tested after the device is properly initialized.
5. I_{DD} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
6. The I_{DD} current will decrease as the CAS latency is reduced. This is due to the fact that the maximum cycle rate is slower as the CAS latency is reduced.
7. Address transitions average one transition every two clocks.
8. ^tCK = 7.5ns for -133, 10ns for -10E and 15ns for -662.
9. Other input signals are allowed to transition no more than once every two clocks and are otherwise at valid V_{IH} or V_{IL} levels.
10. CKE is high during refresh command period (^tRFC [MIN]) else CKE is low. The $I_{DD}6$ limit is actually a nominal value and does not result in a fail value.
11. Enables on-chip refresh and address counters.

CAPACITANCE

(Note: 1)

PARAMETER		SYMBOL	64MB MIN	64MB MAX	128MB MIN	128MB MAX	UNITS
Input Capacitance: A0-A11, BA0, BA1, RAS#, CAS#, WE#		C_{I1}	22	30	44	60	pF
Input Capacitance: CK0-CK3		C_{I2}	12	18	12	18	pF
Input Capacitance: S0#-S3#		C_{I3}	12	16	12	16	pF
Input Capacitance: CKE0, CKE1		C_{I4}	22	30	22	30	pF
Input Capacitance: DQMB0#-DQMB7#		C_{I5}	4	6	7	9	pF
Input Capacitance: SCL, SA0-SA2		C_{I6}	–	6	–	6	pF
Input/Output Capacitance: DQ0-DQ63, SDA		C_{IO}	6	8	10	14	pF

NOTE: This parameter is sampled. V_{DD} = +3.3V; f = 1 MHz.

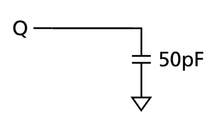
SDRAM COMPONENT* AC ELECTRICAL CHARACTERISTICS

(Notes: 1-6; notes appear below and on next page)

AC CHARACTERISTICS			-13E (PC133)		-133 (PC133)		-10E (PC100)		-662 (PC66)			
PARAMETER		SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from CK (pos. edge)	CL = 3	^tAC		5.4		5.4		6		7.5	ns	7
	CL = 2	^tAC		5.4		6		6		9	ns	
Address hold time		^tAH	0.8		0.8		1		1		ns	
Address setup time		^tAS	1.5		1.5		2		2		ns	
CK high-level width		^tCH	2.5		2.5		3		3		ns	
CK low-level width		^tCL	2.5		2.5		3		3		ns	
Clock cycle time	CL = 3	^tCK	7		7.5		8		10		ns	8
	CL = 2	^tCK	7.5		10		10		15		ns	8
CKE hold time		^tCKH	0.8		0.8		1		1		ns	
CKE setup time		^tCKS	1.5		1.5		2		2		ns	
CS#, RAS#, CAS#, WE#, DQM hold time		^tCMH	0.8		0.8		1		1		ns	
CS#, RAS#, CAS#, WE#, DQM setup time		^tCMS	1.5		1.5		2		2		ns	
Data-in hold time		^tDH	0.8		0.8		1		1		ns	
Data-in setup time		^tDS	1.5		1.5		2		2		ns	
Data-out high-impedance time	CL = 3	^tHZ		5.4		5.4		6		8	ns	9
	CL = 2	^tHZ		5.4		7		7		10	ns	9
Data-out low-impedance time		^tLZ	1		1		1		2		ns	
Data-out hold time (load)		^tOH	2.7		2.7		3		3		ns	
Data-out hold time (no load)		^tOH_N	1.8		1.8		1.8		n/a		ns	10
ACTIVE to PRECHARGE command		^tRAS	37	120,000	44	120,000	50	120,000	60	120,000	ns	
ACTIVE to ACTIVE command period		^tRC	60		66		70		90		ns	
AUTO REFRESH period		^tRCAR	15		66		70		90		ns	
ACTIVE to READ or WRITE delay		^tRCD		64	20		20		30		ns	
Refresh period (4,096 cycles)		^tREF	66			64		64		64	ms	
PRECHARGE command period		^tRP	15		20		20		30		ns	
ACTIVE bank A to ACTIVE bank B command		^tRRD	14		15		20		20		ns	
Transition time		^tT	0.3	1.2	0.3	1.2	0.3	1.2	1	1.2	ns	11
WRITE recovery time		^tWR	1 CK + 7ns		1 CK + 7.5ns		1 CK + 8ns		1 CK + 8ns		–	12
			14		15		15		15		ns	13
Exit SELF REFRESH to ACTIVE command		^tXSR	67			75		80		90	ns	14

*Specifications for the SDRAM components used on the module.

NOTE:
1. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ +70°C) is ensured.
2. An initial pause of 100µs is required after power-up, followed by two AUTO REFRESH commands, before proper device operation is ensured. The two AUTO REFRESH command wake-ups should be repeated any time the ^tREF refresh requirement is exceeded.
3. AC characteristics assume ^tT = 1ns.
4. In addition to meeting the transition rate specification, the clock and CKE must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
5. Outputs measured at 1.5V with equivalent load:



NOTES: (continued)

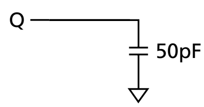
6. AC timing and I_{DD} tests have V_{IL} = 0V and V_{IH} = 3V, with timing referenced to 1.5V crossover point. If the input transition time is longer than 1ns, then the timing is referenced at V_{IL} (MAX) and V_{IL} (MIN) and no longer at the 1.5V crosspover point.
7. ^{t}AC for -133 at CL = 3 with no load is 4.6ns and is guaranteed by design.
8. The clock frequency must remain constant (stable clock is defined as a signal cycling within timing constraints specified for the clock pin) during access or precharge states (READ, WRITE, including ^{t}WR, and PRECHARGE commands). CKE may be used to reduce the data rate.
9. ^{t}HZ defines the time at which the output achieves the open circuit condition; it is not a reference to V_{OH} or V_{OL}. The last valid data element will meet ^{t}OH before going High-Z.
10. Parameter guaranteed by design.
11. AC characteristics assume ^{t}T = 1ns.
12. Auto precharge mode only. The precharge timing budget (^{t}RP) begins 7.5ns/8ns after the first clock delay, after the last WRITE is executed.
13. Precharge mode only.
14. CK must be toggled a minimum of two times during this period.

AC FUNCTIONAL CHARACTERISTICS

(Notes: 1-6)

PARAMETER		SYMBOL	-133	-13E/ -10E	-662	UNITS	NOTES
READ/WRITE command to READ/WRITE command		^{t}CCD	1	1	1	^{t}CK	7
CKE to clock disable or power-down entry mode		^{t}CKED	1	1	1	^{t}CK	8
CKE to clock enable or power-down exit setup mode		^{t}PED	1	1	1	^{t}CK	8
DQM to input data delay		^{t}DQD	0	0	0	^{t}CK	7
DQM to data mask during WRITEs		^{t}DQM	0	0	0	^{t}CK	7
DQM to data high-impedance during READs		^{t}DQZ	2	2	2	^{t}CK	7
WRITE command to input data delay		^{t}DWD	0	0	0	^{t}CK	7
Data-in to ACTIVE command		^{t}DAL	5	4	4	^{t}CK	9, 10
Data-in to PRECHARGE command		^{t}DPL	2	2	2	^{t}CK	10, 11
Last data-in to burst STOP command		^{t}BDL	1	1	1	^{t}CK	7
Last data-in to new READ/WRITE command		^{t}CDL	1	1	1	^{t}CK	7
Last data-in to PRECHARGE command		^{t}RDL	2	2	2	^{t}CK	10, 11
LOAD MODE REGISTER command to ACTIVE or REFRESH command		^{t}MRD	2	2	2	^{t}CK	12
Data-out to high-impedance from PRECHARGE command	CL = 3	^{t}ROH	3	3	3	^{t}CK	7
	CL = 2	^{t}ROH	2	2	2	^{t}CK	7

NOTE:
1. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ +70°C) is ensured.
2. An initial pause of 100µs is required after power-up, followed by two AUTO REFRESH commands, before proper device operation is ensured. The two AUTO REFRESH command wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
3. AC characteristics assume ^{t}T = 1ns.
4. In addition to meeting the transition rate specification, the clock and CKE must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
5. Outputs measured at 1.5V with equivalent load:



6. AC timing and I_{DD} tests have V_{IL} = 0V and V_{IH} = 3V, with timing referenced to 1.5V crossover point. If the input transition time is longer than 1ns, then the timing is referenced at V_{IL} (MAX) and V_{IL} (MIN) and no longer at the 1.5V crosspover point.
7. Required clocks are specified by JEDEC functionality and are not dependent on any timing parameter.
8. Timing actually specified by ^{t}CKS; clock(s) specified as a reference only at minimum cycle rate.
9. Timing actually specified by ^{t}WR plus ^{t}RP; clock(s) specified as a reference only at minimum cycle rate.
10. Based on ^{t}CK = 143 MHz for 13E, ^{t}CK = 133 MHz for -75, 100 MHz for -10E and 66 MHz for -662.
11. Timing actually specified by ^{t}WR.
12. JEDEC and PC100 specify three clocks.

SERIAL PRESENCE-DETECT EEPROM DC OPERATING CONDITIONS

(Note: 1) (V_{DD} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
SUPPLY VOLTAGE	V_{DD}	3	3.6	V	
INPUT HIGH VOLTAGE: Logic 1; All inputs	V_{IH}	V_{DD} x 0.7	V_{DD} + 0.5	V	
INPUT LOW VOLTAGE: Logic 0; All inputs	V_{IL}	-1	V_{DD} x 0.3	V	
OUTPUT LOW VOLTAGE: I_{OUT} = 3mA	V_{OL}	–	0.4	V	
INPUT LEAKAGE CURRENT: V_{IN} = GND to V_{DD}	I_{LI}	–	10	µA	
OUTPUT LEAKAGE CURRENT: V_{OUT} = GND to V_{DD}	I_{LO}	–	10	µA	
STANDBY CURRENT: SCL = SDA = V_{DD} - 0.3V; All other inputs = GND or 3.3V +10%	I_{SB}	–	30	µA	
POWER SUPPLY CURRENT: SCL clock frequency = 100 KHz	I_{DD}	–	2	mA	

NOTE: 1. All voltages referenced to V_{SS}.

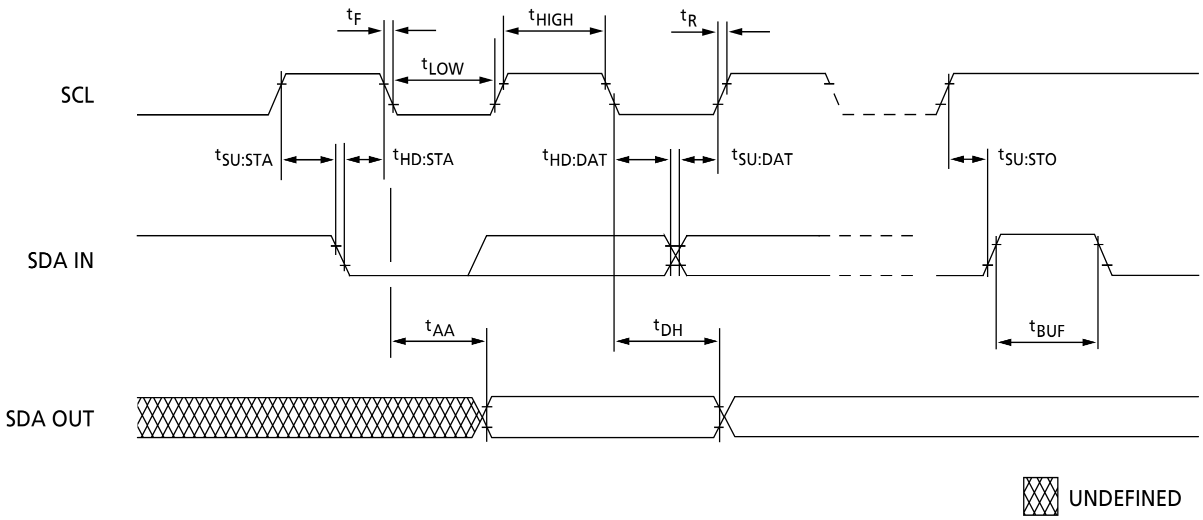
SERIAL PRESENCE-DETECT EEPROM AC OPERATING CONDITIONS

(Note: 1) (V_{DD} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
SCL LOW to SDA data-out valid	^{t}AA	0.3	3.5	µs	
Time the bus must be free before a new transition can start	^{t}BUF	4.7		µs	
Data-out hold time	^{t}DH	300		ns	
SDA and SCL fall time	^{t}F		300	ns	
Data-in hold time	$^{t}HD:DAT$	0		µs	
Start condition hold time	$^{t}HD:STA$	4		µs	
Clock HIGH period	$^{t}HIGH$	4		µs	
Noise suppression time constant at SCL, SDA inputs	^{t}I		100	ns	
Clock LOW period	^{t}LOW	4.7		µs	
SDA and SCL rise time	^{t}R		1	µs	
SCL clock frequency	^{t}SCL		100	KHz	
Data-in setup time	$^{t}SU:DAT$	250		ns	
Start condition setup time	$^{t}SU:STA$	4.7		µs	
Stop condition setup time	$^{t}SU:STO$	4.7		µs	
WRITE cycle time	^{t}WRC		10	ms	2

NOTE:
1. All voltages referenced to V_{SS}.
2. The SPD EEPROM WRITE cycle time (^{t}WRC) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal erase/program cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistor, and the EEPROM does not respond to its slave address.

SPD EEPROM

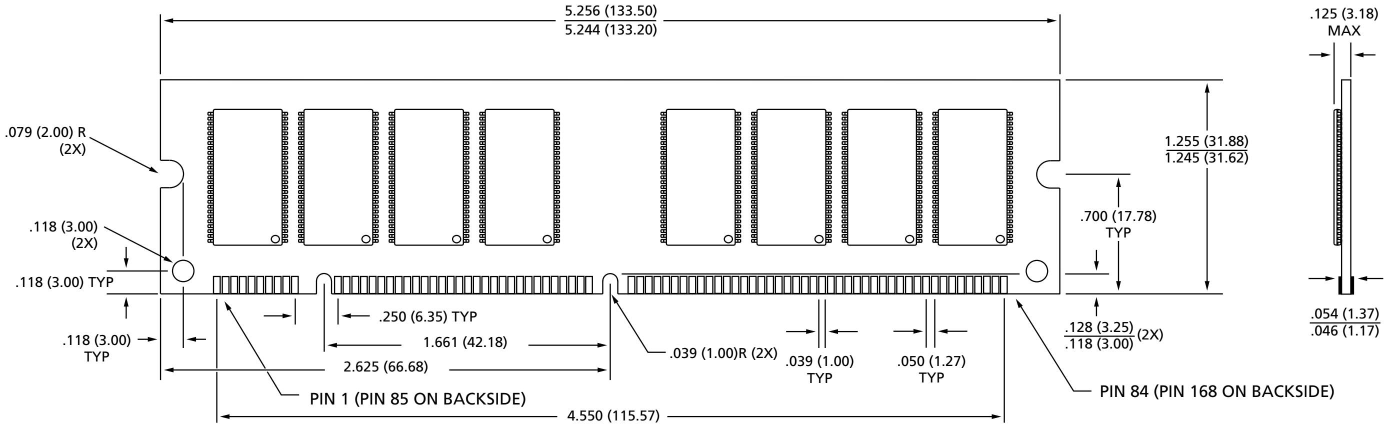


SERIAL PRESENCE-DETECT EEPROM TIMING PARAMETERS

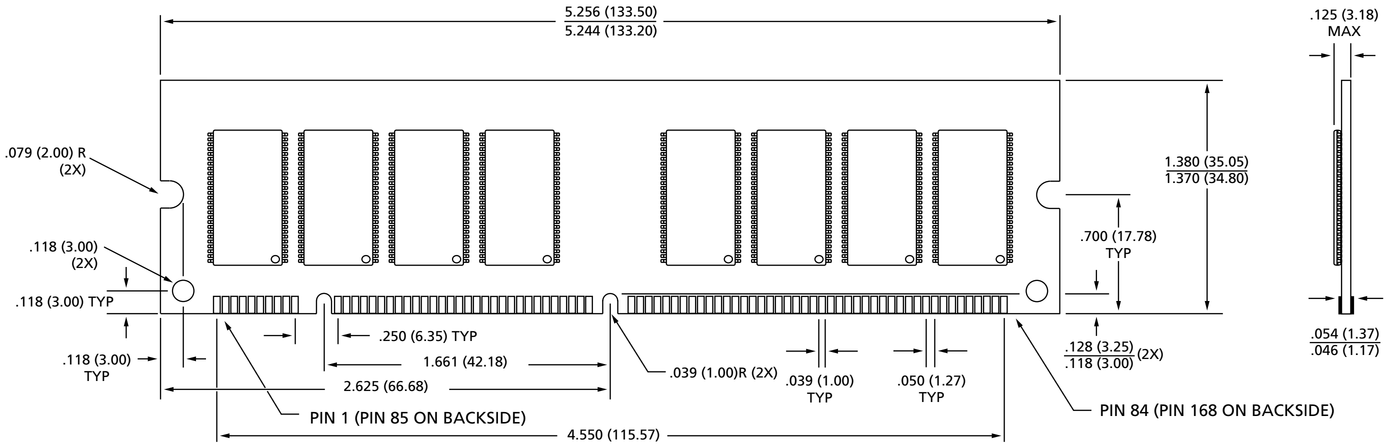
SYMBOL	MIN	MAX	UNITS
^tAA	0.3	3.5	µs
^tBUF	4.7		µs
^tDH	300		ns
^tF		300	ns
$^tHD:DAT$	0		µs
$^tHD:STA$	4		µs

SYMBOL	MIN	MAX	UNITS
^tHIGH	4		µs
^tLOW	4.7		µs
^tR		1	µs
$^tSU:DAT$	250		ns
$^tSU:STA$	4.7		µs
$^tSU:STO$	4.7		µs

168-PIN DIMM
(64MB, 66 MHz)

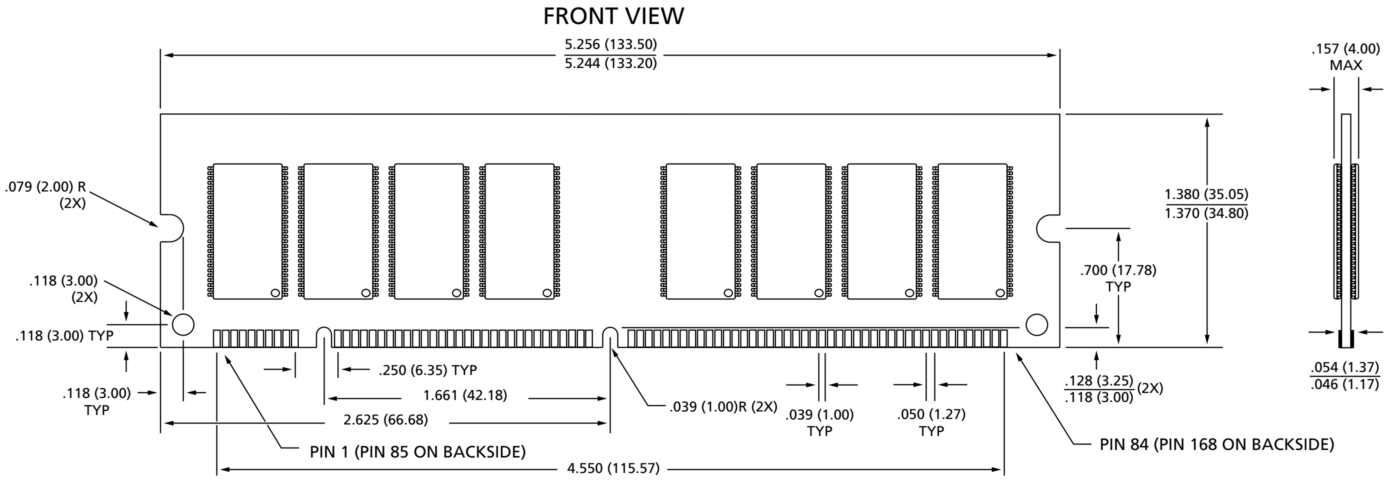


168-PIN DIMM
(64MB, 100 MHz)



NOTE: All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

168-PIN DIMM
(128MB)



NOTE: All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

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