

# HN62414 Series

# HN62434 Series

## 4M (256K x 16-bit) and (512K x 8-bit) Mask ROM

### ■ DESCRIPTION

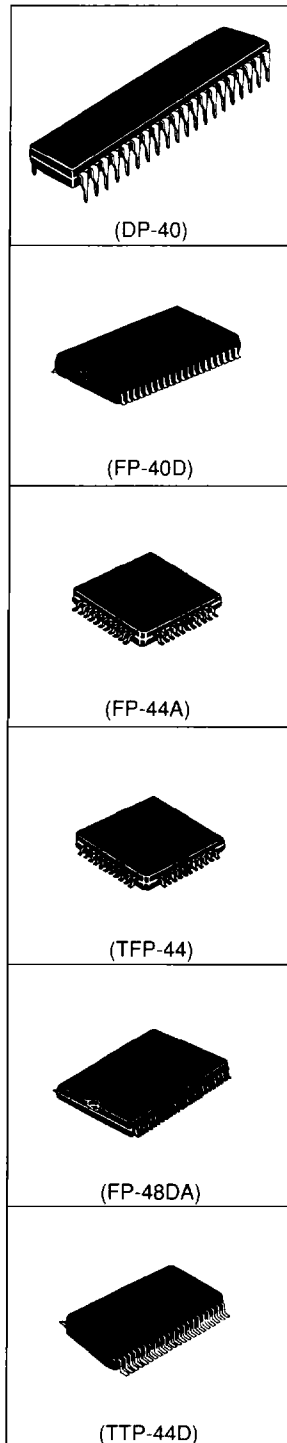
The Hitachi HN62414/HN62434 Series is a 16-Megabit CMOS Mask Programmable Read Only Memory organized as 262,144 x 16-bit and 524,288 x 8-bit.

The low power consumption of this device makes it ideal for battery powered, portable systems. In addition, the high density and high speed provide enough capacity and high performance to be used as a character generator in laser printers.

Hitachi's HN62414/HN62434 Series is offered in 40-pin Plastic DIP, 40-lead Plastic SOP, 44-lead Plastic QFP and TQFP, 48-lead Plastic SOP and 44-lead Plastic TSOP packages.

### ■ FEATURES

- Single Power Supply:  
 $V_{CC} = 5 V \pm 10\%$
- Fast Access Times:  
120 ns/150 ns/170 ns (max)
- Low Power Consumption:  
Active Current: 100 mW (typ)  
Standby Current: 5  $\mu$ W (typ)
- User Selectable Organization:  
256K x 16-bit (Word-Wide)  
512K x 8-bit (Byte-Wide)  
Switchable with BHE pin
- TTL-Compatible Inputs and Outputs
- Three-State Data Outputs
- Packages:
  - 40-pin Plastic DIP
  - 40-lead Plastic SOP
  - 44-lead Plastic QFP
  - 44-lead Plastic TQFP
  - 48-lead Plastic SOP
  - 44-lead Plastic TSOP (Type II)

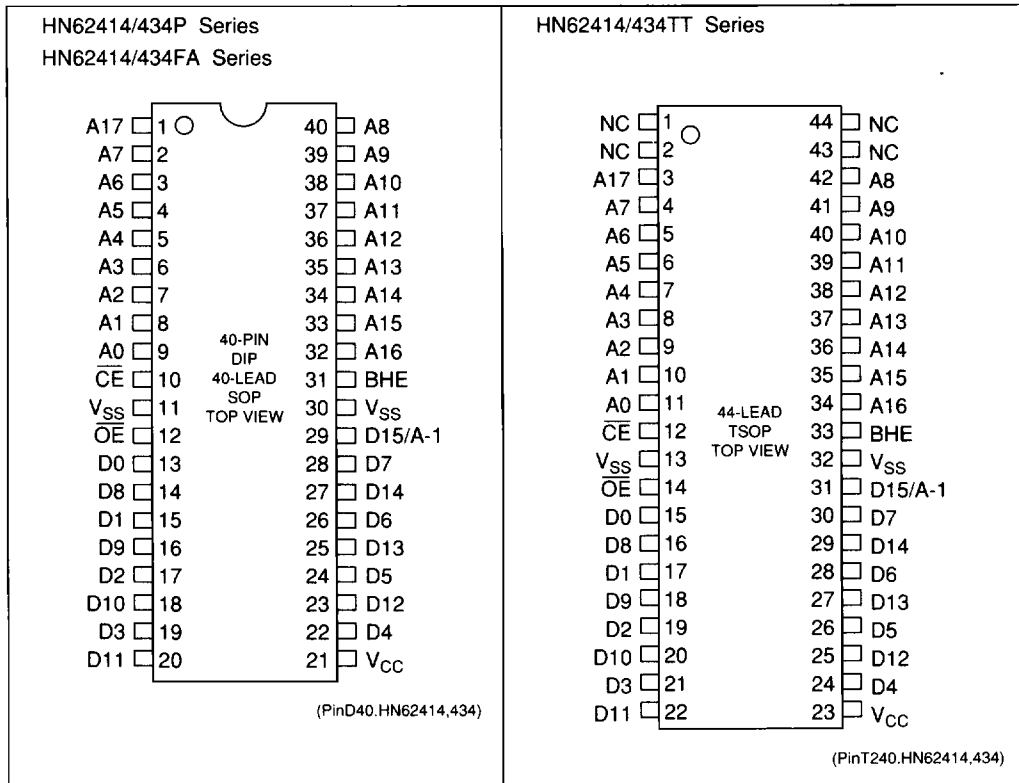


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■ ORDERING INFORMATION

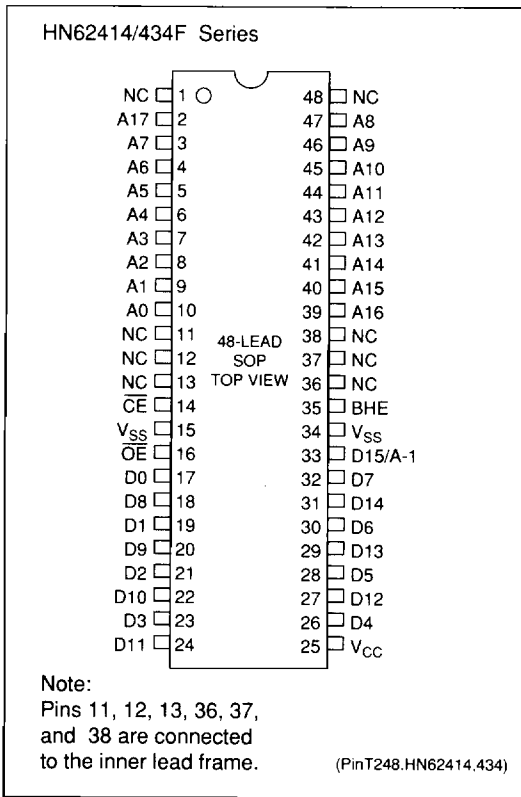
Type No.	Access Time	Package
HN62434P HN62414P	120/150 ns 170 ns	40-pin Plastic DIP (DP-40)
HN62434FA HN62414FA	120/150 ns 170 ns	40-lead Plastic SOP (FP-40D)
HN62434FP HN62414FP	120/150 ns 170 ns	44-lead Plastic QFP (FP-44A)
HN62434TFP HN62414TFP	120/150 ns 170 ns	44-lead Plastic TQFP (TFP-44)
HN62434F HN62414F	120/150 ns 170 ns	48-lead Plastic SOP (FP-48DA)
HN62434TT HN62414TT	120/150 ns 170 ns	44-lead Plastic TSOP (TTP-44D)

■ PIN ARRANGEMENT



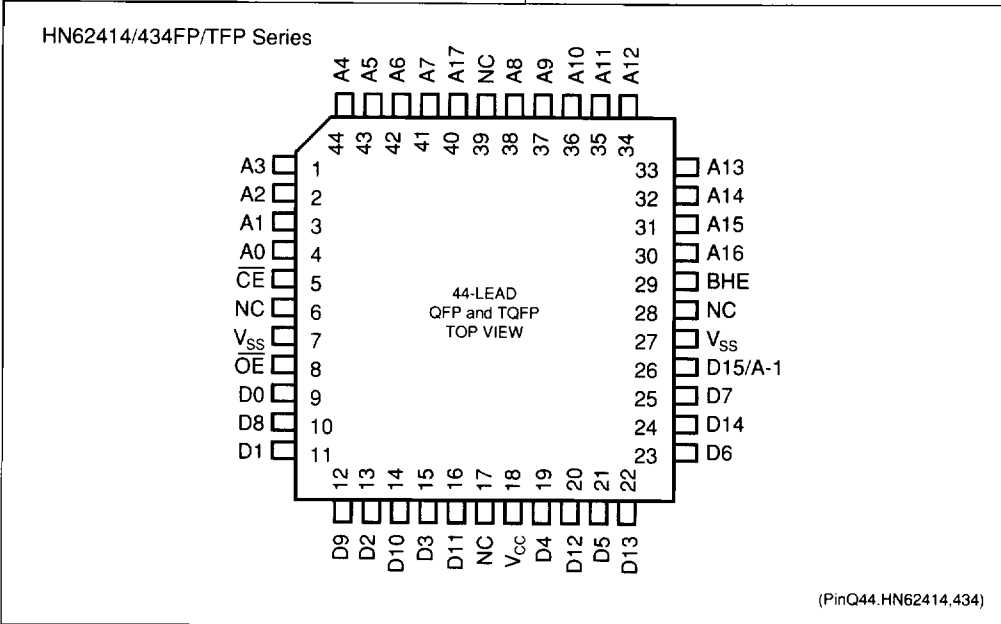
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■ PIN ARRANGEMENT (cont.)



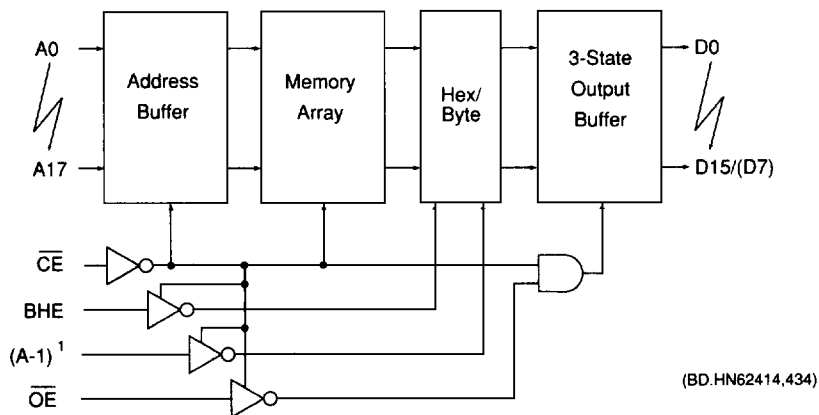
■ PIN DESCRIPTION

Pin Name	Function
$A_0 - A_{17}$	Address
$A_{-1}$	Address (Word-Wide)
$D_0 - D_{15}$	Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
BHE	Byte Enable
$V_{CC}$	Power Supply
$V_{SS}$	Ground
NC	No Connection



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■ BLOCK DIAGRAM



- Notes:
1. \* :  $A_1$  is the Least Significant Address bit in Byte-Wide Mode.
  2.  $BHE = V_{IH}$  : 16-bit ( $D_{15} - D_0$ )  
 $BHE = V_{IL}$  : 8-bit ( $D_7 - D_0$ )  
 When BHE is low,  $D_{14} - D_8$  are in high impedance states.

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■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage <sup>1</sup>	$V_{CC}$	-0.3 to +7.0	V
Terminal Voltage <sup>1</sup>	$V_T$	-0.3 to $V_{CC} + 0.3$	V
Operating Temperature Range	$T_{OPR}$	0 to +70	°C
Storage Temperature Range	$T_{STG}$	-55 to +125	°C
Temperature Under Bias	$T_{BIAS}$	-20 to +85	°C

Notes: 1. With respect to  $V_{SS}$ .

■ CAPACITANCE

( $V_{CC} = 5V \pm 10\%$ ,  $V_{SS} = 0V$ ,  $T_a = 25^\circ C$ ,  $V_{IN} = 0V$ ,  $f = 1MHz$ )

Item	Symbol	Min.	Max.	Unit
Input Capacitance <sup>1</sup>	$C_{IN}$	-	15	pF
Output Capacitance <sup>1</sup>	$C_{OUT}$	-	15	pF

Notes: 1. This parameter is sampled and not 100% tested.

■ DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

( $V_{CC} = 5V \pm 10\%$ ,  $V_{SS} = 0V$ ,  $T_a = 0$  to  $70^\circ C$ )

Item	Symbol	Min.	Max.	Unit	Test Condition
Input Leakage Current	$I_{LI}$	-	10	$\mu A$	$V_{IN} = 0$ to $V_{CC}$
Output Leakage Current	$I_{LO}$	-	10	$\mu A$	$\overline{CE} = 2.2V$ , $V_{OUT} = 0$ to $V_{CC}$
Operating $V_{CC}$ Current	$I_{CC}$	-	50	mA	$V_{CC} = 5.5V$ , $I_{DOUT} = 0$ mA, $t_{RC} = \text{Min.}$
Standby $V_{CC}$ Current	$I_{SB}$	-	30	$\mu A$	$V_{CC} = 5.5V$ , $\overline{CE} \geq V_{CC} - 0.2V$
Input Voltage	$V_{IH}$	2.2	$V_{CC} + 0.3$	V	
	$V_{IL}$	-0.3	0.8	V	
Output Voltage	$V_{OH}$	2.4	-	V	$I_{OH} = -205 \mu A$
	$V_{OL}$	-	0.4	V	$I_{OL} = 1.6$ mA

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**■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION**
 $(V_{CC} = 5V \pm 10\%, V_{SS} = 0V, T_a = 0 \text{ to } 70^\circ\text{C})$ 
**Test Conditions**

- Input pulse levels: 0.8 V / 2.4 V
- Input rise and fall times:  $\leq 10$  ns
- Output load: 1 TTL Gate + CL = 100 pF (Including jig capacitance)
- Input/Output Timing Reference level: 1.5 V

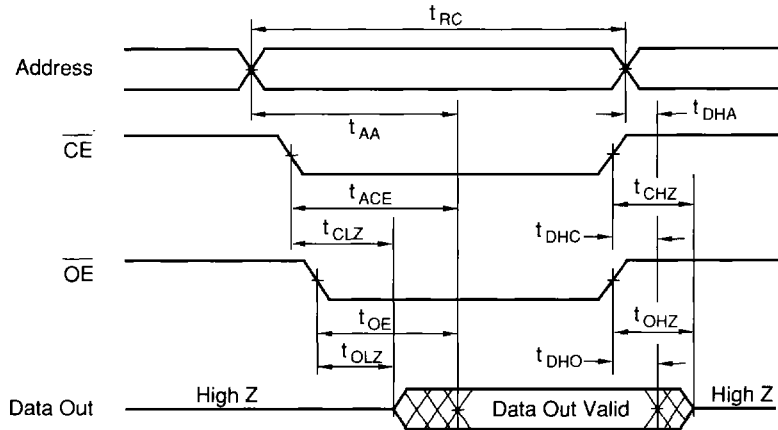
Item	Symbol	HN62434-12		HN62434-15		HN62414-17		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	$t_{RC}$	120	-	150	-	170	-	ns
Address Access Time	$t_{AA}$	-	120	-	150	-	170	ns
$\overline{CE}$ Access Time	$t_{ACE}$	-	120	-	150	-	170	ns
$\overline{OE}$ Access Time	$t_{OE}$	-	60	-	70	-	70	ns
BHE Access Time	$t_{BHE}$	-	120	-	150	-	170	ns
Output Hold Time from Address Change	$t_{DHA}$	0	-	0	-	0	-	ns
Output Hold Time from $\overline{CE}$	$t_{DHC}$	0	-	0	-	0	-	ns
Output Hold Time from $\overline{OE}$	$t_{DHO}$	0	-	0	-	0	-	ns
Output Hold Time from BHE	$t_{DHB}$	0	-	0	-	0	-	ns
$\overline{CE}$ to Output in High Z <sup>1</sup>	$t_{CHZ}$	-	60	-	70	-	70	ns
$\overline{OE}$ to Output in High Z <sup>1</sup>	$t_{OHZ}$	-	60	-	70	-	70	ns
BHE to Output in High Z <sup>1</sup>	$t_{BHZ}$	-	60	-	70	-	70	ns
$\overline{CE}$ to Output in Low Z	$t_{CLZ}$	5	-	10	-	10	-	ns
$\overline{OE}$ to Output in Low Z	$t_{OLZ}$	5	-	10	-	10	-	ns
BHE to Output in Low Z	$t_{BLZ}$	5	-	10	-	10	-	ns

Note: 1.  $t_{CHZ}$ ,  $t_{OHZ}$ , and  $t_{BHZ}$  are defined as the time at which the output becomes an open circuit and are not referenced to output voltage levels.

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■ READ TIMING WAVEFORM

Word Mode (BHE =  $V_{IH}$ ) or Byte Mode (BHE =  $V_{IL}$ )

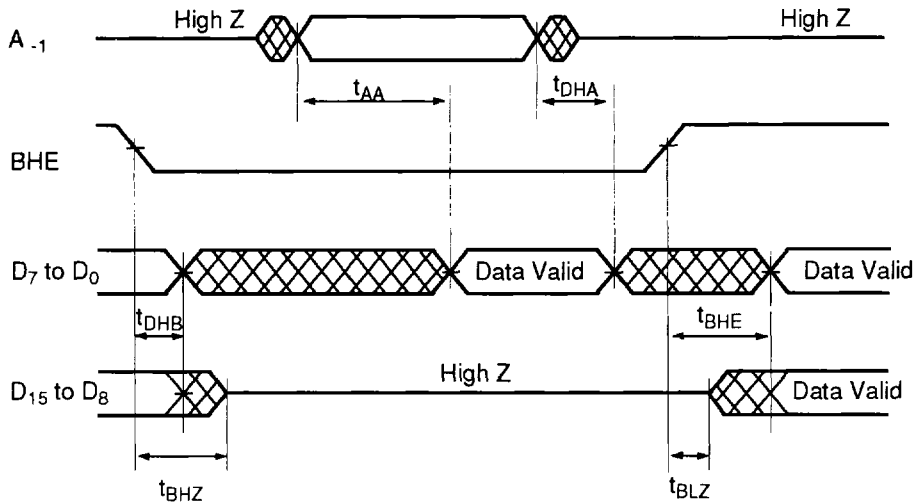


(TD.R.HN62414,434)

- Note:
1.  $t_{DHA}$ ,  $t_{DHC}$ ,  $t_{DHO}$  are determined by the faster time.
  2.  $t_{AA}$ ,  $t_{ACE}$ ,  $t_{OE}$  are determined by the slower time.
  3.  $t_{CLZ}$ ,  $t_{OLZ}$  are determined by the slower time.

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Word Mode/Byte Mode Switch



(TD.R1.HN62414,434)

- Note:
1.  $\overline{CE}$  and  $\overline{OE}$  are enabled,  $A_{17}$  to  $A_0$  are valid.
  2.  $D_{15}/A_{-1}$  pin is in the output state when BHE is high,  $\overline{CE}$  and  $\overline{OE}$  are enabled. Therefore, the input signals of opposite phase to the output must not be applied to them.

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