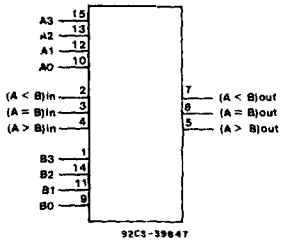
File Number **1770**

CD54/74HC85
CD54/74HCT85

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

4-Bit Magnitude Comparator

Type Features:

- *Buffered inputs and outputs*
- *Typical propagation delay = 13 ns (Data to Output) @ V_{CC} = 5V, C_L =15 pF, T_A = 25°C*
- *Serial or Parallel expansion without external gating.*

The RCA-CD54/74HC/HCT85 are high-speed magnitude comparators that use silicon-gate CMOS technology to achieve operating speeds similar to LSTTL with the low power consumption of standard CMOS integrated circuits.

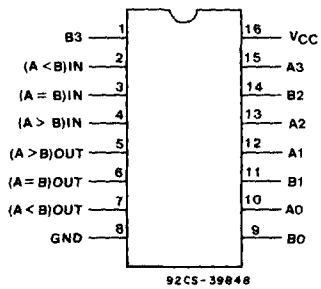
These 4-bit devices compare two binary, BCD, or other monotonic codes and present the three possible magnitude results at the outputs (A > B, A < B, and A = B). The 4-bit input words are weighted (A0 to A3 and B0 to B3), where A3 and B3 are the most significant bits.

The HC/HCT85 are expandable without external gating, in both serial and parallel fashion. The upper part of the truth table indicates operation using a single device or devices in a serially-expanded application. The parallel expansion scheme is described by the last three entries in the truth table. Circuits for serial and parallel comparison of 12 bits are shown in figures 3 and 4, respectively.

The CD54HC/HCT85 are supplied in 16-lead ceramic dual-in-line packages (F suffix). The CD74HC/HCT85 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- *Fanout (Over Temperature Range):*
  Standard Outputs - 10 LSTTL Loads
  Bus Driver Outputs - 15 LSTTL Loads
- *Wide Operating Temperature Range:*
  CD74HC/HCT/HCU: -40 to +85°C
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation
  High Noise Immunity:
  N_{IL} = 30%, N_{IH} = 30% of V_{CC}; @ V_{CC} = 5 V
- *CD54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation
  Direct LSTTL Input Logic Compatibility
  V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.
  CMOS Input Compatibility $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}



TERMINAL ASSIGNMENT

CD54/74HC85
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MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) ..... -0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} + 0.5$ V) ..... ±20mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC} + 0.5$ V) ..... ±20mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR $-0.5 \text{ V} < V_O < V_{CC} + 0.5$ V) ..... ±25mA
DC V_{CC} OR GROUND CURRENT (I_{CC}) ..... ±50mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H ..... -55 to +125°C
PACKAGE TYPE E, M ..... -40 to +85°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only ..... +300°C

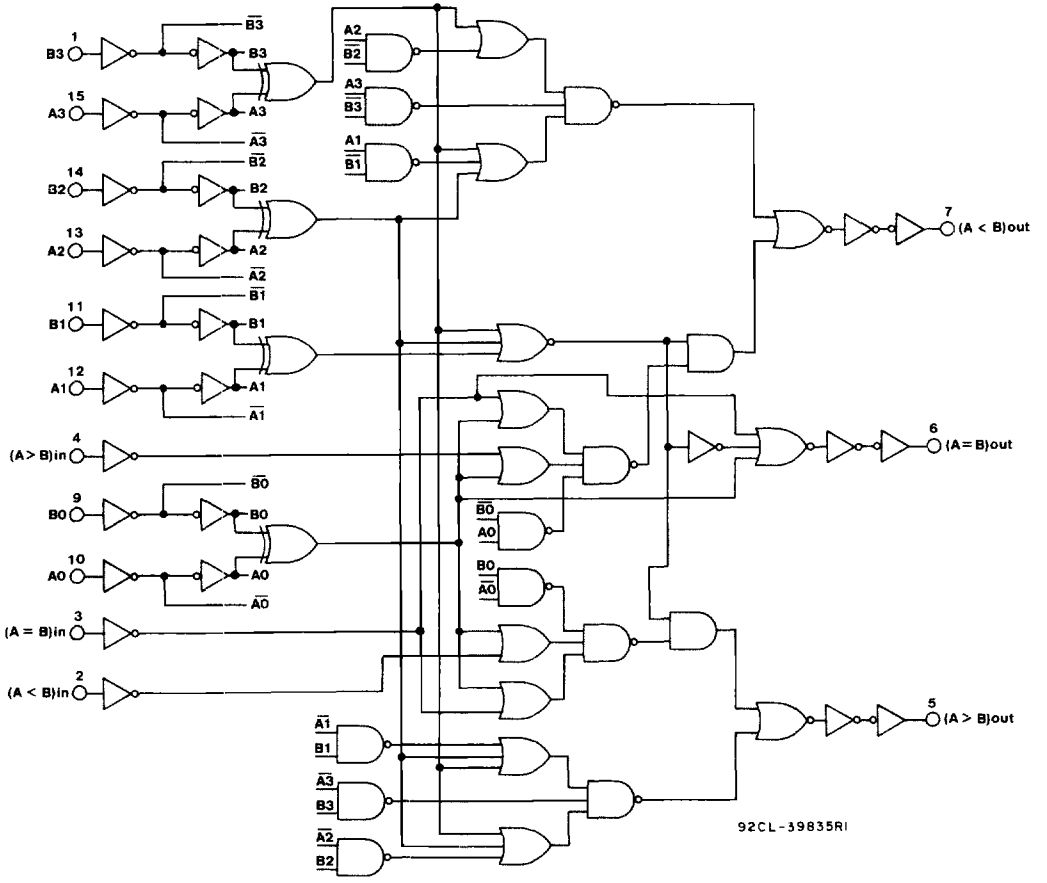

Fig. 1 - Logic diagram

CD54/74HC85
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TRUTH TABLE

Comparing Inputs				Cascading Inputs			Outputs			
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B	
A3 > B3	X	X	X	X	X	X	H	L	L	single device or series cascading
A3 < B3	X	X	X	X	X	X	L	H	L	
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L	
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L	
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	H	L	L	
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L	
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L	
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L	
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L	
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L	
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H	L	L	H	
A3 = B3	A2 = B2	A1 = B1	A0 = B0	X	X	H	L	L	H	parallel cascading
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	L	L	L	L	
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	L	H	H	L	

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	
Input Rise and Fall Times t_r, t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.

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STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC85/CD54HC85										CD74HCT85/CD54HCT85										UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES			
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C			
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max		
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—		4.5									
			4.5	3.15	—	—	3.15	—	3.15	—	—	to	2	—	—	2	—	2	—	V	
			6	4.2	—	—	4.2	—	4.2	—		5.5									
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5		4.5									
			4.5	—	—	1.35	—	1.35	—	1.35	—	to	—	—	0.8	—	0.8	—	0.8	V	
			6	—	—	1.8	—	1.8	—	1.8		5.5									
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V	
			4.5	4.4	—	—	4.4	—	4.4	—											
			6	5.9	—	—	5.9	—	5.9	—											
TTL Loads	V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V	
		-5.2	6	5.48	—	—	5.34	—	5.2	—											
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V	
			4.5	—	—	0.1	—	0.1	—	0.1											
			6	—	—	0.1	—	0.1	—	0.1											
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V	
		5.2	6	—	—	0.26	—	0.33	—	0.4											
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} and Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA	
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA	
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA	

* For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
A0-A3, B0-B3 and (A=B) in	1.5
(A>B) in, (A<B) in	1

*Unit Load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 360 μA max. @ 25°C.

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A 25°C, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	C_L (pF)	TYPICAL 54/74HC	TYPICAL 54/74HCT	UNITS
Propagation Delay An, Bn to (A>B)out, (A<B)out	t_{PLH} t_{PHL}	15	16	15	ns
An, Bn to (A=B) out			14	17	ns
(A>B)in,(A<B),in (A=B)in to (A>B)out,(A<B)out			11	12	ns
(A=B) in to (A=B)out			9	13	ns
Power Dissipation Capacitance*	C_{PD}	—	24	26	pF

*C_{PD} is used to determine the dynamic power consumption, per package.
$P_D = V_{CC}^2 fi\ (C_{PD} + C_L)$ where: fi=input frequency
C_L=output load capacitance
V_{CC}=supply voltage

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC	TEST CONDITION V_{CC} V	LIMITS 25°C HC Min	HC Max	HCT Min	HCT Max	-40°C to +85°C 74HC Min	74HC Max	74HCT Min	74HCT Max	-55°C to +125°C 54HC Min	54HC Max	54HCT Min	54HCT Max	UNITS
Propagation Delay t_{PLH} An, Bn to (A>B)out, t_{PHL} (A<B)out	2	—	195	—	—	—	245	—	—	—	295	—	—	ns
	4.5	—	39	—	37	—	47	—	46	—	59	—	56	
	6	—	33	—	—	—	42	—	—	—	50	—	—	
An, Bn to (A=B)out	2	—	175	—	—	—	240	—	—	—	265	—	—	ns
	4.5	—	35	—	40	—	44	—	50	—	53	—	60	
	6	—	30	—	—	—	37	—	—	—	45	—	—	
(A>B)in, (A<B)in, (A=B)in to (A>B)out, (A<B)out	2	—	140	—	—	—	175	—	—	—	210	—	—	ns
	4.5	—	28	—	30	—	35	—	38	—	42	—	45	
	6	—	24	—	—	—	30	—	—	—	36	—	—	
(A=B)in to (A=B)out	2	—	120	—	—	—	150	—	—	—	180	—	—	ns
	4.5	—	24	—	31	—	30	—	39	—	36	—	47	
	6	—	20	—	—	—	26	—	—	—	31	—	—	
Output Transition Time t_{TLH} t_{THL}	2	—	75	—	—	—	95	—	—	—	110	—	—	ns
	4.5	—	15	—	15	—	19	—	19	—	22	—	22	
	6	—	13	—	—	—	16	—	—	—	19	—	—	—
Input Capacitance C_I	—	—	10	—	10	—	10	—	10	—	10	—	10	pF

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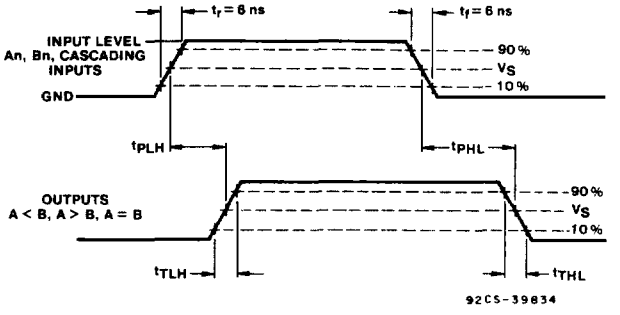

	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_S	50% V_{CC}	1.3 V

Fig. 2 - Transition times, propagation delay times

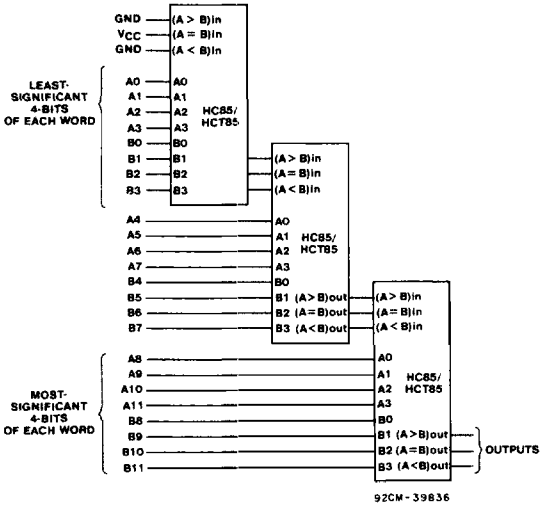

Fig. 3 - Series cascading --- comparing 12-bit words.

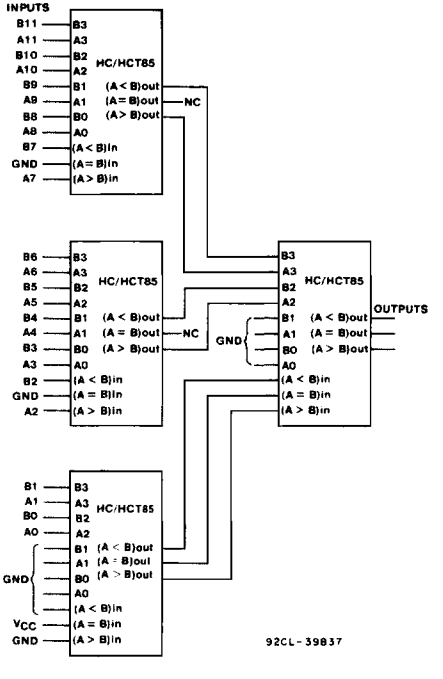

Fig. 4 - Parallel cascading --- comparing 12-bit words.