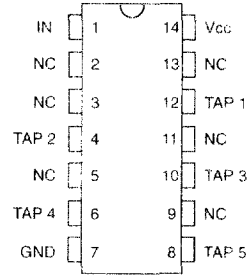
DALLAS SEMICONDUCTOR

DS1005
5-Tap Silicon Delay Line

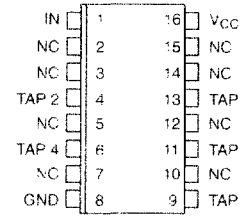
FEATURES

- All-silicon time delay
- 5 taps equally spaced
- Delay tolerance ±2 ns or ±3%, whichever is greater
- Stable and precise over temperature and voltage range
- Leading and trailing edge accuracy
- Economical
- Auto-insertable, low profile
- Standard 14-pin DIP, 8-pin DIP, or 16-pin SOIC
- Tape and reel available for surface-mount
- Low-power CMOS
- TTL/CMOS compatible
- Vapor phase, IR and wave solderability
- Custom delays available
- Quick turn prototypes
- Extended temperature range available

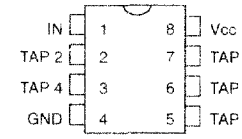
PIN ASSIGNMENT



DS1005 14-PIN DIP (300 MIL)
See Mech. Drawings Section



DS1005S 16-PIN SOIC
(300 MIL)
See Mech. Drawings Section



DS1005M 8-PIN DIP (300 MIL)
See Mech. Drawings Section

PIN DESCRIPTION

TAP 1 – TAP 5	– Tap Output Number
V_{CC}	– +5 Volts
GND	– Ground
NC	– No Connection
IN	– Input

DESCRIPTION

The DS1005 5-Tap Silicon Delay Line provides five equally spaced taps with delays ranging from 12 ns to 250 ns, with an accuracy of ±2 ns or ±3%, whichever is greater. This device is offered in a standard 14-pin DIP, making it compatible with existing delay line products. Space-saving 8-pin DIPs and 16-pin SOICs are also available. Both enhanced performance and superior reliability over hybrid technology is achieved by the combination of a 100% silicon delay line and industry standard DIP and SOIC packaging. In order to maintain complete pin compatibility, DIP packages are available with hybrid lead configurations. The DS1005 reproduces the input logic level at each tap after the fixed delay specified by the dash number in NO TAG. The device is designed with both leading and trailing edge accuracy. Each tap is capable of driving up to ten 74LS loads. Dallas Semiconductor can customize standard products to meet special needs. For special requests and rapid delivery, call (972) 371–4348.