FUJITSU SEMICONDUCTOR
DATA SHEET

8-bit Proprietary Microcontroller

CMOS

F²MC-8L MB89530H Series

MB89537H/537HC/538H/538HC/P538/PV530

■ DESCRIPTION

The MB89530H series has been developed as a general-purpose version of the F²MC*-8L family consisting of proprietary 8-bit, single-chip microcontrollers.

In addition to a compact instruction set, the microcontroller contains a variety of peripheral functions such as I²C interface, 8-bit PWM,16-bit timer, 21-bit timer/counter, 8-bit PWC, 17-bit watch prescalar, UART, Serial I/O, 6-bit PPG, 12-bit PPG , an A/D converter, and external interrupt(level and edge), watch timer reset..

*: F²MC stands for FUJITSU Flexible Microcontroller.

■ FEATURES

- Various package options
  Three types of QFP packages (1-mm, 0.65-mm, or 0.5-mm lead pitch)
  SH-DIP package
- High-speed operating capability at low voltage
- Minimum execution time: 0.32 μs/12.5MHz
- F²MC-8L family CPU core

  Instruction set optimized for controllers { Multiplication and division instructions / 16-bit arithmetic operations / Test and branch instructions / Bit manipulation instructions, etc.

- Dual-clock control system
  Main clock: 12.5MHz ; Subclock: 32.768KHz
- Five types of timers
  8-bit PWM timer: 2 channels timers (also usable as a interval timer)
  16-bit timer/counter
  21-bit time-base timer
  8 bit PWC timer operation
  Watch prescaler (17 bits)
- UART
  CLK-synchronous/CLK-asynchronous data transfer capable
- Serial interface
  Switchable transfer direction allows communication with various equipment.
- 10-bit A/D converter (8 channels)
  Activation by timebase timer , external trigger or software.

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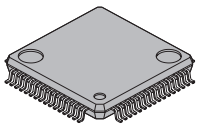
- Two Type of progammable Pulse Generator (PPG)
  6-bit PPG with program-selectable pulse width and period.
  12-bit PPG (2 channels) with program-selectable pulse width and period.
- I^2C interface circuit
- External interrupt 1: 4 channels
  Four channels are independent and capable of wake-up from low-power consumption modes (with an edge detection function).
- External interrupt 2: 8 channels
  Eight channels are independent and capable of wake-up from low-power consumption modes (with a low level Ldetection function).
- Low-power consumption modes
  Stop mode (Oscillation stops to minimize the current consumption.)
  Sleep mode (The CPU stops to reduce the current consumption to approx. 1/3 of normal.)
  Subclock mode
  Watch mode
- Watch dog timer reset
- I/O ports: max. 53 channels

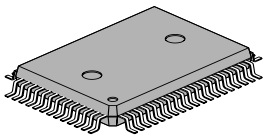
■ PACKAGE

64-pin Plastic LQFP



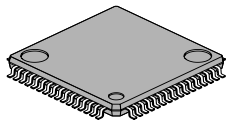
(FPT-64P-M03)

64-pin Plastic QFP



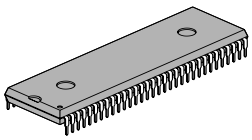
(FPT-64P-M06)

64-pin Plastic QFP



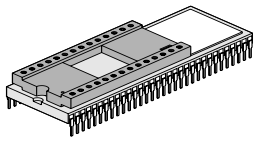
(FPT-64P-M09)

64-pin Plastic SH-DIP



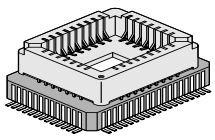
(DIP-64P-M01)

64-pin Ceramic MDIP



(MDP-64C-P02)

64-pin Ceramic MQFP



(MQP-64C-P01)

■ PRODUCT LINEUP

Part number / Parameter	MB89537H	MB89537HC	MB89538H	MB89538HC	MB89P538	MB89PV530
Classification	Mass production products (mask ROM product)				OTP	Piggy-back
ROM size	32 K x 8 bits		48 K × 8 bits			
RAM size	1K x 8 bits		2K × 8 bits			
CPU functions	Number of instructions: : 136 Instruction bit length: : 8 bits Instruction length: : 1 to 3 bytes Data bit length: : 1, 8, 16 bits Minimum execution time: : 0.32 µs/12.5 MHz Minimum interrupt processing time: : 2.88 µs/12.5 MHz					
Ports	Input port : 5 pins Output-only ports (CMOS) : 8 pins I/O ports (N-channel open drain) : 2 pins I/O ports (CMOS) : 38 pins Total : 53 pins					
Clock	Dual/Single					
Wild Register	Yes					
PWM Timer	8 bits reload timer operation(toggled output capable, operating clock cycle: 1, 8, 16, 64 tinst). 8 bits resolution PWM operation(conversion cycle:256 tinst to 256 X 64 tinst) 2 channels or combine to 1 channel with channel 1 being the count clock of channel 2.					
Pulse width count timer	8 bits timer operation (underflow output capable, operating clock cycle:1, 4, 32 tinst, external) 8 bits reload timer (toggled output capable, operating clock cycle: 1, 4, 32 tinst, external) 8 bits pulse-width measurement					
6-bit PPG	Internal 6-bit counter Output frequency: pulse width and cycle are program selectable					
12-bit PPG	2 channels, Internal 12-bit counter Output frequency: pulse width and cycle are program selectable					
I^2C interface	MB89537H/MB89538H do not have I^2C interface. 1 channel, Use a 2-wire protocol to communicate with other device					
16-bit Timer/Counter	16-bit timer operation (operating clock period: 1 t_{inst}, external) 16-bit event counter operation (rising, falling, or both edges can be selected) 16 bits x 1 channel					
Serial I/O	8-bit length; Selectable LSB-first or MSB-first; 4 shift clock mode selectable					
UART/SIO	Transfer data length: 7, 8 bits for UART, 8 bits for SIO support sub-clock mode					
UART	CLK-synchronous/CLK-asynchronous data transfer capable (4,6,7 and 8 bits with parity bit ; 5,7,8 and 9 bits without parity bit)					
External interrupt 1	Edge detection of 4 external sources; Interrupt can be generated at the same time flag is set; Can be used to release the sleep or stop mode.					
External interrupt 2	8 external interrupt input (level interrupt); Available for the wake up interrupt input.					
A/D converter	10-bit resolution × 8 channels (conversion time: 60 tinst) A/D conversion function Supports repeated activation by an external or internal clock. Reference voltage input provided (AVR).					
Standby mode	Sleep mode, stop mode and clock mode					
Process	CMOS					
Operating Voltage	3.5V ~ 5.5V				2.2V ~ 5.5 V	

Note : 1 tinst = one instruction cycle (execution time) which can be selected as 1/4, 1/8, 1/16, or 1/64 of main clock, or 1/2 of the subclock if subclock mode is selected.

■ PACKAGE AND CORRESPONDING PRODUCTS

Package \ Models	MB89537H/ 537HC	MB89538H/ 538HC	MB89P538	MB89PV530
DIP-64P-M01	O	X	O	X
FPT-64P-M03	O	O	X	X
FPT-64P-M06	O	X	O	X
FPT-64P-M09	O	O	O	X
MDP-64C-P02	X	X	X	O
MQP-64P-P01	X	X	X	O

O : Availabe X : Not available

■ DIFFERENCES AMONG PRODUCTS

1. Memory Size

Before evaluating using the OTPROM (one-time PROM) products, verify its differences from the product that will actually be used. Take particular care on the following points:

- The number of register banks available is different between the MB89PV530 and the MB89537H/538H/P538.
- The stack area, etc., is set at the upper limit of the RAM.

2. Current Consumption

- For the MB89PV530, add the current consumed by the EPROM mounted in the piggy-back socket.
- When operating at low speed, the current consumed by the one-time PROM product is greater than for the mask ROM product. However, the current consumption are roughly the same in sleep or stop mode.
- (For more information, see “■ Electrical Characteristics.”)

3. Mask Options

The functions available as options and the method of specifying options differ between products.

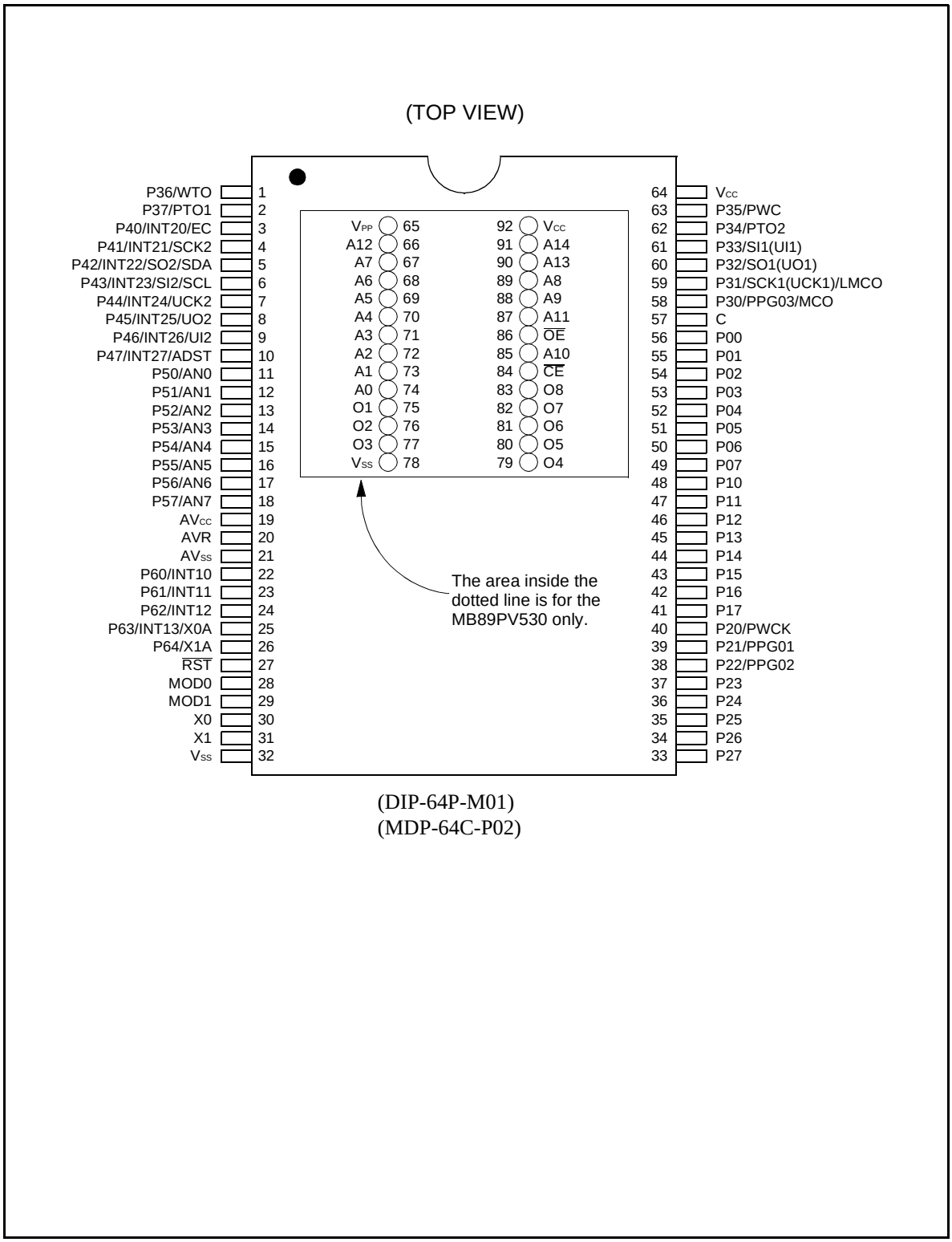
Before using options check “■ Mask Options.”

4. Functionalities different between products in MB89530 series

Functionalities	MB89537H/537HC/538H/538HC	MB89P538	MB89PV530
Power-on reset wait time	Regulator stab. time + Regulator recovery. time + Osc. stab. time	Regulator stab. time + Osc. stab. time	Osc. stab. time
Wait time for external reset in stop/sub/clock mode or wait time for external interrupt trigger recover from main stop mode	Regulator recovery time + Osc. stab. time	Osc. stab. time	
Port pin pull up resistors	Selectable by software.		Not available.
AD conversion time	60 t_{inst}*		
I^2C noise cancelling circuit	Always available independent of ICCR:DMBP bit selection.		Not available when ICCR:DMBP bit is asserted.

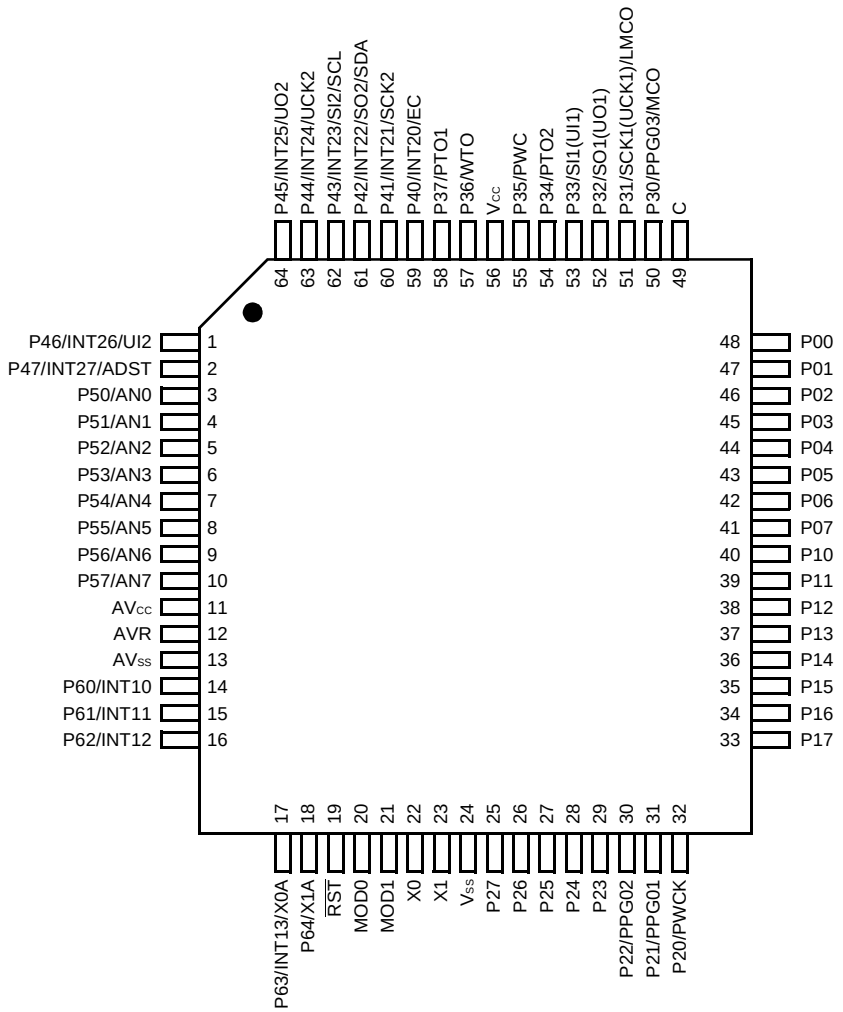
Note:For more information on t_{inst} see “■ Electrical Characteristics (4) Instruction cycles"

■ PIN ASSIGNMENT



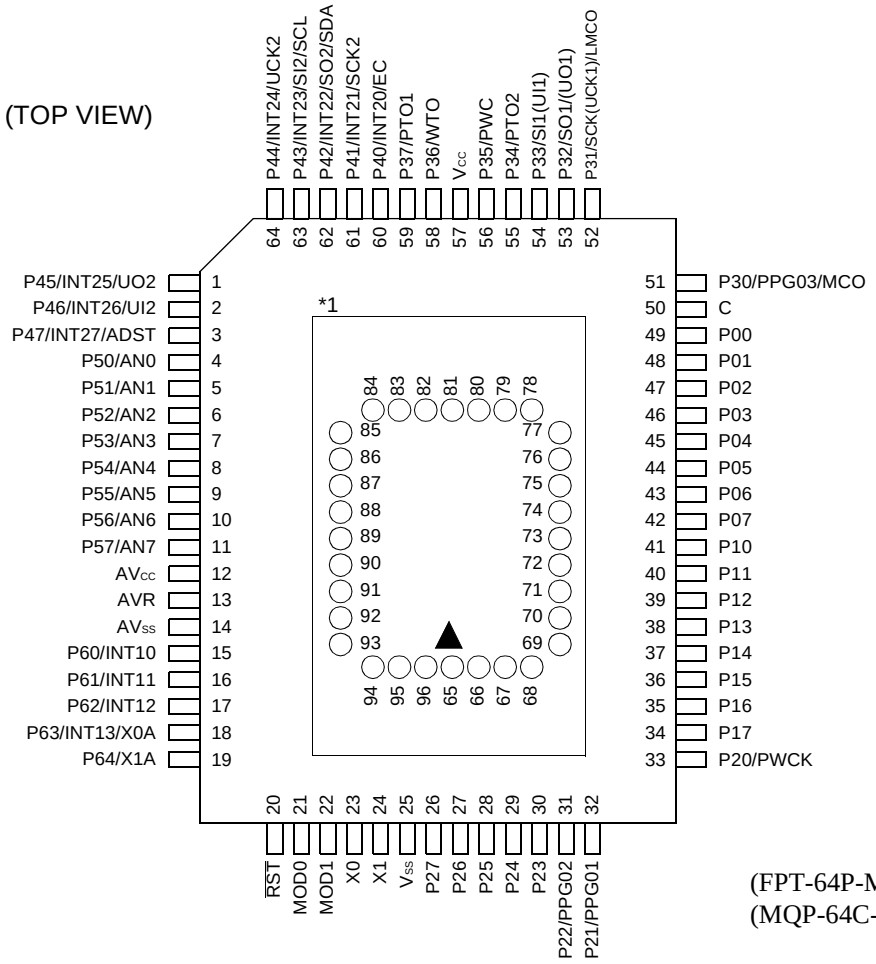
(DIP-64P-M01)
(MDP-64C-P02)

(TOP VIEW)



(FPT-64P-M03)
(FPT-64P-M09)

(TOP VIEW)



(FPT-64P-M06)
(MQP-64C-P01)

*1: Package upper-side pin assignment (MB89PV530 only)

Pin No.	Pin Symbol	Pin No.	Pin Symbol	Pin No.	Pin Symbol	Pin No.	Pin Symbol
65	N.C.	73	A2	81	N.C.	89	$\overline{OE}$
66	V_{PP}	74	A1	82	O4	90	N.C.
67	A12	75	A0	83	O5	91	A11
68	A7	76	N.C.	84	06	92	A9
69	A6	77	O1	85	07	93	A8
70	A5	78	O2	86	O8	94	A13
71	A4	79	O3	87	$\overline{CE}$	95	A14
72	A3	80	V_{SS}	88	A10	96	V_{CC}

N.C.: As connected internally, do not use.

■ PIN DESCRIPTION

Pin Number			Pin Name	Circuit Type	Function
SH-DIP*1 MDIP*2	QFP*3 MQFP*4	LQFP*5 QFP*6			
30	23	22	X0	A	Connection pins for a crystal or other oscillator. An external clock can be connected to X0. In this case, leave X1 open.
31	24	23	X1		
28	21	20	MOD0	B	Connect directly to V_{SS}.
29	22	21	MOD1		
27	20	19	$\overline{RST}$	C	Reset I/O pin. The pin is a CMOS I/O with pull-up resistor and a hysteresis input. The pin outputs a “L” level when an internal reset request is present. Inputting an “L” level initializes internal circuits.
56 - 49	49 - 42	48 - 41	P00 - P07	D	General-purpose I/O port.
48 - 41	41 - 34	40 - 33	P10- P17	D	General-purpose I/O port.
40	33	32	P20/PWCK	E	General-purpose input port. A hysteresis input. The pin is shared with the PWC Clk input.
39	32	31	P21/PPG01	D	General-purpose I/O port. The pin is shared with the PPG01 output
38	31	30	P22/PPG02	D	General-purpose I/O port. The pin is shared with the PPG02 output
37	30	29	P23	D	General-purpose I/O port.
36	29	28	P24	D	General-purpose I/O port.
35	28	27	P25	D	General-purpose I/O port.
34	27	26	P26	D	General-purpose I/O port.
33	26	25	P27	D	General-purpose I/O port.
58	51	50	P30/PPG03/ MCO	D	General-purpose I/O port. The pin is shared with the PPG03 output and main clock output.
59	52	51	P31/ SCK1(UCK1)/ LMCO	E	General-purpose input port. A hysteresis input. The pin is shared with the clock I/O of Uart/SIO and sub-clock output.
60	53	52	P32/SO1(UO1)	D	General-purpose I/O port. The pin is shared with the serial data output of Uart/SIO.
61	54	53	P33/SI1(UI1)	E	General-purpose input port. A hysteresis input. The pin is shared with the serial data input of Uart/SIO.
62	55	54	P34/PTO2	D	General-purpose I/O port. The pin is shared with the PWM timer 2 output .

*1: DIP-64P-M01, DIP-64C-A06
*2: DIP-64C-P02
*3: FPT-64P-M06
*4: MQP-64C-P01
*5: FPT-64P-M03
*6: FPT-64P-M09

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Pin Number			Pin Name	Circuit Type	Function
SH-DIP*1 MDIP*2	QFP*3 MQFP*4	LQFP*5 QFP*6			
63	56	55	P35/PWC	E	General-purpose input port. A hysteresis input. The pin is shared with the input for PWC.
1	58	57	P36/WTO	D	General-purpose I/O port. The pin is shared with the output of PWC.
2	59	58	P37/PTO1	D	General-purpose I/O port. The pin is shared with the output of PWM timer 1.
3	60	59	P40/INT20/EC	E	General-purpose input port. A hysteresis input. The pin is shared with a external interrupt input and 16-bit timer/counter input.
4	61	60	P41/INT21/ SCK2	E	General-purpose input port. A hysteresis input. The pin is shared with a external interrupt input and clock I/O for SIO.
5	62	61	P42/INT22/ SO2/SDA	G	N-channel open-drain output The pin is shared with a external interrupt input and serial data output of SIO and data line of I^2C.
6	63	62	P43/INT23/SI2/ SCL	G	N-channel open-drain output The pin is shared with a external interrupt input and serial data input for SIO and the clock I/O of I^2C
7	64	63	P44/INT24/ UCK2	E	General-purpose input port. A hysteresis input. The pin is shared with a external interrupt input and clock I/O for UART.
8	1	64	P45/INT25/UO2	E	General-purpose input port. A hysteresis input. The pin is shared with a external interrupt input and data output for UART
9	2	1	P46/INT26/UI2	E	General-purpose input port. A hysteresis input. The pin is shared with a external interrupt input and data input for UART
10	3	2	P47/INT27/ ADST	E	General-purpose input port. A hysteresis input. The pin is shared with a external interrupt input and clock input pin of A/D converter

*1: DIP-64P-M01, DIP-64C-A06
*2: DIP-64C-P02
*3: FPT-64P-M06
*4: MQP-64C-P01
*5: FPT-64P-M03
*6: FPT-64P-M09

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Pin Number			Pin Name	Circuit Type	Function
SH-DIP*1 MDIP*2	QFP*3 MQFP*4	LQFP*5 QFP*6			
11 - 18	4 - 11	3 - 10	P50/AN0 - P57/ AN7	H	N-channel open-drain output ports. The pins are shared with the analog inputs for the A/D converter.
22 - 24	15 -17	14 - 16	P60/INT10 - P62/INT12	I	General-purpose input ports. The pins are shared with the external interrupt inputs. Hysteresis inputs.
25	18	17	P63/INT13/X0A	I/A	General-purpose input ports. The pins are shared with the external interrupt inputs and sub-clock pin. Hysteresis inputs.
26	19	18	P64/X1A	J/A	General-purpose input port. The pin is shared with a sub-clock pin. A hysteresis input.
57	50	49	C	—	capacitor connection pin *7
64	57	56	V_{CC}	—	Power supply pin.
32	25	24	V_{SS}	—	Power supply pins (GND).
19	12	11	AV_{CC}	—	A/D converter power supply pin.
20	13	12	AVR	—	Reference voltage input pin for the A/D converter.
21	14	13	AV_{SS}	—	A/D converter power supply pin. Use at the same voltage level as V_{SS}.

*1: DIP-64P-M01, DIP-64C-A06 *4: MQP-64C-P01
*2: DIP-64C-P02 *5: FPT-64P-M03
*3: FPT-64P-M06 *6: FPT-64P-M09

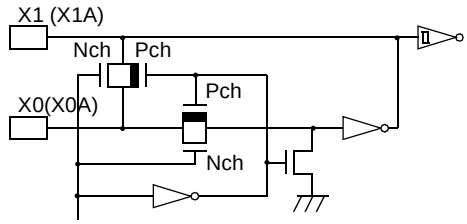
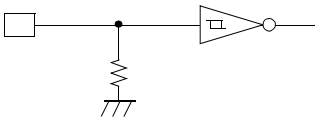
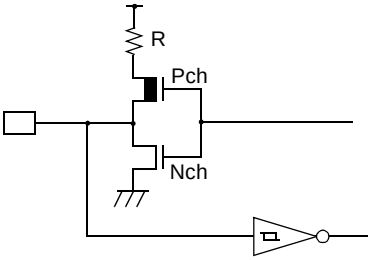
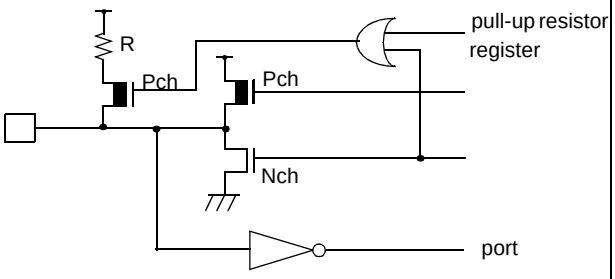
*7: When MB89PV530 is used, this pin will become a N.C. pin without internal connection.
When MB89P538 is used , this pin is used to select a regulator stabilization delay time.
If 5V used in MB89P538, this pin must be connected to Vss.
If 3V used in MB89P538, this pin must be connected to Vcc.
If MB89527H/538H/537HC/538HC are used, 0.1µF capacitor must be connected to this pin.

• External Eprom Socket (MB89PV530 only)

Pin Number		Pin Name	I/O	Function
MDIP*1	MDIP*2			
65	66	V_{PP}	O	"H" level output pin.
66	67	A12	O	Address output pins.
67	68	A7		
68	69	A6		
69	70	A5		
70	71	A4		
71	72	A3		
72	73	A2		
73	74	A1		
74	75	A0		
75	77	O1	I	Data input pins.
76	78	O2		
77	79	O3		
78	80	V_{SS}	O	Power supply pin (GND).
79	82	O4	I	Data input pins.
80	83	O5		
81	84	O6		
82	85	O7		
83	86	O8		
84	87	$\overline{CE}$	O	Chip enable pin for the ROM. Outputs "H" in standby mode.
85	88	A10	O	Address output pin.
86	89	$\overline{OE}$	O	Output enable pin for the ROM. Always outputs "L".
87	91	A11	O	Address output pins.
88	92	A9		
89	93	A8		
90	94	A13	O	
91	95	A14	O	
92	96	V_{CC}	O	Power supply pin for the EPROM.
—	65 76 81 90	N.C.	—	Internally connected pins. Always leave open.

*1: MDP-64C-P02
*2: MQP-64C-P01

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A	 Stop mode control signal	• Hysteresis input for X1(X1A) • main and sub-clock circuits
B		• Hysteresis input • The pull-down resistor (p-channel) is approx. 50kΩ for MB89567H/567HC and MB89568H/568HC only.
C		• The output pull-up resistance (P-channel) is approx. 50 kΩ. • Hysteresis input
D		• CMOS output • CMOS input • Selectable pull-up resistor option available . Approx. 50 kΩ.

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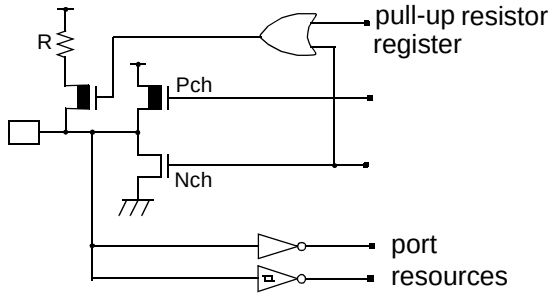
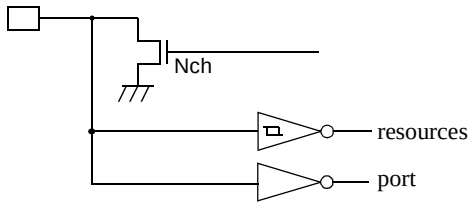
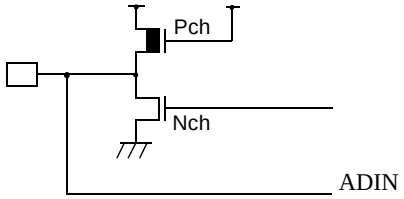
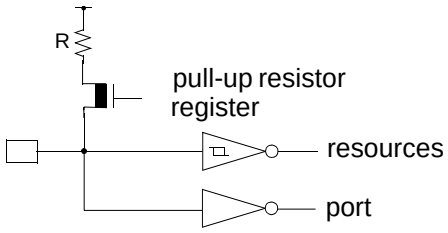
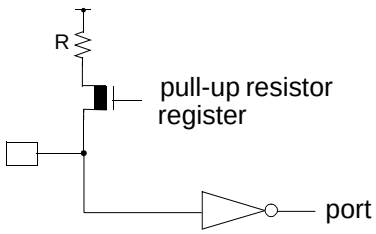
Type	Circuit	Remarks
E		• CMOS output • CMOS input port • Hysteresis input for resource • Selectable pull-up resistor option available. Approx. 50 kΩ.
G		• N-channel open-drain output • Hysteresis input for resource • CMOS input port
H		• N-channel open-drain output • Analog input (A/D converter)
I		• CMOS input port • Hysteresis input for resource • Selectable pull-up resistor option available. Approx. 50 kΩ.
J		• CMOS input • Selectable pull-up resistor option available. Approx. 50 kΩ.

■ HANDLING DEVICES

1. Preventing Latchup

Latchup may occur on CMOS ICs if voltage higher than V_{CC} or lower than V_{SS} is applied to input and output pins other than medium- to high-voltage pins or if higher than the voltage which shows on “1. Absolute Maximum Ratings” in “■ Electrical Characteristics” is applied between V_{CC} and V_{SS}.

When latchup occurs, power supply current increases rapidly and might thermally damage elements. When using, take great care not to exceed the absolute maximum ratings.

Also, take care to prevent the analog power supply (AV_{CC} and AVR) and analog input from exceeding the digital power supply (V_{CC}) when the analog system power supply is turned on and off.

2. Treatment of Unused Input Pins

Leaving unused input pins open could cause malfunctions. They should be connected to a pull-up or pull-down resistor.

3. Treatment of Power Supply Pins on Microcontrollers with A/D and D/A Converters

Connect to be AV_{CC} = DAVC = V_{CC} and AV_{SS} = AVR = V_{SS} even if the A/D and D/A converters are not in use.

4. Treatment of N.C. Pins

Be sure to leave (internally connected) N.C. pins open.

5. Power Supply Voltage Fluctuations

Although V_{CC} power supply voltage is assured to operate within the rated range, a rapid fluctuation of the voltage could cause malfunctions, even if it occurs within the rated range. Stabilizing voltage supplied to the IC is therefore important. As stabilization guidelines, it is recommended to control power so that V_{CC} ripple fluctuations (P-P value) will be less than 10% of the standard V_{CC} value at the commercial frequency (50 to 60 Hz) and the transient fluctuation rate will be less than 0.1 V/ms at the time of a momentary fluctuation such as when power is switched.

6. Precautions when Using an External Clock

Even when an external clock is used, oscillation stabilization time is required for power-on reset (optional) and wake-up from stop mode.

■ PROGRAMMING TO THE EPROM ON THE MB89P538

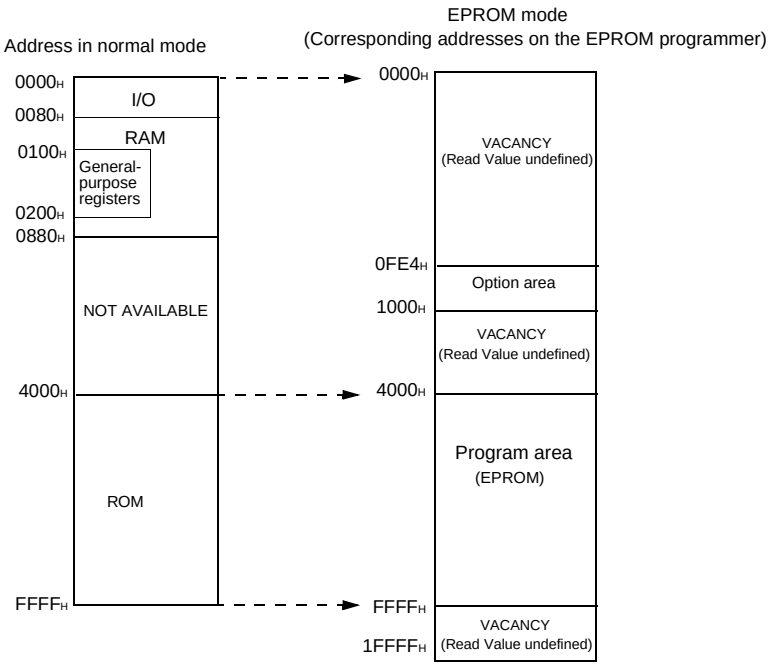
The MB89P538 is an OTPROM version of the MB89537H, MB89537HC, MB89538H, MB89538HC.

1. Features

- 48-Kbyte PROM on chip
- Equivalency to the MBM27C1001A in EPROM mode (when programmed with the EPROM programmer)

2. Memory Space

Memory space in EPROM mode is diagrammed below.



3. Programming to the EPROM

In EPROM mode, the MB89P538 functions equivalent to the MBM27C1001A. This allows the PROM to be programmed with a general-purpose EPROM programmer (the electronic signature mode cannot be used) by using the dedicated socket adapter.

- **Programming procedure**

(1) Set the EPROM programmer to the MBM27C1001A.

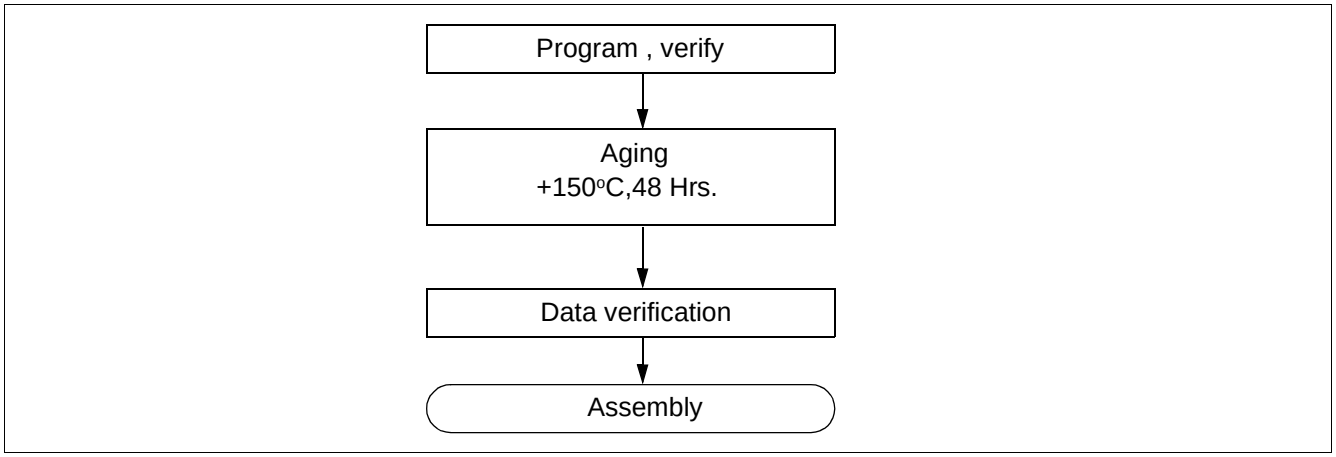
(2) Load program data into the EPROM programmer at $0FE4_H$ to $FFFF_H$

(3) Program with the EPROM programmer.

■ HANDLING THE MB89P538

1. Recommended Screening Conditions

High-temperature aging is recommended as the pre-assembly screening procedure.



2. Programming Yield

All bits cannot be programmed at Fujitsu shipping test to a blanked OTPROM microcomputer, due to its nature. For this reason, a programming yield of 100% cannot be assured at all times.

■ PROGRAMMING TO THE EPROM WITH PIGGYBACK/EVALUATION DEVICE

1. EPROM for Use

MBM27C512-20TV

2. Programming Socket Adapter

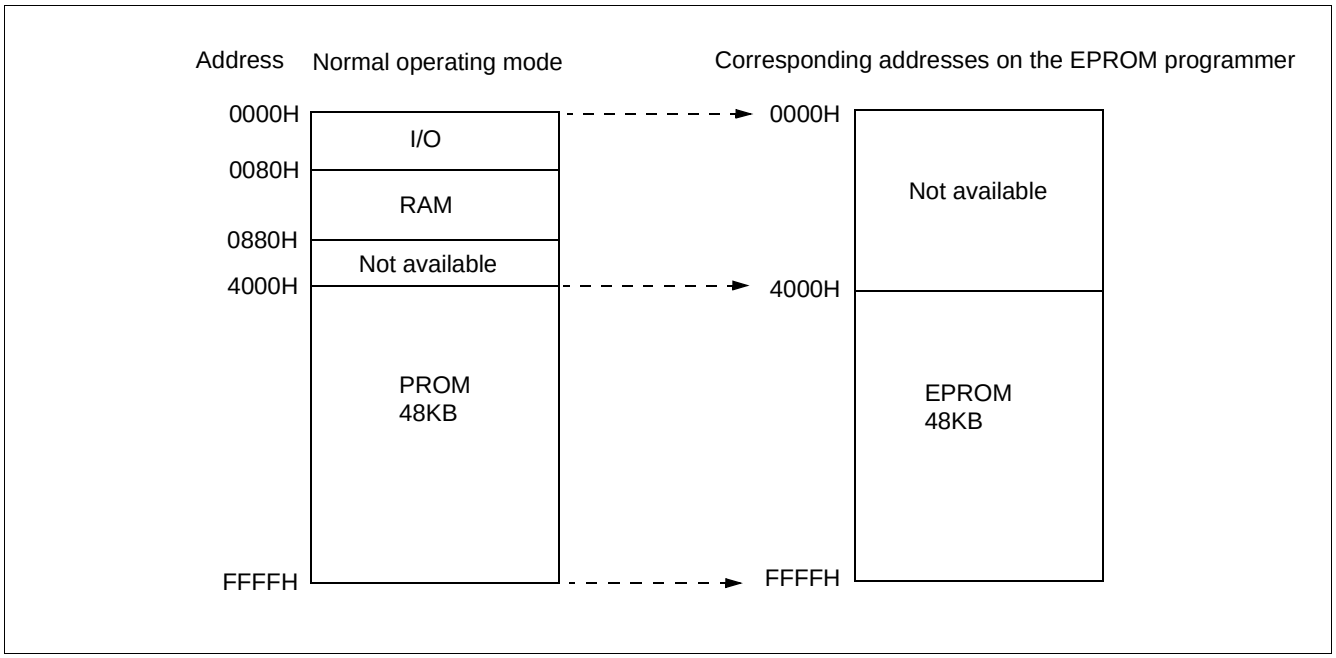
To program to the PROM using an EPROM programmer, use the socket adapter (manufacturer: Sun Hayato Co., Ltd.) listed below.

Package	Adapter socket part number
LCC-32 (Rectangle)	ROM-32LC-28DP-YG

Inquiry: Sun Hayato Co., Ltd.: TEL 81-3-3802-5760

3. Memory Space

Memory space in each mode is diagrammed below.



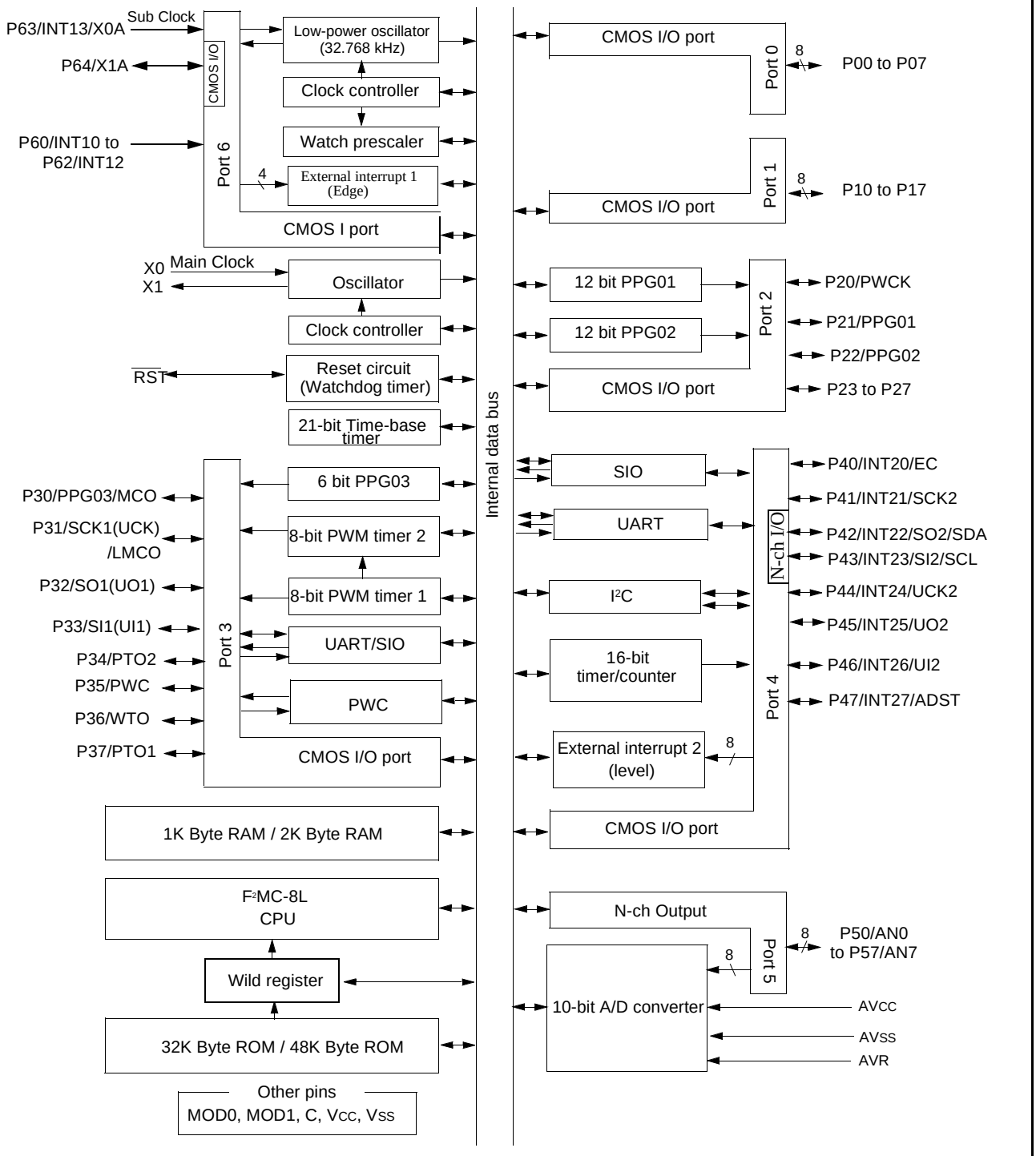
4. Programming to the EPROM

(1) Set the EPROM programmer to the MBM27C512.

(2) Load program data into the EPROM programmer at 4000_H to $FFFF_H$.

(3) Program to 4000_H to $FFFF_H$ with the EPROM programmer.

■ Block Diagram



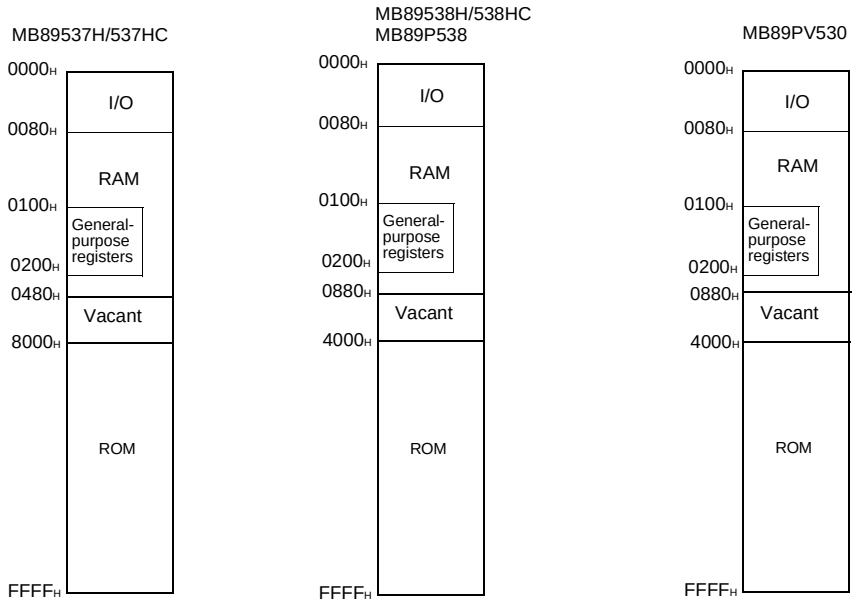
* I²C is not available in MB89537 and MB89538

■ CPU CORE

1. Memory Space

The microcontrollers of the MB89530 series offer a memory space of 64 Kbytes for storing all of I/O, data, and program areas. The I/O area is located the lowest address. The data area is provided immediately above the I/O area. The data area can be divided into register, stack, and direct areas according to the application. The program area is located at exactly the opposite end, that is, near the highest address. Provide the tables of interrupt reset vectors and vector call instructions toward the highest address within the program area. The memory space of the MB89530 series is structured as illustrated below.

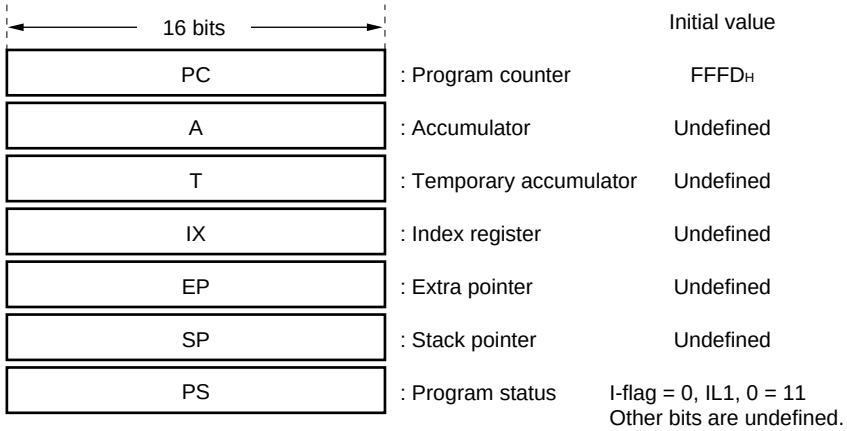
Memory Space



2. Registers

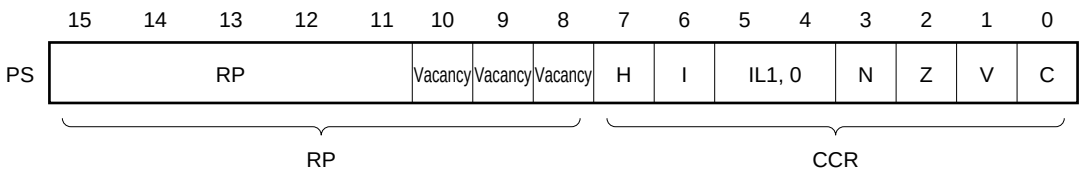
The F²MC-8L family has two types of registers; dedicated registers in the CPU and general-purpose registers in the memory. The following registers are provided:

Program counter (PC):	A 16-bit register for indicating specifies instruction storage positions.
Accumulator (A):	A 16-bit temporary register for storing arithmetic operations, etc. When the instruction is an 8-bit data processing instruction, the lower byte is used.
Temporary accumulator (T):	A 16-bit register which performs arithmetic operations with the accumulator When the instruction is an 8-bit data processing instruction, the lower byte is used.
Index register (IX):	A 16-bit register for index modification
Extra pointer (EP):	A 16-bit pointer for indicating a memory address
Stack pointer (SP):	A 16-bit register for indicating a stack area
Program status (PS):	A 16-bit register for storing a register pointer, a condition code



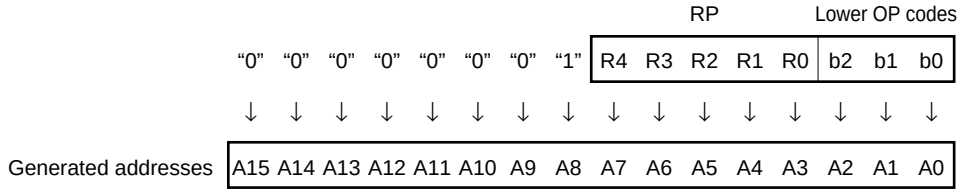
The PS can further be divided into higher 8 bits for use as a register bank pointer (RP) and the lower 8 bits for use as a condition code register (CCR). (See the diagram below.)

Structure of the Program Status Register



The RP indicates the address of the register bank currently in use. The relationship between the pointer contents and the actual address is based on the conversion rule illustrated below.

Rule for Conversion of Actual Addresses of the General-purpose Register Area



The CCR consists of bits indicating the results of arithmetic operations and the contents of transfer data and bits for control of CPU operations at the time of an interrupt.

H-flag: Set when a carry or a borrow from bit 3 to bit 4 occurs as a result of an arithmetic operation. Cleared otherwise. This flag is for decimal adjustment instructions.

I-flag: Interrupt is allowed when this flag is set to 1. Interrupt is prohibited when the flag is set to 0. Set to 0 when reset.

IL1, 0: Indicates the level of the interrupt currently allowed. Processes an interrupt only if its request level is higher than the value indicated by this bit.

IL1	IL0	Interrupt level	High-low
0	0	1	High
0	1		
1	0	2	
1	1	3	Low = no interrupt

N-flag: Set if the MSB is set to 1 as the result of an arithmetic operation. Cleared when the bit is set to 0.

Z-flag: Set when an arithmetic operation results in 0. Cleared otherwise.

V-flag: Set if the complement on 2 overflows as a result of an arithmetic operation. Reset if the overflow does not occur.

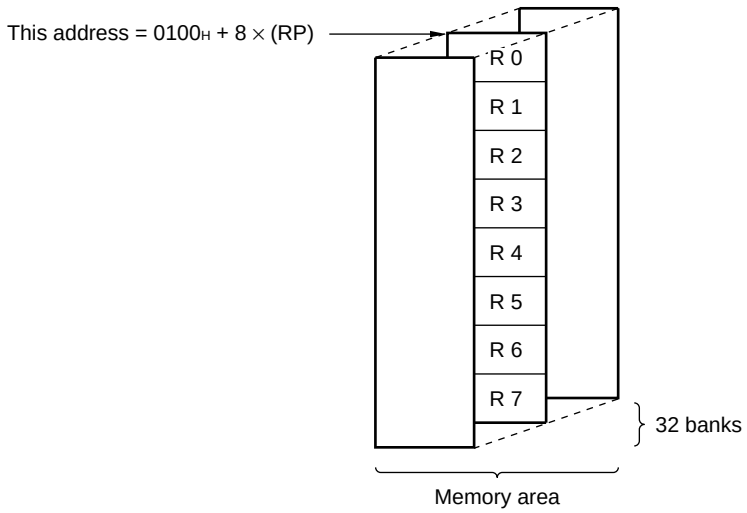
C-flag: Set when a carry or a borrow from bit 7 occurs as a result of an arithmetic operation. Cleared otherwise. Set to the shift-out value in the case of a shift instruction.

The following general-purpose registers are provided:

General-purpose registers: An 8-bit resister for storing data

The general-purpose registers are 8 bits and located in the register banks of the memory. One bank contains eight registers. Up to a total of 32 banks can be used on the MB89530 series. The bank currently in use is indicated by the register bank pointer (RP).

Register Bank Configuration



■ I/O MAP

Address	Register name	Register Description	Read/Write	Initial value
00_H	PDR0	Port 0 data register	R/W	$XXXXXXXX_B$
01_H	DDR0	Port 0 data direction register	W	00000000_B
02_H	PDR1	Port 1 data register	R/W	$XXXXXXXX_B$
03_H	DDR1	Port 1 data direction register	W	00000000_B
04_H - 06_H	(Vacancy)			
07_H	SYCC	System clock control register	R/W	$XX1MM100_B$
08_H	STBC	Standby control register	R/W	$00010XXX_B$
09_H	WDTC	Watchdog timer control register	R/W	$0XXXXXXX_B$
$0A_H$	TBTC	Timebase timer control register	R/W	$00XXX000_B$
$0B_H$	WPCR	Watch prescaler control register	R/W	$00XX0000_B$
$0C_H$	PDR2	Port 2 data register	R/W	$XXXXXXXX_B$
$0D_H$	DDR2	Port 2 data direction register	R/W	00000000_B
$0E_H$	PDR3	Port 3 data register	R/W	$XXXXXXXX_B$
$0F_H$	DDR3	Port 3 direction register	R/W	00000000_B
10_H	PDR4	Port 4 data register	R/W	$XXXXXXXX_B$
11_H	DDR4	Port 4 direction register	R/W	$0000XX00_B$
12_H	PDR5	Port 5 data register	R/W	11111111_B
13_H	PDR6	Port 6 data register	R/W	$XXXXXXXX_B$
14_H - 21_H	(Vacancy)			
22_H	SMC11	UART1 mode control register	R/W	00000000_B
23_H	SRC1	UART1 mode data register	R/W	$XX011000_B$
24_H	SSD1	UART1 status register	R/W	$00100X1X_B$
25_H	SIDR1/SODR1	UART1 data register	R/W	$XXXXXXXX_B$
26_H	SMC12	UART1 mode control register2	R/W	$XX100001_B$
27_H	CNTR1	PWM control register 1	R/W	00000000_B
28_H	CNTR2	PWM control register 2	R/W	$000X0000_B$
29_H	CNTR3	PWM control register 3	R/W	$X000XXXX_B$
$2A_H$	COMR1	PWM compare register 1	W	$XXXXXXXX_B$
$2B_H$	COMR2	PWM compare register 2	W	$XXXXXXXX_B$
$2C_H$	PCR1	PWC pulse width control register 1	R/W	$000XX000_B$
$2D_H$	PCR2	PWC pulse width control register 2	R/W	00000000_B
$2E_H$	RLBR	PWC reload buffer register	R/W	$XXXXXXXX_B$
$2F_H$	SMC21	UART/SIO mode control register 1	R/W	00000000_B
30_H	SMC22	UART/SIO mode control register 2	R/W	00000000_B
31_H	SSD2	UART/SIO status/data register	R/W	$00001XXX_B$
32_H	SSIDR2/SODR2	UART/SIO data register	R/W	$XXXXXXXX_B$
33_H	SRC2	UART/SIO rate control register	R/W	$XXXXXXXX_B$
34_H	ADC1	A/D control register 1	R/W	$X00000X0_B$
35_H	ADC2	A/D control register 2	R/W	$X0000001_B$

(Continued)

(Continued)

Address	Register name	Register Description	Read/Write	Initial value
36H	ADDL	A/D data register L	R/W	XXXXXXXXB
37H	ADDH	A/D data register H	R/W	XXXXXXXXB
38H	PPGC2	PPG2 control register (12-bit PPG)	R/W	00000000B
39H	PRL22	PPG2 reload register 2(12-bit PPG)	R/W	0X000000B
3AH	PRL21	PPG2 reload register 1(12-bit PPG)	R/W	XX000000B
3BH	PRL23	PPG2 reload register 3(12-bit PPG)	R/W	XX000000B
3CH	TMCR	16-bit Timer control register	R/W	XX100000B
3DH	TCHR	16-bit Timer high byte data register	R/W	00000000B
3EH	TCLR	16-bit Timer low byte data register	R/W	00000000B
3FH	EIC1	External interrupt 1 control register 1	R/W	00000000B
40H	EIC2	External interrupt 1 control register 2	R/W	00000000B
41H - 48H	(Vacancy)			
49H	DDCR	DDC selection register	R/W	XXXXXXX0B
4A-4BH	(Vacancy)			
4CH	PPGC1	PPG1 control register (12-bit PPG)	R/W	00000000
4DH	PRL12	PPG1 reload register2 (12-bit PPG)	R/W	0X000000
4EH	PRL11	PPG1 reload register1 (12-bit PPG)	R/W	XX000000
4FH	PRL13	PPG1 reload register3 (12-bit PPG)	R/W	XX000000
50H	IACR	I2C Slave address control register	R/W	XXXXX000B
51H	IBSR	I^2C bus status register	R	00000000B
52H	IBCR	I^2C bus control register	R/W	00000000B
53H	ICCR	I^2C clock control register	R/W	000XXXXXB
54H	IADR	I^2C address register	R/W	XXXXXXXXB
55H	IDAR	I^2C data register	R/W	XXXXXXXXB
56H	EIE2	External interrupt 2 enable register	R/W	00000000B
57H	EIF2	External interrupt 2 flag register	R/W	XXXXXXX0B
58H	RCR1	Remote control register 1(PPG03)6-bit	R/W	00000000B
59H	RCR2	Remote control register 2(PPG03)6-bit	R/W	0X000000B
5AH	CKR	Clock Output control register	R/W	XXXXXX00B
5BH - 6FH	(Vacancy)			
70H	SMR	Serial mode register(SIO)	R/W	00000000B
71H	SDR	Serial data register(SIO)	R/W	XXXXXXXXB
72H	PURR0	Pull-up resister register 0	R/W	11111111B
73H	PURR1	Pull-up resister register 1	R/W	11111111B
74H	PURR2	Pull-up resister register 2	R/W	11111111B
75H	PURR3	Pull-up resister register 3	R/W	11111111B
76H	PURR4	Pull-up resister register 4	R/W	1111XX11B
77H	WREN	Wild Register Enable register	R/W	XX000000B
78H	WROR	Wild Register Data register enable	R/W	XX000000B

(Continued)

(Continued)

Address	Register name	Register Description	Read/Write	Initial value
79H	PURR6	Pull-up resister register 6	R/W	XXX11111B
7AH	(Vacancy)			
7BH	ILR1	Interrupt level setting register 1	W	11111111B
7CH	ILR2	Interrupt level setting register 2	W	11111111B
7DH	ILR3	Interrupt level setting register 3	W	11111111B
7EH	ILR4	Interrupt level setting register 4	W	11111111B
7FH	ITR	Interrupt test register	Access prohibited	XXXXXX00B

■ Extend I/O Map

Address	Register name	Register description	Read/Write	Initial value
C80H	WRARH1	Wild register high-byte address register1	R/W	XXXXXXXXB
C81H	WRARL1	Wild register low-byte address register1	R/W	XXXXXXXXB
C82H	WRDR1	Wild register data register1	R/W	XXXXXXXXB
C83H	WRARH2	Wild register high-byte address register2	R/W	XXXXXXXXB
C84H	WRARL2	Wild register low-byte address register2	R/W	XXXXXXXXB
C85H	WRDR2	Wild register data register2	R/W	XXXXXXXXB
C86H	WRARH3	Wild register high-byte address register3	R/W	XXXXXXXXB
C87H	WRARL3	Wild register low-byte address register3	R/W	XXXXXXXXB
C88H	WRDR3	Wild register data register3	R/W	XXXXXXXXB
C89H	WRARH4	Wild register high-byte address register4	R/W	XXXXXXXXB
C8AH	WRARL4	Wild register low-byte address register4	R/W	XXXXXXXXB
C8BH	WRDR4	Wild register data register4	R/W	XXXXXXXXB
C8CH	WRARH5	Wild register high-byte address register5	R/W	XXXXXXXXB
C8DH	WRARL5	Wild register low-byte address register5	R/W	XXXXXXXXB
C8EH	WRDR5	Wild register data register5	R/W	XXXXXXXXB
C8FH	WRARH6	Wild register high-byte address register6	R/W	XXXXXXXXB
C90H	WRARL6	Wild register low-byte address register6	R/W	XXXXXXXXB
C91H	WRDR6	Wild register data register6	R/W	XXXXXXXXB

● **Read/write access symbols**

R/W : Readable and writable
R : Read-only
W : Write-only

● **Initial value symbols**

0: The initial value of this bit is “0”.
1: The initial value of this bit is “1”.
X: The initial value of this bit is undefined.
M: The initial value of this bit is determined by mask option.

Note: Do not use vacancies.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

(AV_{SS} = V_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC} AV_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	*MB89537H/537HC/538H/ 538HC/MB89P538
	AVR	V_{SS} – 0.3	V_{SS} + 6.0	V	
Program voltage	V_{PP}	V_{SS} – 0.6	V_{SS} + 13.0	V	Only for the MB89P538
Input voltage	V_I	V_{SS} – 0.3	V_{CC} + 0.3	V	For pins other than P42 and P43
			V_{SS} + 6.0	V	For P42 and P43
Output voltage	V_O	V_{SS} – 0.3	V_{CC} + 0.3	V	For pins other than P42 and P43
			V_{SS} + 6.0		For P42 and P43
“L” level maximum output current	I_{OL}	—	15	mA	
“L” level average output current	I_{OLAV}	—	4	mA	Average value (operating current × operating rate)
“L” level total maximum output current	$\sum I_{OL}$	—	100	mA	
“L” level total average output current	$\sum I_{OLAV}$	—	40	mA	Average value (operating current × operating rate)
“H” level maximum output current	I_{OH}	—	–15	mA	
“H” level average output current	I_{OHAV}	—	–4	mA	Average value (operating current × operating rate)
“H” level total maximum output current	$\sum I_{OH}$	—	–50	mA	
“H” level total average output current	$\sum I_{OHAV}$	—	–20	mA	Average value (operating current × operating rate)
Power consumption	P_D	—	300	mW	
Operating temperature	T_A	–40	+85	°C	
Storage temperature	Tstg	–55	+150	°C	

* : Use AV_{CC} and V_{CC} set at the same voltage.
Take care so that AV_{CC} does not exceed V_{CC}, such as when power is turned on.

Precautions: Permanent device damage may occur if the above “Absolute Maximum Ratings” are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. Recommended Operating Conditions

(AV_{SS} = V_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks	
		Min.	Max.			
Power supply voltage	V_{CC} AV_{CC}	3.5*	5.5	V	Operation assurance range	MB89537H/ 537HC/538H/ 538HC
		3.0	5.5	V	Retains the RAM state in stop mode	
		2.7*	5.5	V	Operation assurance range	MB89P538
		1.5	5.5	V	Retains the RAM state in stop mode	
	AVR	3.5	AV_{CC}	V		
Operating temperature	T_A	–40	+85	°C		

* : These values depend on the operating conditions and the analog assurance range. See Figure 1 and "5. A/D Converter Electrical Characteristics."

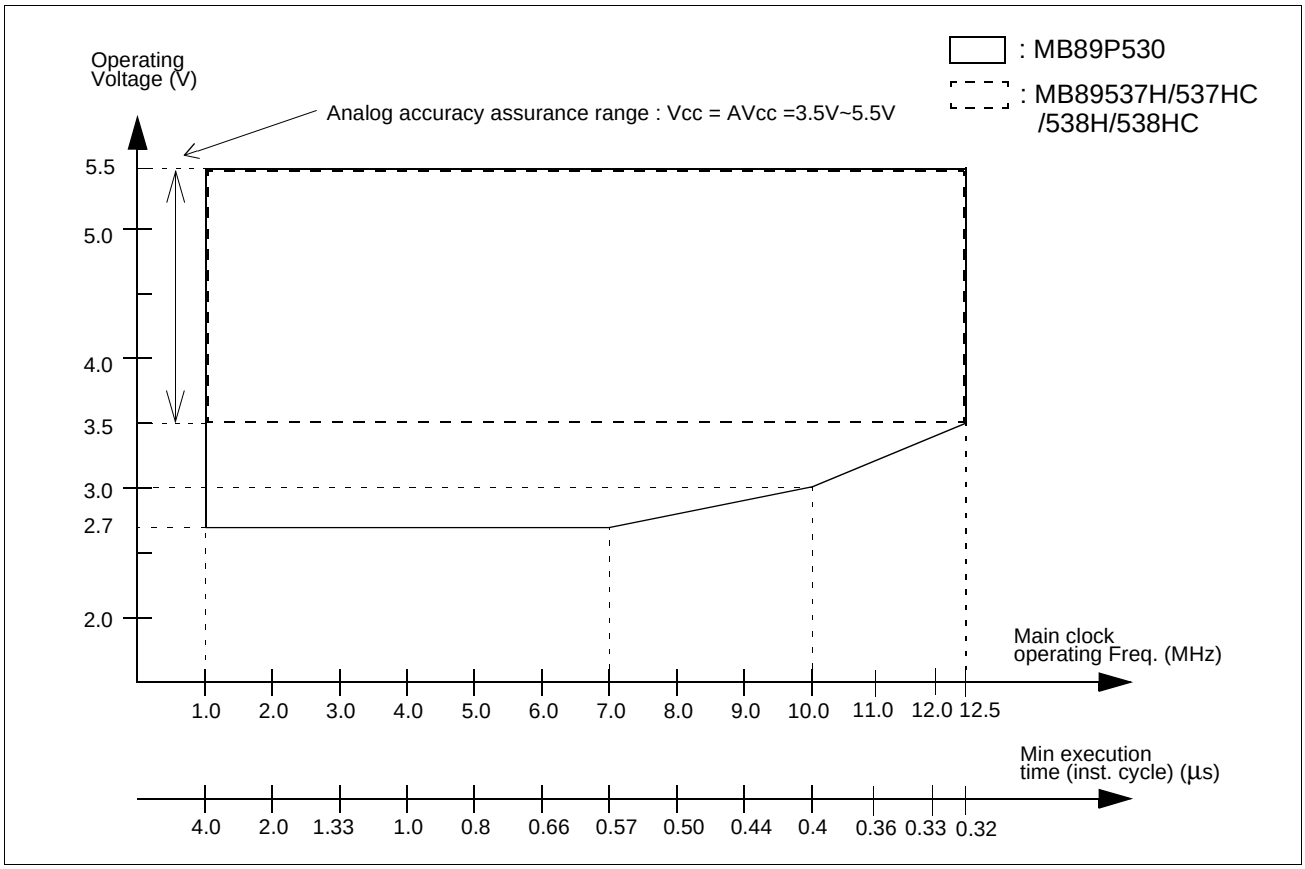


Figure 1 Operating Voltage vs. Main Clock Operating Frequency (MB89P538)

Figure 1 indicate the operating frequency of the external oscillator at an instruction cycle of 4/F_{CH}.

Since the operating voltage range is dependent on the instruction cycle, see minimum execution time if the operating speed is switched using a gear.

3. DC Characteristics

($AV_{CC} = V_{CC} = 5.0$ V, $AV_{SS} = V_{SS} = 0.0$ V, $T_A = -40°C$ to $+85°C$)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
"H" level input voltage	V_{IH}	P00 ~ P07, P10 ~ P17, P20 ~ P27 P30 ~ P37 P40 ~ P47 P60 ~ P62, SI1,SI2	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	
	V_{IHS}	$\overline{RST}$, MOD0, MOD1, INT20~INT27,UCK1,UI 1, INT10 ~ INT12, SCK1,EC,PWCK, PWC,SCK2, UCK2,UI2,ADST	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	
	V_{IHSMB}	SCL,SDA	—	V_{SS} +1.4	—	V_{SS} + 5.5	V	SMB input buffer selected
	V_{IHI2C}		—	0.7 V_{CC}	—	V_{SS} + 5.5	V	I2C input buffer selected
"L" level input voltage	V_{IL}	P00 ~ P07, P10 ~ P17, P20 ~ P27 P30 ~ P37 P40 ~ P47 P60 ~ P62, SI1, SI2	—	V_{SS} – 0.3	—	0.3 V_{CC}	V	
	V_{ILS}	$\overline{RST}$, MOD0, MOD1, INT20~INT27,UCK1,UI 1, INT10 ~ INT12, SCK1,EC,PWCK, PWC,SCK2, UCK2,UI2,ADST	—	V_{SS} – 0.3	—	0.2 V_{CC}	V	
	V_{ILSMB}	SCL,SDA	—	V_{SS} - 0.3	—	V_{SS} + 0.6	V	SMB input buffer selected
	V_{ILI2C}		—	V_{SS} – 0.3	—	0.3 V_{CC}	V	I2C input buffer selected
Open-drain output pin application voltage	V_{D1}	P50 ~ P57	—	V_{SS} – 0.3	—	V_{CC} + 0.3	V	
	V_{D2}	P42, P43				V_{SS} + 5.5	V	
"H" level output voltage	V_{OH}	P00 ~ P07, P10 ~ P17, P20 ~ P24, P30 ~ P37, P40,P41,P44 ~ P47	$I_{OH} = -2.0$mA	4.0	—	—	V	
		P25 ~ P27	$I_{OH} = -3$mA					

(Continued)

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(AV_{CC} = V_{CC} = 5.0 V, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
"L" level output voltage	V_{OL}	P00 ~ P07, P10 ~ P17, P20 ~ P24, P30 ~ P37, P40 ~ P47, $\overline{RST}$	I_{OL} = 4.0 mA	—	—	0.4	V	
Input leakage current	I_{LI}	P00 ~ P07, P10 ~ P17, P20 ~ P27, P30 ~ P37, P40 ~ P47, P50 ~ P57, P60 ~ P62	0.0 V < V_I < V_{CC}	-5	—	+5	µA	Without pull-up Resister
Open drain output leakage current	I_{LIOD}	P42, P43	0.0 V < V_I < V_{SS} + 5.5V	—	—	+5	µA	
Pull-up resistance	R_{PULL}	P00 ~ P07, P10 ~ P17, P20 ~ P27, P30 ~ P37, P40,P41,P44 ~ P47, P60 ~ P62, $\overline{RST}$	V_I = 0.0 V	25	50	100	kΩ	When pull-up resistor selected except $\overline{RST}$
Power supply current	I_{CC1}	V_{CC}	F_{CH} = 10.0MHz t_{inst}*2 = 0.4 µs	—	15	20	mA	main clock run mode MB89P538
				—	6	10	mA	main clock run mode MB89537H/ 537HC/538H/ 538HC
	I_{CC2}		F_{CH} = 10.0MHz t_{inst}*2 = 6.4 µs	—	5	8.5	mA	main clock run mode MB89P538
				—	1.5	3	mA	main clock run mode MB89537H/ 537HC/538H/ 538HC
	I_{CCS1}		F_{CH} = 10.0MHz t_{inst}*2 = 0.4 µs	—	5	7	mA	sleep mode MB89P538
				—	2	4	mA	sleep mode MB89537H/ 537HC/538H/ 538HC
	I_{CCS2}		F_{CH} = 10.0MHz t_{inst}*2 = 6.4 µs		1.5	3	mA	sleep mode MB89P538
					1	2	mA	sleep mode MB89537H/ 537HC/538H/ 538HC

(Continued)

(Continued)

(AV_{CC} = V_{CC} = 5.0 V, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Power supply current	I_{CCL}	V_{CC}	F_{CL} = 32.768 kHz	—	3	7	mA	sub clock mode MB89P538
					20	50	µA	sub-clock mode MB89537H/ 537HC/538H/ 538HC
	I_{CCLS}		F_{CL} = 32.768 kHz	—	30	50	µA	sub-cock sleep mode MB89P538
				—	15	30	µA	sub-cock sleep mode MB89537H/ 537HC/538H/ 538HC
	I_{CCT}		F_{CL} = 32.768 kHz	—	5	15	µA	Watch mode main stop
	I_{CCH}		Ta=+25°C	—	3	10	µA	stop mode
	I_A	AV_{cc}	F_{CH}=10MHz	—	4	6	mA	A/D converting
	I_{AH}		Ta=+25°C	—	1	5	µA	A/D stop
Input capacitance	C_{IN}	not include V_{CC},V_{SS},AV_{CC},AV_{SS}	f=1MHz	—	10	—	pF	

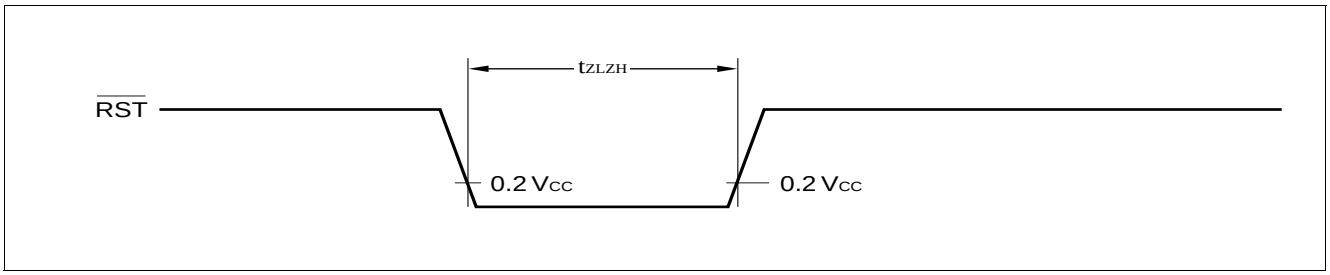
4. AC Characteristics

(1) Reset Timing

(V_{CC} = 5.0V, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
$\overline{RST}$ "L" pulse width	t_{ZLZH}	—	48 t_{HCYL}*	—	ns	

* : t_{HCYL} is the oscillation cycle (1/F_C) to input to the X0 pin.

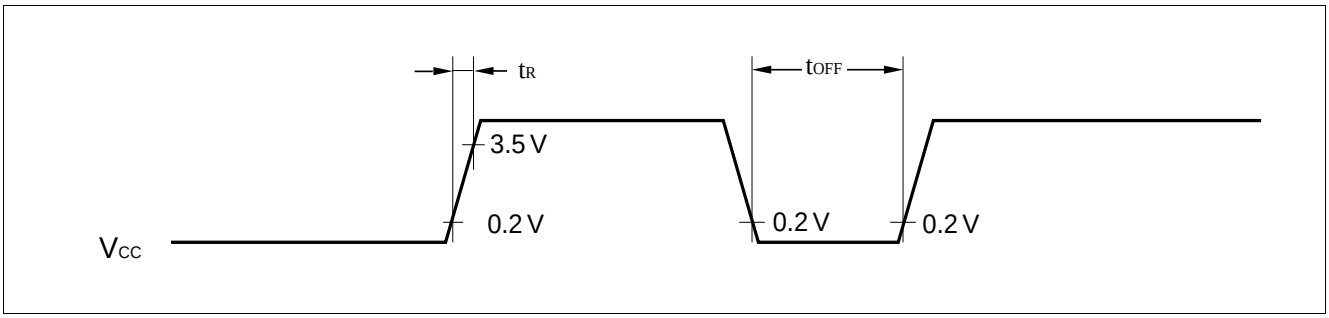


(2) Power-on Reset

(AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
Power supply rising time	t_R	—	0.5	50	ms	
Power supply cut-off time	t_{OFF}		1	—	ms	Due to repeated operations

Note: Make sure that power supply rises within the selected oscillation stabilization time.
For example, when the main clock is operating at 3 MHz (F_{CH}) and the oscillation stabilization time select option has been set to $2^{12}/F_{CH}$, the oscillation stabilization delay time is 1.4 ms. Therefore, the maximum value of power supply rising time is about 1.4 ms.
Rapid changes in power supply voltage may cause a power-on reset. If power supply voltage needs to be varied in the course of operation, a smooth voltage rise is recommended.

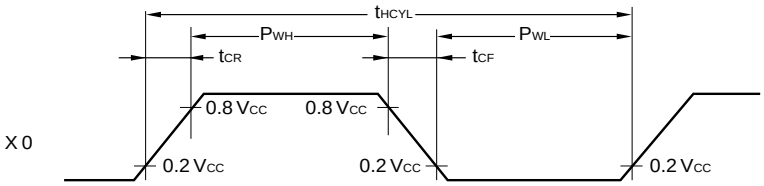


(3) Clock Timing

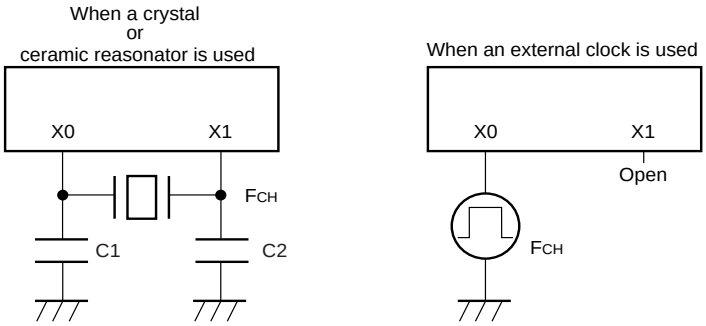
(V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min.	Typ.	Max.		
Clock frequency	F_{CH}	X0, X1	1	—	12.5	MHz	Main clock
	F_{CL}	X0A, X1A	—	32.768	—	kHz	Subclock
Clock cycle time	t_{HCYL}	X0, X1	80	—	1000	ns	Main clock
	t_{LCYL}	X0A, X1A	—	30.5	—	µs	Subclock
Input clock pulse width	P_{WH} P_{WL}	X0	20	—	—	ns	External clock
	P_{WHH} P_{WLL}	X0A	—	15.2	—	µs	External clock
Input clock rising/falling time	t_{CR} t_{CF}	X0	—	—	10	ns	External clock

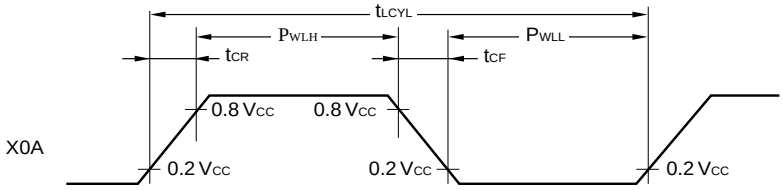
X0 and X1 Timing and Conditions



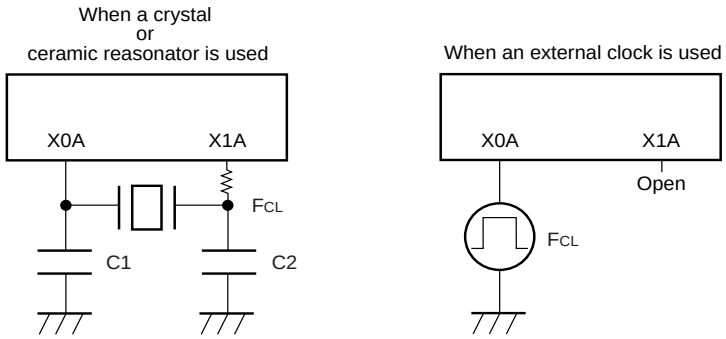
Main Clock Conditions



X0A and X1A Timing and Conditions



Subclock Conditions



(4) Instruction Cycle

(AVss=V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Value	Unit	Remarks
Instruction cycle (minimum execution time)	t_{inst}	$4/F_{CH}$, $8/F_{CH}$, $16/F_{CH}$, $64/F_{CH}$	µs	$(4/F_{CH})t_{inst}$ = 0.32 µs when operating at F_{CH} = 12.5 MHz
		$2/F_{CL}$	µs	t_{inst} = 61.036 µs when operating at F_{CL} = 32.768 kHz

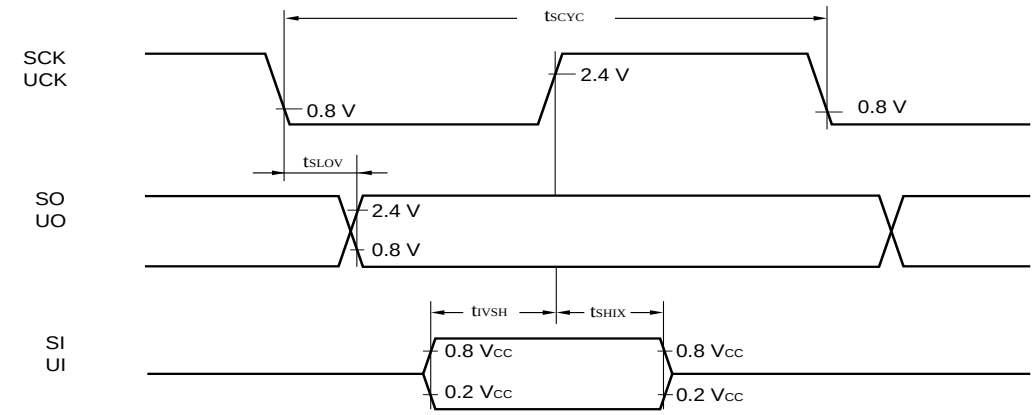
(5) Serial I/O Timing

(V_{CC} = 5.0 V, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

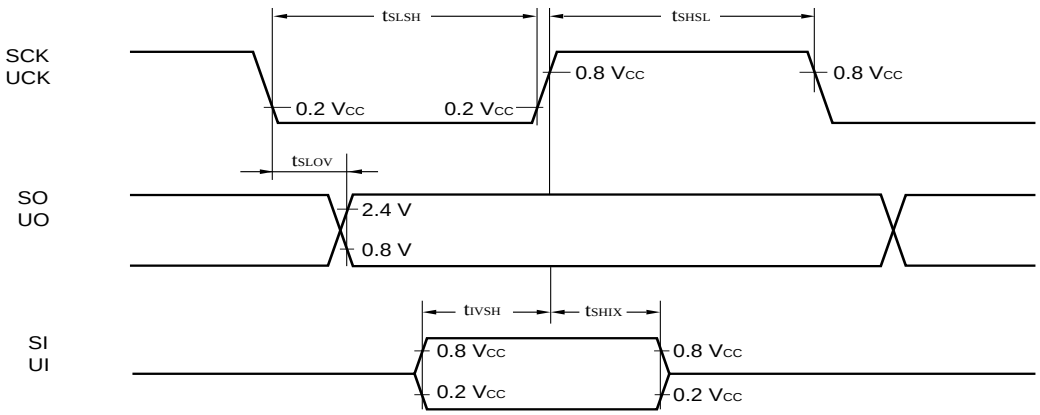
Parameter	Symbol	Pin	Condition	Value		Unit
				Min.	Max.	
Serial clock cycle time	t_{SCYC}	SCK,UCK	Internal shift clock mode	2 t_{inst}*	—	µs
SCK ↓ → SO time	t_{SLOV}	SCK, SO, UCK, UO		–200	200	ns
Valid SI → SCK	t_{IVSH}	SI, SCK, UI, UCK		200	—	ns
SCK ↑ → valid SI hold time	t_{SHIX}	SCK, SI, UCK, UI		200	—	ns
Serial clock “H” pulse width	t_{SHSL}	SCK, UCK	External shift clock mode	1 t_{inst}*	—	µs
Serial clock “L” pulse width	t_{SLSH}			1 t_{inst}*	—	µs
SCK ↓ → SO time	t_{SLOV}	SCK, SO, UCK, UO		0	200	ns
Valid SI → SCK ↑	t_{IVSH}	SI, SCK, UI, UCK		200	—	ns
SCK ↑ → valid SI hold time	t_{SHIX}	SCK, SI, UCK UI		200	—	ns

* : For information on t_{inst}, see “(4) Instruction Cycle.”

Internal Shift Clock Mode



External Shift Clock Mode

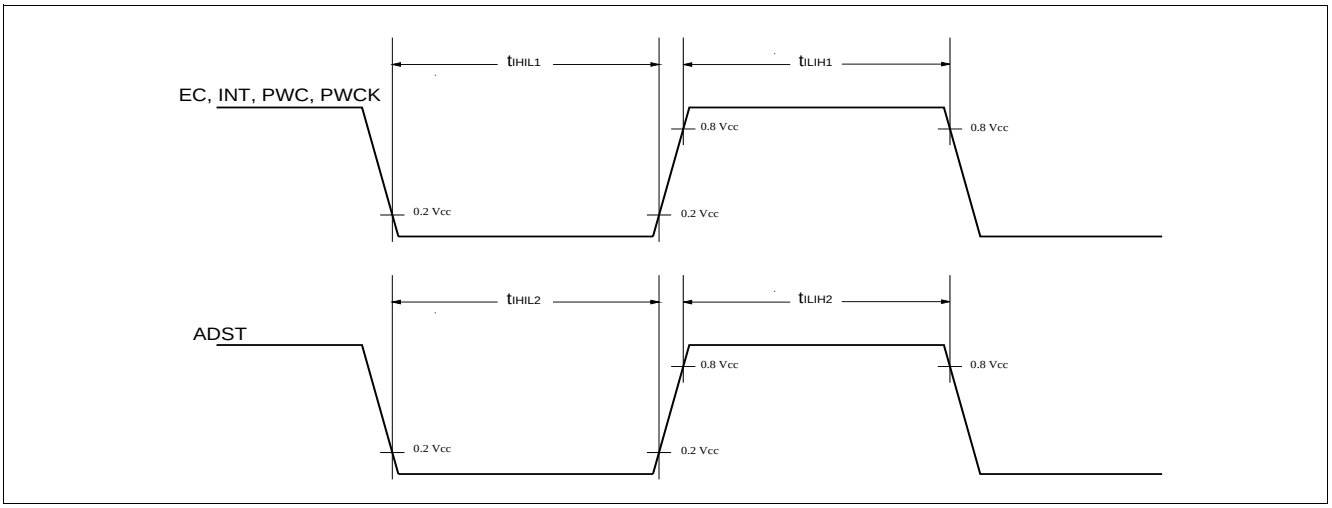


(6) Peripheral Input Timing

(V_{CC} = 5.0 V, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Value		Unit	Remarks
			Min.	Max.		
Peripheral input “H” pulse width 1	t_{ILIH1}	INT10 toINT27, EC, PWC, PWCK	2 t_{inst}*	—	µs	
Peripheral input “L” pulse width 1	t_{IHIL1}		2 t_{inst}*	—	µs	
Peripheral input “H” pulse width 2	t_{ILIH2}	ADST	2^8 t_{inst}*	—	µs	
Peripheral input “L” pulse width 2	t_{IHIL2}		2^8 t_{inst}*	—	µs	

* : For information on t_{inst}, see “(4) Instruction Cycle.”

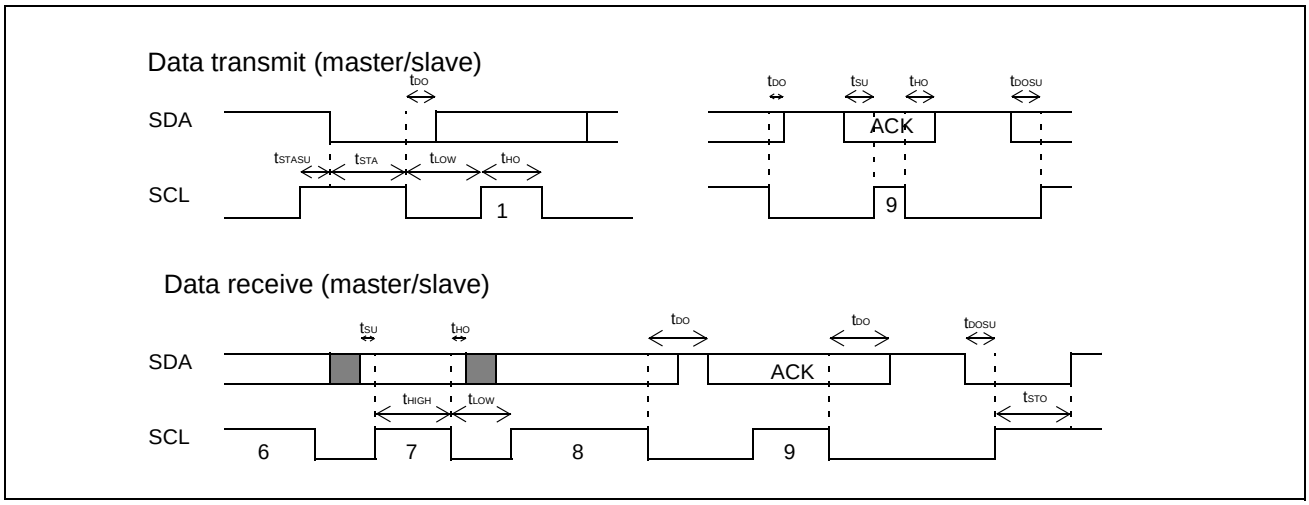


(7) I²C timing

(V_{CC} = 5.0 V, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min.	Max.		
Start condition output	t_{STA}	SCL SDA		1/4t_{INST} x m x n - 20	1/4t_{INST} x m x n + 20	ns	master mode
Stop condition output	t_{STO}	SCL SDA		1/4t_{INST} x (m x n + 8) - 20	1/4t_{INST} x (m x n + 8) + 20	ns	master mode
Start condition detect	t_{STA}	SCL SDA		1/4t_{INST} x 6 + 40	—	ns	
Stop condition detect	t_{STO}	SCL SDA		1/4t_{INST} x 6 + 40	—	ns	
Re-start condition output	t_{STASU}	SCL SDA		1/4t_{INST} x (m x n + 8) - 20	1/4t_{INST} x (m x n + 8) + 20	ns	master mode
Re-start condition detect	t_{STASU}	SCL SDA		1/4t_{INST} x 4 + 40	—	ns	
SCL output LOW width	t_{LOW}	SCL		1/4t_{INST} x m x n - 20	1/4t_{INST} x m x n + 20	ns	master mode
SCL output HIGHT width	t_{HIGH}	SCL		1/4t_{INST} x (m x n + 8) - 20	1/4t_{INST} x (m x n + 8) + 20	ns	master mode
SDA output delay	t_{DO}	SDA		1/4t_{INST} x 4 - 20	1/4t_{INST} x 4 + 20	ns	
SDA output setup time after interrupt	t_{DOSU}	SDA		1/4t_{INST} x 4 - 20	—	ns	
SCL input LOW pulse width	t_{LOW}	SCL		1/4t_{INST} x 6 + 40	—	ns	
SCL input HIGH pulse width	t_{HIGH}	SCL		1/4 t_{INST} x 2 + 40	—	ns	
SDA input setup time	t_{SU}	SDA		40	—	ns	
SDA hold time	t_{HO}	SDA		0	—	ns	

- For information in t_{INST}, see "(4) Instruction Cycle".
- m is defined in the ICCR CS3 and CS3 (bit 4 to bit 3)
- n is defined in the ICCR CS2 to CS0 (bit 2 to bit 0)
- t_{DOSU} shows that interrupt period is under than "L" width
- The specification of SDA, SCL output is on the assumption that rising time is 0 ns..



5. A/D Converter Electrical Characteristics

(1) MB89537H/637HC/538H/538HC A/D Converter Electrical Characteristics

(V_{CC} = 3.5 V ~ 5.5 V, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min.	Typ.	Max.		
Resolution	—	—	—	—	10	bit	At AV_{CC} = V_{CC}
Total error			—	—	±5.0	LSB	
Linearity error			—	—	±2.5	LSB	
Differential linearity error			—	—	±1.9	LSB	
Zero transition voltage	V_{OT}	—	AV_{SS} – 3.5 LSB	AV_{SS} + 0.5 LSB	AV_{SS} + 4.5 LSB	mV	
Full-scale transition voltage	V_{FST}		AVR – 6.5 LSB	AVR – 1.5 LSB	AVR + 1.5 LSB	mV	
Interchannel disparity	—		—	—	4	LSB	
A/D mode conversion time			—	60 tinst	—	µs	*
Sampling time			—	16 tinst	—	µs	
Analog port input current	I_{AIN}	AN0 to AN7	—	—	10	µA	
Analog input voltage	V_{AIN}		AV_{SS}	—	AVR	V	
Reference voltage	—	AVR	AV_{SS} + 3.5	—	AV_{CC}	V	
Reference voltage supply current	I_R		—	400	—	µA	At A/D start
	I_{RH}		—	—	5	µA	At A/D stop

* : Sampling time included

(2) MB89P538 A/D Converter Electrical Characteristics

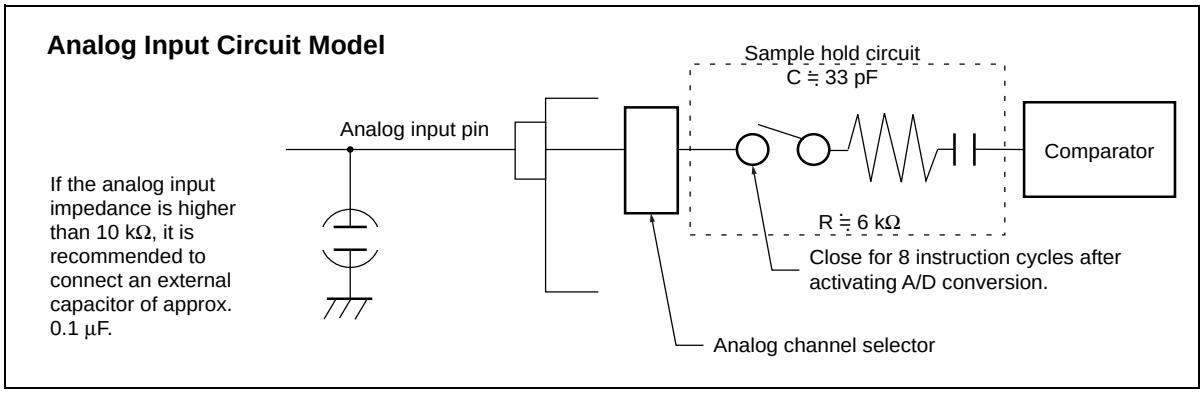
(V_{CC} = 3.5 V ~ 5.5 V, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min.	Typ.	Max.		
Resolution	—	—	—	—	10	bit	At AV_{CC} = V_{CC}
Total error			—	—	±3.0	LSB	
Linearity error			—	—	±2.5	LSB	
Differential linearity error			—	—	±1.9	LSB	
Zero transition voltage	V_{OT}	—	AV_{SS} – 1.5 LSB	AV_{SS} + 0.5 LSB	AV_{SS} + 2.5 LSB	mV	
Full-scale transition voltage	V_{FST}		AVR – 3.5 LSB	AVR – 1.5 LSB	AVR + 1.5 LSB	mV	
Interchannel disparity	—		—	—	4	LSB	
A/D mode conversion time			—	60 tinst	—	µs	*
Sampling time			—	16 tinst	—	µs	
Analog port input current	I_{AIN}	AN0 to AN7	—	—	10	µA	
Analog input voltage	V_{AIN}		0	—	AVR	V	
Reference voltage	—	AVR	AV_{SS} + 3.5	—	AV_{CC}	V	
Reference voltage supply current	I_R		—	400	—	µA	At A/D start
	I_{RH}		—	—	5	µA	At A/D stop

* : Sampling time included

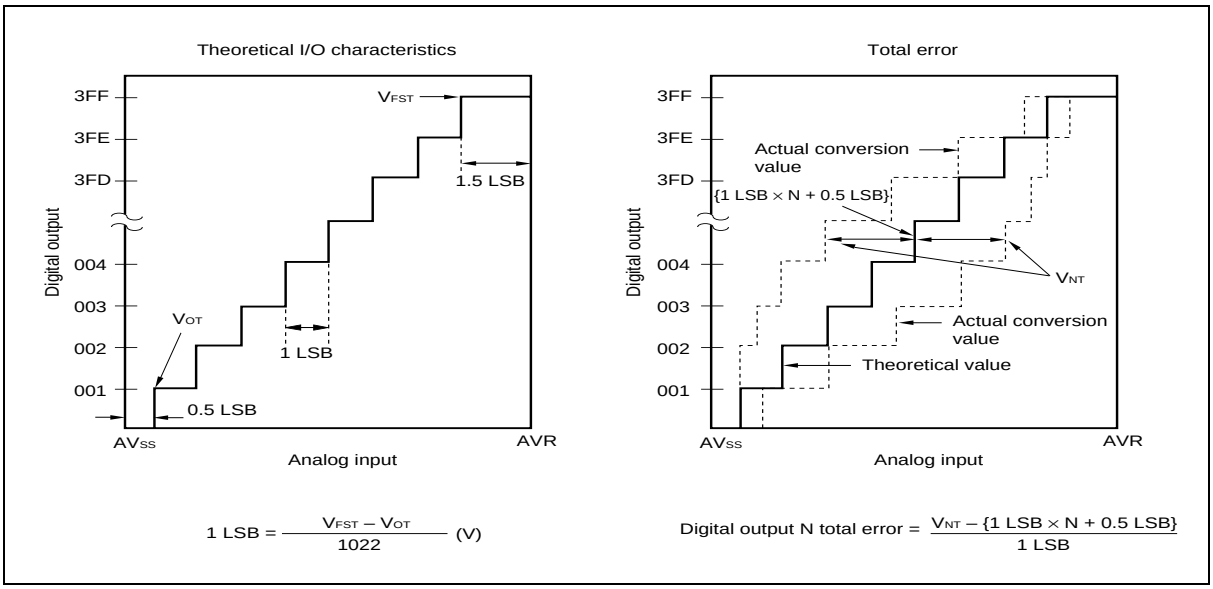
(3) Precautions

- The smaller the | AVR–AVSS |, the greater the error would become relatively.
- The output impedance of the external circuit for the analog input must satisfy the following conditions:
  Output impedance of the external circuit < Approx. 10 kΩ
- If the output impedance of the external circuit is too high, an analog voltage sampling time might be insufficient (sampling time = 6 µs at 10MHz oscillation.)



(4) A/D Converter Glossary

- Resolution
  Analog changes that are identifiable with the A/D converter.
- Linearity error
  The deviation of the straight line connecting the zero transition point (“00 0000 0000” ↔ “00 0000 0001”) with the full-scale transition point (“11 1111 1110” ↔ “11 1111 1111”) from actual conversion characteristics
- Differential linearity error
  The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value
- Total error (unit: LSB)
  The difference between theoretical and actual conversion values caused by the zero transition error, full-scale transition error, linearity error, quantization error, and noise



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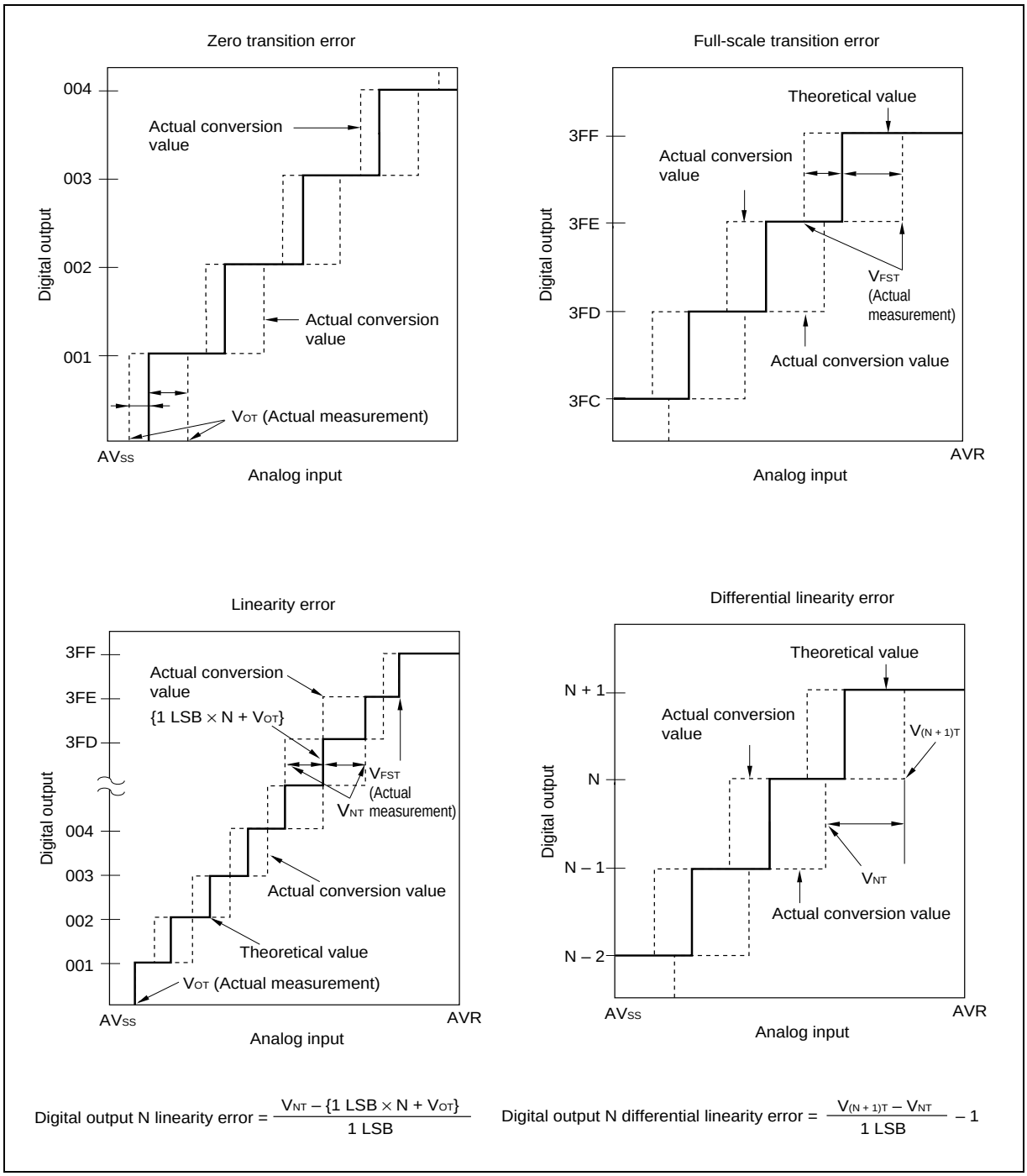


$$\text{Digital output N linearity error} = \frac{V_{NT} - \{1\ \text{LSB} \times N + V_{OT}\}}{1\ \text{LSB}}$$

$$\text{Digital output N differential linearity error} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1$$

■ INSTRUCTIONS

Execution instructions can be divided into the following four groups:

- Transfer
- Arithmetic operation
- Branch
- Others

Table 1 lists symbols used for notation of instructions.

Table 1 Instruction Symbols

Symbol	Meaning
dir	Direct address (8 bits)
off	Offset (8 bits)
ext	Extended address (16 bits)
#vct	Vector table number (3 bits)
#d8	Immediate data (8 bits)
#d16	Immediate data (16 bits)
dir: b	Bit direct address (8:3 bits)
rel	Branch relative address (8 bits)
@	Register indirect (Example: @A, @IX, @EP)
A	Accumulator A (Whether its length is 8 or 16 bits is determined by the instruction in use.)
AH	Upper 8 bits of accumulator A (8 bits)
AL	Lower 8 bits of accumulator A (8 bits)
T	Temporary accumulator T (Whether its length is 8 or 16 bits is determined by the instruction in use.)
TH	Upper 8 bits of temporary accumulator T (8 bits)
TL	Lower 8 bits of temporary accumulator T (8 bits)
IX	Index register IX (16 bits)

(Continued)

(Continued)

Symbol	Meaning
EP	Extra pointer EP (16 bits)
PC	Program counter PC (16 bits)
SP	Stack pointer SP (16 bits)
PS	Program status PS (16 bits)
dr	Accumulator A or index register IX (16 bits)
CCR	Condition code register CCR (8 bits)
RP	Register bank pointer RP (5 bits)
Ri	General-purpose register Ri (8 bits, i = 0 to 7)
×	Indicates that the very × is the immediate data. (Whether its length is 8 or 16 bits is determined by the instruction in use.)
(×)	Indicates that the contents of × is the target of accessing. (Whether its length is 8 or 16 bits is determined by the instruction in use.)
((×))	The address indicated by the contents of × is the target of accessing. (Whether its length is 8 or 16 bits is determined by the instruction in use.)

Columns indicate the following:

Mnemonic: Assembler notation of an instruction

~: Number of instructions

#: Number of bytes

Operation: Operation of an instruction

TL, TH, AH: A content change when each of the TL, TH, and AH instructions is executed. Symbols in the column indicate the following:

- "–" indicates no change.
- dH is the 8 upper bits of operation description data.
- AL and AH must become the contents of AL and AH immediately before the instruction is executed.
- 00 becomes 00.

N, Z, V, C: An instruction of which the corresponding flag will change. If + is written in this column, the relevant instruction will change its corresponding flag.

OP code: Code of an instruction. If an instruction is more than one code, it is written according to the following rule:

Example: 48 to 4F ← This indicates 48, 49, ... 4F.

Table 2 Transfer Instructions (48 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
MOV dir,A	3	2	(dir) ← (A)	–	–	–	– – – –	45
MOV @IX +off,A	4	2	((IX) +off) ← (A)	–	–	–	– – – –	46
MOV ext,A	4	3	(ext) ← (A)	–	–	–	– – – –	61
MOV @EP,A	3	1	((EP)) ← (A)	–	–	–	– – – –	47
MOV Ri,A	3	1	(Ri) ← (A)	–	–	–	– – – –	48 to 4F
MOV A,#d8	2	2	(A) ← d8	AL	–	–	+ + – –	04
MOV A,dir	3	2	(A) ← (dir)	AL	–	–	+ + – –	05
MOV A,@IX +off	4	2	(A) ← ((IX) +off)	AL	–	–	+ + – –	06
MOV A,ext	4	3	(A) ← (ext)	AL	–	–	+ + – –	60
MOV A,@A	3	1	(A) ← ((A))	AL	–	–	+ + – –	92
MOV A,@EP	3	1	(A) ← ((EP))	AL	–	–	+ + – –	07
MOV A,Ri	3	1	(A) ← (Ri)	AL	–	–	+ + – –	08 to 0F
MOV dir,#d8	4	3	(dir) ← d8	–	–	–	– – – –	85
MOV @IX +off,#d8	5	3	((IX) +off) ← d8	–	–	–	– – – –	86
MOV @EP,#d8	4	2	((EP)) ← d8	–	–	–	– – – –	87
MOV Ri,#d8	4	2	(Ri) ← d8	–	–	–	– – – –	88 to 8F
MOVW dir,A	4	2	(dir) ← (AH),(dir + 1) ← (AL)	–	–	–	– – – –	D5
MOVW @IX +off,A	5	2	((IX) +off) ← (AH), ((IX) +off + 1) ← (AL)	–	–	–	– – – –	D6
MOVW ext,A	5	3	(ext) ← (AH), (ext + 1) ← (AL)	–	–	–	– – – –	D4
MOVW @EP,A	4	1	((EP)) ← (AH),((EP) + 1) ← (AL)	–	–	–	– – – –	D7
MOVW EP,A	2	1	(EP) ← (A)	–	–	–	– – – –	E3
MOVW A,#d16	3	3	(A) ← d16	AL	AH	dH	+ + – –	E4
MOVW A,dir	4	2	(AH) ← (dir), (AL) ← (dir + 1)	AL	AH	dH	+ + – –	C5
MOVW A,@IX +off	5	2	(AH) ← ((IX) +off), (AL) ← ((IX) +off + 1)	AL	AH	dH	+ + – –	C6
MOVW A,ext	5	3	(AH) ← (ext), (AL) ← (ext + 1)	AL	AH	dH	+ + – –	C4
MOVW A,@A	4	1	(AH) ← ((A)), (AL) ← ((A)) + 1)	AL	AH	dH	+ + – –	93
MOVW A,@EP	4	1	(AH) ← ((EP)), (AL) ← ((EP) + 1)	AL	AH	dH	+ + – –	C7
MOVW A,EP	2	1	(A) ← (EP)	–	–	dH	– – – –	F3
MOVW EP,#d16	3	3	(EP) ← d16	–	–	–	– – – –	E7
MOVW IX,A	2	1	(IX) ← (A)	–	–	–	– – – –	E2
MOVW A,IX	2	1	(A) ← (IX)	–	–	dH	– – – –	F2
MOVW SP,A	2	1	(SP) ← (A)	–	–	–	– – – –	E1
MOVW A,SP	2	1	(A) ← (SP)	–	–	dH	– – – –	F1
MOV @A,T	3	1	((A)) ← (T)	–	–	–	– – – –	82
MOVW @A,T	4	1	((A)) ← (TH),((A) + 1) ← (TL)	–	–	–	– – – –	83
MOVW IX,#d16	3	3	(IX) ← d16	–	–	–	– – – –	E6
MOVW A,PS	2	1	(A) ← (PS)	–	–	dH	– – – –	70
MOVW PS,A	2	1	(PS) ← (A)	–	–	–	+ + + +	71
MOVW SP,#d16	3	3	(SP) ← d16	–	–	–	– – – –	E5
SWAP	2	1	(AH) ↔ (AL)	–	–	AL	– – – –	10
SETB dir: b	4	2	(dir): b ← 1	–	–	–	– – – –	A8 to AF
CLRB dir: b	4	2	(dir): b ← 0	–	–	–	– – – –	A0 to A7
XCH A,T	2	1	(AL) ↔ (TL)	AL	–	–	– – – –	42
XCHW A,T	3	1	(A) ↔ (T)	AL	AH	dH	– – – –	43
XCHW A,EP	3	1	(A) ↔ (EP)	–	–	dH	– – – –	F7
XCHW A,IX	3	1	(A) ↔ (IX)	–	–	dH	– – – –	F6
XCHW A,SP	3	1	(A) ↔ (SP)	–	–	dH	– – – –	F5
MOVW A,PC	2	1	(A) ← (PC)	–	–	dH	– – – –	F0

Notes: • During byte transfer to A, T ← A is restricted to low bytes.
• Operands in more than one operand instruction must be stored in the order in which their mnemonics are written. (Reverse arrangement of F²MC-8 family)

Table 3 Arithmetic Operation Instructions (62 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
ADDC A,Ri	3	1	(A) ← (A) + (Ri) + C	–	–	–	+ + + +	28 to 2F
ADDC A,#d8	2	2	(A) ← (A) + d8 + C	–	–	–	+ + + +	24
ADDC A,dir	3	2	(A) ← (A) + (dir) + C	–	–	–	+ + + +	25
ADDC A,@IX +off	4	2	(A) ← (A) + ((IX) +off) + C	–	–	–	+ + + +	26
ADDC A,@EP	3	1	(A) ← (A) + ((EP)) + C	–	–	–	+ + + +	27
ADDCW A	3	1	(A) ← (A) + (T) + C	–	–	dH	+ + + +	23
ADDC A	2	1	(AL) ← (AL) + (TL) + C	–	–	–	+ + + +	22
SUBC A,Ri	3	1	(A) ← (A) – (Ri) – C	–	–	–	+ + + +	38 to 3F
SUBC A,#d8	2	2	(A) ← (A) – d8 – C	–	–	–	+ + + +	34
SUBC A,dir	3	2	(A) ← (A) – (dir) – C	–	–	–	+ + + +	35
SUBC A,@IX +off	4	2	(A) ← (A) – ((IX) +off) – C	–	–	–	+ + + +	36
SUBC A,@EP	3	1	(A) ← (A) – ((EP)) – C	–	–	–	+ + + +	37
SUBCW A	3	1	(A) ← (T) – (A) – C	–	–	dH	+ + + +	33
SUBC A	2	1	(AL) ← (TL) – (AL) – C	–	–	–	+ + + +	32
INC Ri	4	1	(Ri) ← (Ri) + 1	–	–	–	+ + + –	C8 to CF
INCW EP	3	1	(EP) ← (EP) + 1	–	–	–	– – – –	C3
INCW IX	3	1	(IX) ← (IX) + 1	–	–	–	– – – –	C2
INCW A	3	1	(A) ← (A) + 1	–	–	dH	+ + – –	C0
DEC Ri	4	1	(Ri) ← (Ri) – 1	–	–	–	+ + + –	D8 to DF
DECW EP	3	1	(EP) ← (EP) – 1	–	–	–	– – – –	D3
DECW IX	3	1	(IX) ← (IX) – 1	–	–	–	– – – –	D2
DECW A	3	1	(A) ← (A) – 1	–	–	dH	+ + – –	D0
MULU A	19	1	(A) ← (AL) × (TL)	–	–	dH	– – – –	01
DIVU A	21	1	(A) ← (T) / (AL),MOD → (T)	dL	00	00	– – – –	11
ANDW A	3	1	(A) ← (A) ∧ (T)	–	–	dH	+ + R –	63
ORW A	3	1	(A) ← (A) ∨ (T)	–	–	dH	+ + R –	73
XORW A	3	1	(A) ← (A) ∀ (T)	–	–	dH	+ + R –	53
CMP A	2	1	(TL) – (AL)	–	–	–	+ + + +	12
CMPW A	3	1	(T) – (A)	–	–	–	+ + + +	13
RORC A	2	1	→ C → A ┐	–	–	–	+ + – +	03
ROLC A	2	1	┌ C ← A ←	–	–	–	+ + – +	02
CMP A,#d8	2	2	(A) – d8	–	–	–	+ + + +	14
CMP A,dir	3	2	(A) – (dir)	–	–	–	+ + + +	15
CMP A,@EP	3	1	(A) – ((EP))	–	–	–	+ + + +	17
CMP A,@IX +off	4	2	(A) – ((IX) +off)	–	–	–	+ + + +	16
CMP A,Ri	3	1	(A) – (Ri)	–	–	–	+ + + +	18 to 1F
DAA	2	1	Decimal adjust for addition	–	–	–	+ + + +	84
DAS	2	1	Decimal adjust for subtraction	–	–	–	+ + + +	94
XOR A	2	1	(A) ← (AL) ∀ (TL)	–	–	–	+ + R –	52
XOR A,#d8	2	2	(A) ← (AL) ∀ d8	–	–	–	+ + R –	54
XOR A,dir	3	2	(A) ← (AL) ∀ (dir)	–	–	–	+ + R –	55
XOR A,@EP	3	1	(A) ← (AL) ∀ ((EP))	–	–	–	+ + R –	57
XOR A,@IX +off	4	2	(A) ← (AL) ∀ ((IX) +off)	–	–	–	+ + R –	56
XOR A,Ri	3	1	(A) ← (AL) ∀ (Ri)	–	–	–	+ + R –	58 to 5F
AND A	2	1	(A) ← (AL) ∧ (TL)	–	–	–	+ + R –	62
AND A,#d8	2	2	(A) ← (AL) ∧ d8	–	–	–	+ + R –	64
AND A,dir	3	2	(A) ← (AL) ∧ (dir)	–	–	–	+ + R –	65

(Continued)

(Continued)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
AND A,@EP	3	1	(A) ← (AL) ∧ ((EP))	–	–	–	+ + R –	67
AND A,@IX +off	4	2	(A) ← (AL) ∧ ((IX) +off)	–	–	–	+ + R –	66
AND A,Ri	3	1	(A) ← (AL) ∧ (Ri)	–	–	–	+ + R –	68 to 6F
OR A	2	1	(A) ← (AL) ∨ (TL)	–	–	–	+ + R –	72
OR A,#d8	2	2	(A) ← (AL) ∨ d8	–	–	–	+ + R –	74
OR A,dir	3	2	(A) ← (AL) ∨ (dir)	–	–	–	+ + R –	75
OR A,@EP	3	1	(A) ← (AL) ∨ ((EP))	–	–	–	+ + R –	77
OR A,@IX +off	4	2	(A) ← (AL) ∨ ((IX) +off)	–	–	–	+ + R –	76
OR A,Ri	3	1	(A) ← (AL) ∨ (Ri)	–	–	–	+ + R –	78 to 7F
CMP dir,#d8	5	3	(dir) – d8	–	–	–	+ + + +	95
CMP @EP,#d8	4	2	((EP)) – d8	–	–	–	+ + + +	97
CMP @IX +off,#d8	5	3	((IX) + off) – d8	–	–	–	+ + + +	96
CMP Ri,#d8	4	2	(Ri) – d8	–	–	–	+ + + +	98 to 9F
INCW SP	3	1	(SP) ← (SP) + 1	–	–	–	– – – –	C1
DECW SP	3	1	(SP) ← (SP) – 1	–	–	–	– – – –	D1

Table 4 Branch Instructions (17 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
BZ/BEQ rel	3	2	If Z = 1 then PC ← PC + rel	–	–	–	– – – –	FD
BNZ/BNE rel	3	2	If Z = 0 then PC ← PC + rel	–	–	–	– – – –	FC
BC/BLO rel	3	2	If C = 1 then PC ← PC + rel	–	–	–	– – – –	F9
BNC/BHS rel	3	2	If C = 0 then PC ← PC + rel	–	–	–	– – – –	F8
BN rel	3	2	If N = 1 then PC ← PC + rel	–	–	–	– – – –	FB
BP rel	3	2	If N = 0 then PC ← PC + rel	–	–	–	– – – –	FA
BLT rel	3	2	If V ∀ N = 1 then PC ← PC + rel	–	–	–	– – – –	FF
BGE rel	3	2	If V ∀ N = 0 then PC ← PC + rel	–	–	–	– – – –	FE
BBC dir: b,rel	5	3	If (dir: b) = 0 then PC ← PC + rel	–	–	–	– + – –	B0 to B7
BBS dir: b,rel	5	3	If (dir: b) = 1 then PC ← PC + rel	–	–	–	– + – –	B8 to BF
JMP @A	2	1	(PC) ← (A)	–	–	–	– – – –	E0
JMP ext	3	3	(PC) ← ext	–	–	–	– – – –	21
CALLV #vct	6	1	Vector call	–	–	–	– – – –	E8 to EF
CALL ext	6	3	Subroutine call	–	–	–	– – – –	31
XCHW A,PC	3	1	(PC) ← (A),(A) ← (PC) + 1	–	–	dH	– – – –	F4
RET	4	1	Return from subrountine	–	–	–	– – – –	20
RETI	6	1	Return form interrupt	–	–	–	Restore	30

Table 5 Other Instructions (9 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
PUSHW A	4	1		–	–	–	– – – –	40
POPW A	4	1		–	–	dH	– – – –	50
PUSHW IX	4	1		–	–	–	– – – –	41
POPW IX	4	1		–	–	–	– – – –	51
NOP	1	1		–	–	–	– – – –	00
CLRC	1	1		–	–	–	– – – R	81
SETC	1	1		–	–	–	– – – S	91
CLRI	1	1		–	–	–	– – – –	80
SETI	1	1		–	–	–	– – – –	90

■ INSTRUCTION MAP

L \ H	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	SWAP	RET	RETI	PUSHW A	POPW A	MOV A,ext	MOVW A,PS	CLRI	SETI	CLRB dir: 0	BBC dir: 0,rel	INCW A	DECW A	JMP @A	MOVW A,PC
1	MULU A	DIVU A	JMP addr16	CALL addr16	PUSHW IX	POPW IX	MOV ext,A	MOVW PS,A	CLRC	SETC	CLRB dir: 1	BBC dir: 1,rel	INCW SP	DECW SP	MOVW SP,A	MOVW A,SP
2	ROLC A	CMP A	ADDC A	SUBC A	XCH A, T	XOR A	AND A	OR A	MOV @A,T	MOV A,@A	CLRB dir: 2	BBC dir: 2,rel	INCW IX	DECW IX	MOVW IX,A	MOVW A,IX
3	RORC A	CMPW A	ADDCW A	SUBCW A	XCHW A, T	XORW A	ANDW A	ORW A	MOVW @A,T	MOVW A,@A	CLRB dir: 3	BBC dir: 3,rel	INCW EP	DECW EP	MOVW EP,A	MOVW A,EP
4	MOV A,#d8	CMP A,#d8	ADDC A,#d8	SUBC A,#d8		XOR A,#d8	AND A,#d8	OR A,#d8	DAA	DAS	CLRB dir: 4	BBC dir: 4,rel	MOVW A,ext	MOVW ext,A	MOVW A,#d16	XCHW A,PC
5	MOV A,dir	CMP A,dir	ADDC A,dir	SUBC A,dir	MOV dir,A	XOR A,dir	AND A,dir	OR A,dir	MOV dir,#d8	CMP dir,#d8	CLRB dir: 5	BBC dir: 5,rel	MOVW A,dir	MOVW dir,A	MOVW SP,#d16	XCHW A,SP
6	MOV A,@IX +d	CMP A,@IX +d	ADDC A,@IX +d	SUBC A,@IX +d	MOV @IX +d,A	XOR @A,IX +d	AND A,@IX +d	OR A,@IX +d	MOV @IX +d,#d8	CMP @IX +d,#d8	CLRB dir: 6	BBC dir: 6,rel	MOVW A,@IX +d	MOVW @IX +d,A	MOVW IX,#d16	XCHW A,IX
7	MOV A,@EP	CMP A,@EP	ADDC A,@EP	SUBC A,@EP	MOV @EP,A	XOR A,@EP	AND A,@EP	OR A,@EP	MOV @EP,#d8	CMP @EP,#d8	CLRB dir: 7	BBC dir: 7,rel	MOVW A,@EP	MOVW @EP,A	MOVW EP,#d16	XCHW A,EP
8	MOV A,R0	CMP A,R0	ADDC A,R0	SUBC A,R0	MOV R0,A	XOR A,R0	AND A,R0	OR A,R0	MOV R0,#d8	CMP R0,#d8	SETB dir: 0	BBS dir: 0,rel	INC R0	DEC R0	CALLV #0	BNC rel
9	MOV A,R1	CMP A,R1	ADDC A,R1	SUBC A,R1	MOV R1,A	XOR A,R1	AND A,R1	OR A,R1	MOV R1,#d8	CMP R1,#d8	SETB dir: 1	BBS dir: 1,rel	INC R1	DEC R1	CALLV #1	BC rel
A	MOV A,R2	CMP A,R2	ADDC A,R2	SUBC A,R2	MOV R2,A	XOR A,R2	AND A,R2	OR A,R2	MOV R2,#d8	CMP R2,#d8	SETB dir: 2	BBS dir: 2,rel	INC R2	DEC R2	CALLV #2	BP rel
B	MOV A,R3	CMP A,R3	ADDC A,R3	SUBC A,R3	MOV R3,A	XOR A,R3	AND A,R3	OR A,R3	MOV R3,#d8	CMP R3,#d8	SETB dir: 3	BBS dir: 3,rel	INC R3	DEC R3	CALLV #3	BN rel
C	MOV A,R4	CMP A,R4	ADDC A,R4	SUBC A,R4	MOV R4,A	XOR A,R4	AND A,R4	OR A,R4	MOV R4,#d8	CMP R4,#d8	SETB dir: 4	BBS dir: 4,rel	INC R4	DEC R4	CALLV #4	BNZ rel
D	MOV A,R5	CMP A,R5	ADDC A,R5	SUBC A,R5	MOV R5,A	XOR A,R5	AND A,R5	OR A,R5	MOV R5,#d8	CMP R5,#d8	SETB dir: 5	BBS dir: 5,rel	INC R5	DEC R5	CALLV #5	BZ rel
E	MOV A,R6	CMP A,R6	ADDC A,R6	SUBC A,R6	MOV R6,A	XOR A,R6	AND A,R6	OR A,R6	MOV R6,#d8	CMP R6,#d8	SETB dir: 6	BBS dir: 6,rel	INC R6	DEC R6	CALLV #6	BGE rel
F	MOV A,R7	CMP A,R7	ADDC A,R7	SUBC A,R7	MOV R7,A	XOR A,R7	AND A,R7	OR A,R7	MOV R7,#d8	CMP R7,#d8	SETB dir: 7	BBS dir: 7,rel	INC R7	DEC R7	CALLV #7	BLT rel

■ MASK OPTIONS

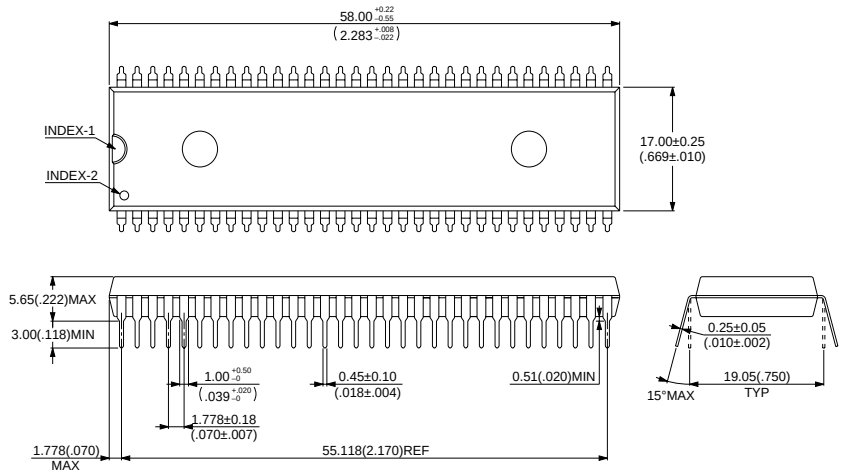
Model	MB89537H/537HC/ MB89538H/538HC/	MB89P538	MB89PV530
Specification method	Specify when ordering mask.	Setting unavailable.	Setting unavailable.
Oscillation stabilization delay time selection (for Fc= 10 MHz) • OSC1 - 2^3/Fc (Approx. 0.8 us). • OSC1 - 2^{14}/Fc (Approx. 1.6 ms). • OSC2 - 2^{17}/Fc (Approx. 13.1 ms). • OSC3 - 2^{18}/Fc (Approx. 26.2 ms).	Selectable	2^{18}/Fc (Approx. 26.2 ms)	2^{18}/Fc (Approx. 26.2 ms).

■ ORDERING INFORMATION

Part number	Package	Remarks
MB89537H-SH MB89537HC-SH MB89538H-SH MB89538HC-SH MB89P538-SH-101 MB89P538-SH-102	64-pin Plastic SH-DIP (DIP-64P-M01)	101-- Single clock 102 -- Dual clock
MB89537HPVF MB89537HCPVF MB89P538-SH-101 MB89P538-SH-102	64-pin Plastic LQFP (FPT-64P-M03)	
MB89537HPF MB89537HCPF MB89538HPF MB89538HCPF	64-pin Plastic QFP (FPT-64P-M06)	
MB89537HPFM MB89537HCPFM MB89P538-SH-101 MB89P538-SH-102	64-pin Plastic QFP (FPT-64P-M09)	
MB89PV530CF-101 MB89PV530CF-102	64-pin Ceramic MQFP (MQP-64C-P01)	
MB89PV530-SH-101 MB89PV530-SH-102	64-pin Ceramic MDIP (MQP-64C-P02)	

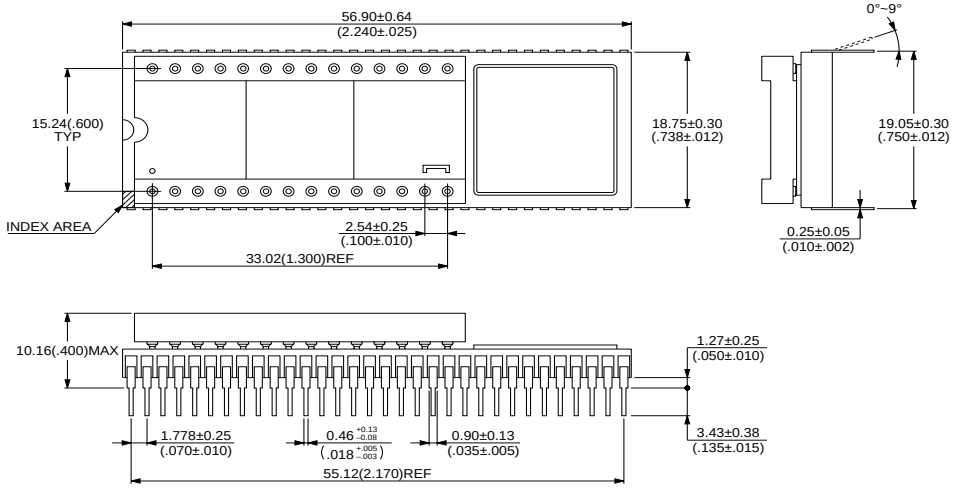
■ PACKAGE DIMENSIONS

64-pin Plastic SH-DIP
DIP-64P-MO1



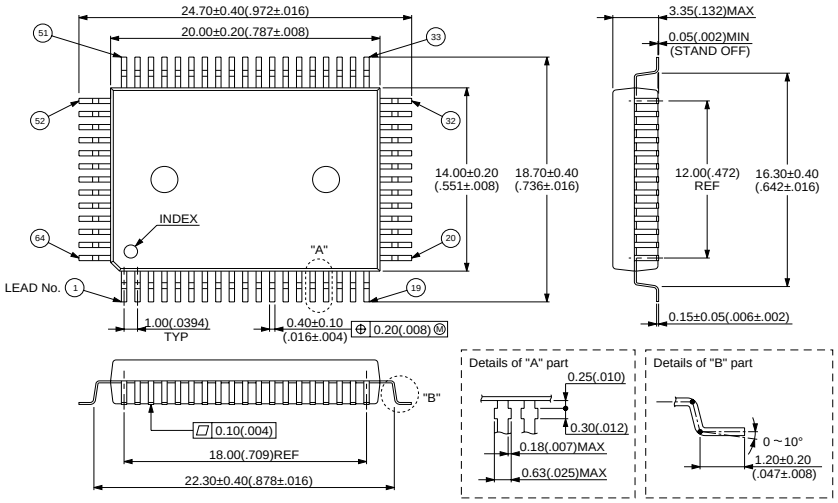
Dimensions in mm (inches)

64-pin Ceramic MDIP
MDP-64C-PO2



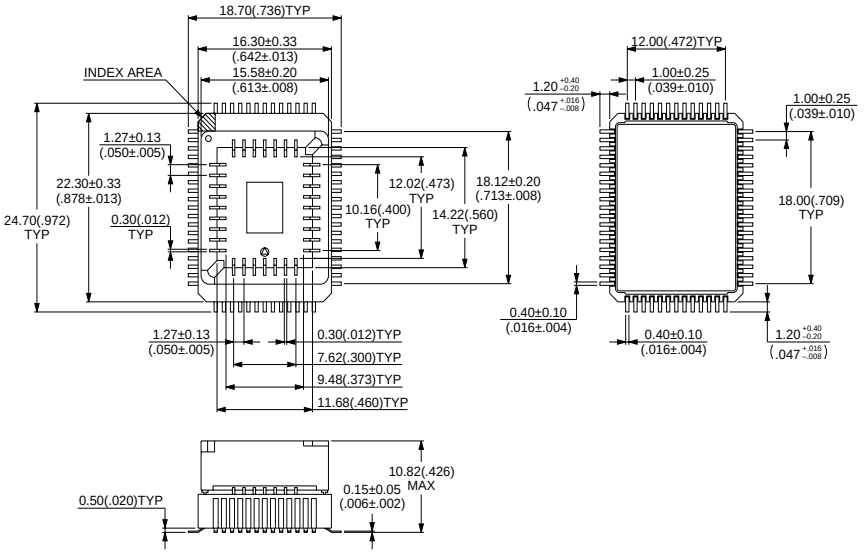
Dimensions in mm (inches)

64-pin Plastic QFP
FPT-64P-MO6



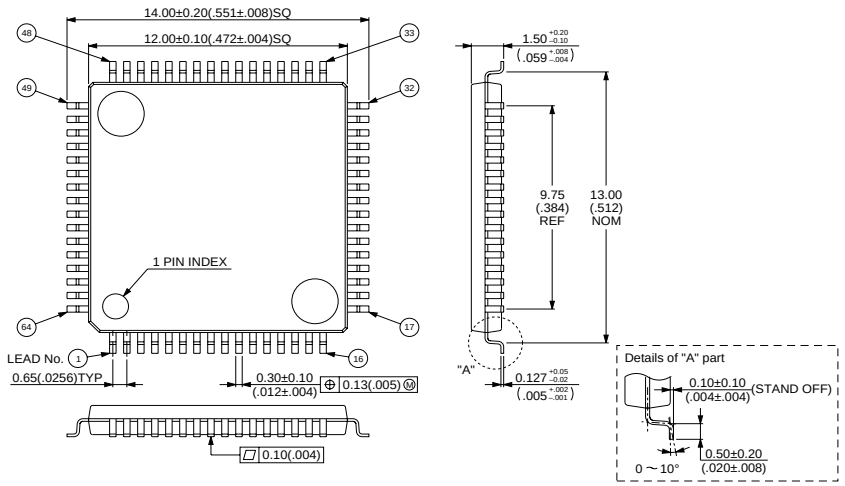
Dimensions in mm (inches)

64-pin Ceramic MQFP
MQP-64C-PO1



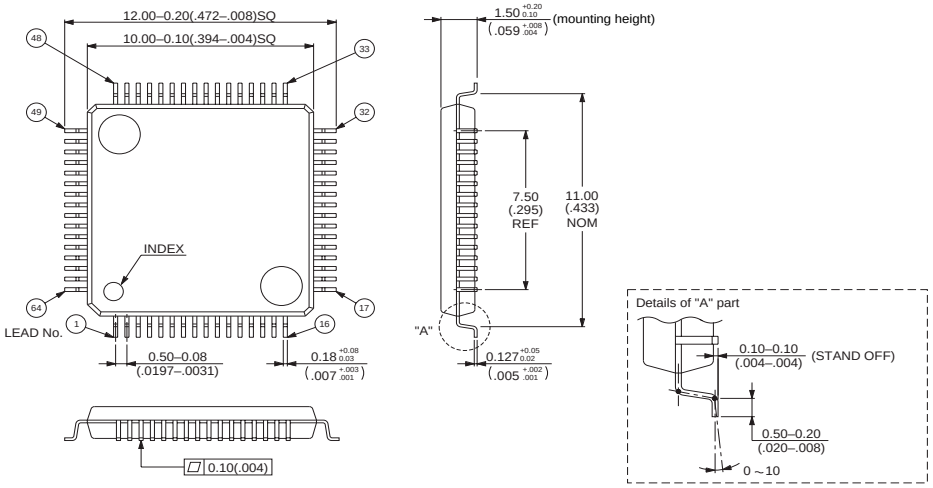
Dimensions in mm (inches)

64-pin Plastic QFP
FPT-64P-MO9



Dimensions in mm (inches)

64-pin Plastic LQFP
FPT-64P-MO3



Dimensions in mm (inches)

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