

HB56T433D Series

4,194,304-word × 32-bit High Density Dynamic RAM Module

HITACHI

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The HB56T433D is a 4 M × 32 dynamic RAM Small Outline DIMM (S.O.DIMM), mounted 8 pieces of 16 Mbit DRAM (HM5117400ATS/ALTS) sealed in TSOP package. An outline of the HB56T433D is 72-pin Zig Zag Dual tabs socket type compact and thin package.

Therefore, the HB56T433D makes high density mounting possible without surface mount technology. Decoupling capacitors are mounted beside the each TSOP of its module board.

- TTL compatible
- Test function
 - 16-bit parallel test mode

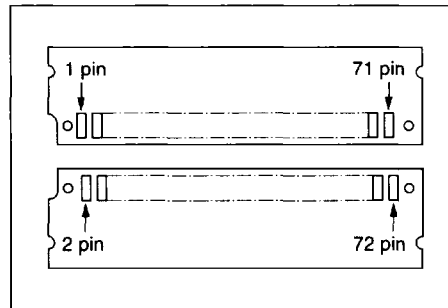
Ordering Information

Type No.	Access time	Package
HB56T433D-6A/6AL	60 ns	Small outline DIMM
HB56T433D-7A/7AL	70 ns	(72-pin)
HB56T433D-8A/8AL	80 ns	

Feature

- 72-pin
 - Lead pitch: 1.27 mm
- Single 5 V (± 5%) supply
- High speed
 - Access time: 60/70/80 ns (max)
- Low power dissipation
 - Active mode: 4.62/4.20/3.78 W (max)
 - Standby mode: 84 mW (max)
 - 6.3 mW (max) (L-version)
- Fast page mode capability
- 2,048 refresh cycle /32 ms
 - /128 ms (L-version)
- 3 variations of refresh
 - $\overline{\text{RAS}}$ -only refresh
 - $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh
 - Hidden refresh

Pin Arrangement



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Pin Arrangement (cont)

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	V _{SS}	37	DQ18	2	DQ0	38	DQ19
3	DQ1	39	V _{SS}	4	DQ2	40	$\overline{\text{CE}}_0$
5	DQ3	41	$\overline{\text{CE}}_2$	6	DQ4	42	$\overline{\text{CE}}_3$
7	DQ5	43	$\overline{\text{CE}}_1$	8	DQ6	44	$\overline{\text{RE}}_0$
9	DQ7	45	NC	10	V _{CC}	46	NC
11	PD1	47	$\overline{\text{WE}}$	12	A0	48	NC
13	A1	49	DQ20	14	A2	50	DQ21
15	A3	51	DQ22	16	A4	52	DQ23
17	A5	53	DQ24	18	A6	54	DQ25
19	A10	55	NC	20	NC	56	DQ27
21	DQ9	57	DQ28	22	DQ10	58	DQ29
23	DQ11	59	DQ31	24	DQ12	60	DQ30
25	DQ13	61	V _{CC}	26	DQ14	62	DQ32
27	DQ15	63	DQ33	28	A7	64	DQ34
29	NC	65	NC	30	V _{CC}	66	PD2
31	A8	67	PD3	32	A9	68	PD4
33	NC	69	PD5	34	$\overline{\text{RE}}_2$	70	PD6
35	DQ16	71	PD7	36	NC	72	V _{SS}

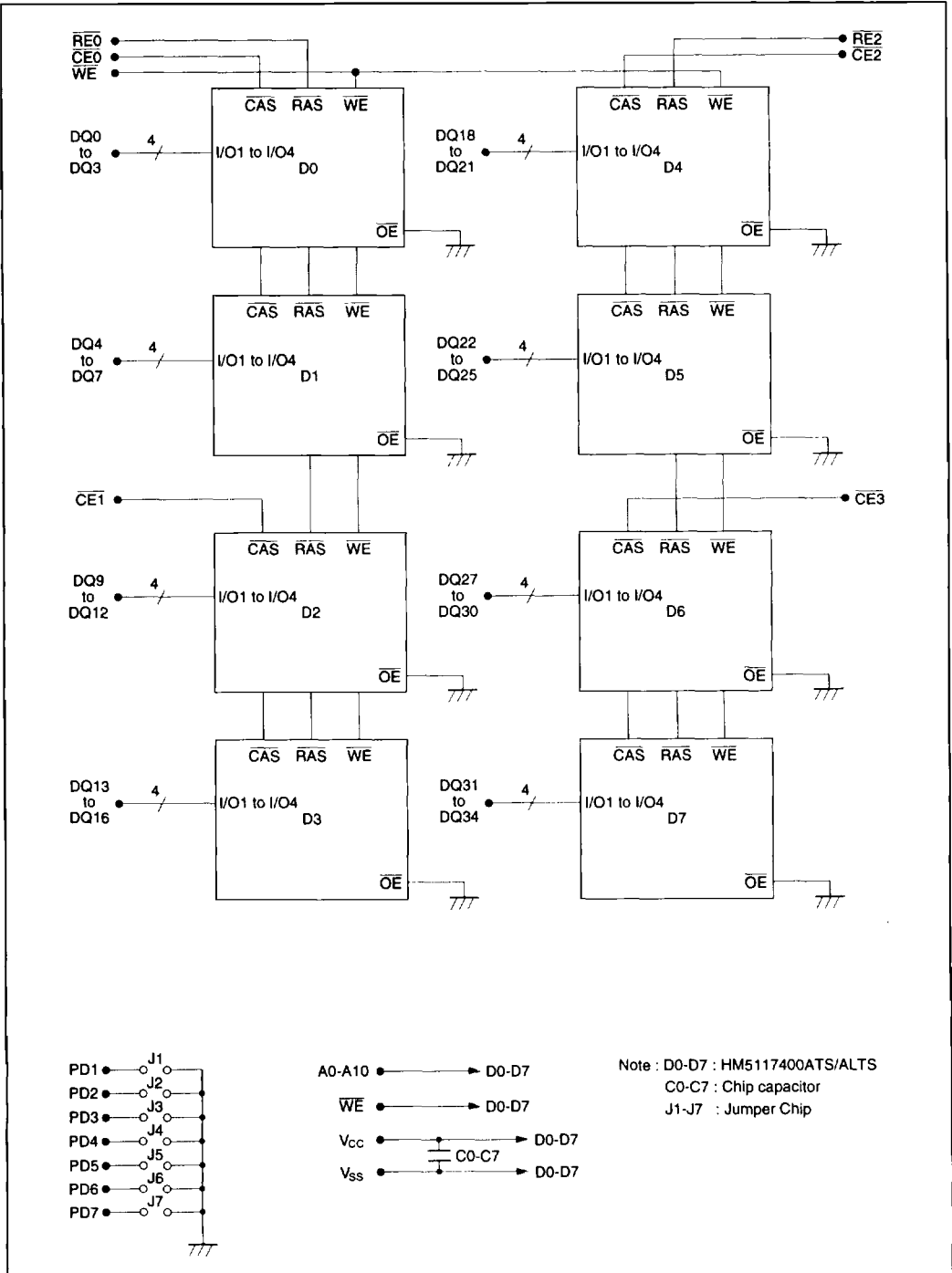
Pin Description

Pin name	Function
A0 – A10	Address input
A0 – A10	Refresh address input
DQ0 – DQ7 DQ9 – DQ16 DQ18 – DQ25 DQ 27 – DQ 34	Data-in/data-out
$\overline{\text{CE}}_0$ – $\overline{\text{CE}}_3$	Column address strobe
$\overline{\text{RE}}_0$, $\overline{\text{RE}}_2$	Row address strobe
$\overline{\text{WE}}$	Read/write enable
V _{CC}	Power supply (+5 V)
V _{SS}	Ground
PD1 – PD7	Presence detect pin
NC	No connection

Presence Detect Pin Arrangement

Pin No.	Pin name	HB56T433D		
		60 ns	70 ns	80 ns
11	PD1	NC	NC	NC
66	PD2	NC	NC	NC
67	PD3	V _{SS}	V _{SS}	V _{SS}
68	PD4	NC	NC	NC
69	PD5	NC	V _{SS}	NC
70	PD6	NC	NC	V _{SS}
71	PD7	NC	NC	NC

Block Diagram



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Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	(Input) V_{in}	-1.0 to +7.0	V
	(Output) V_{out}	-1.0 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	-1.0 to +7.0	V
Short circuit output current	I_{out}	50	mA
Power dissipation	P_T	8	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	-55 to +125	°C

Recommended DC Operating Conditions ($T_a = 0$ to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.75	5.0	5.25	V	1
Input high voltage	V_{IH}	2.4	—	6.5	V	1
Input low voltage	V_{IL}	-1.0	—	0.8	V	1

Note: 1. All voltage referred to V_{SS} .

DC Electrical Characteristics ($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 5\%$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	HB56T433D						Unit	Test conditions	Note
		60 ns		70 ns		80 ns				
		Min	Max	Min	Max	Min	Max			
Operating current	I_{CC1}	—	880	—	800	—	720	mA	$t_{RC} = \text{min}$	1, 2
Standby current	I_{CC2}	—	16	—	16	—	16	mA	TTL interface $\overline{\text{RAS}}, \overline{\text{CAS}} = V_{IH}$ Dout = High-Z	
		—	8	—	8	—	8	mA	CMOS interface $\overline{\text{RAS}}, \overline{\text{CAS}}$ $\geq V_{CC} - 0.2\text{ V}$ Dout = High-Z	
Standby current (L-version)	I_{CC2}	—	1.2	—	1.2	—	1.2	mA	CMOS interface $\overline{\text{RAS}}, \overline{\text{CAS}}$ $\geq V_{CC} - 0.2\text{ V}$ Dout = High-Z	
$\overline{\text{RAS}}$ -only refresh current	I_{CC3}	—	880	—	800	—	720	mA	$t_{RC} = \text{min}$	2
Standby current	I_{CC5}	—	40	—	40	—	40	mA	$\overline{\text{RAS}} = V_{IH}$ $\overline{\text{CAS}} = V_{IL}$ Dout = enable	1
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh current	I_{CC6}	—	880	—	800	—	720	mA	$t_{RC} = \text{min}$	
First page mode current	I_{CC7}	—	640	—	560	—	520	mA	$t_{PC} = \text{min}$	1, 3
Battery backup current (L-version)	I_{CC10}	—	2.8	—	2.8	—	2.8	mA	CMOS interface Dout = High-Z CBR refresh: $t_{RC} = 62.5\ \mu\text{s}$ $t_{RAS} \leq 0.3\ \mu\text{s}$	
Input leakage current	I_{LI}	-10	10	-10	10	-10	10	μA	$0\text{ V} \leq V_{in} \leq 7\text{ V}$	
Output leakage current	I_{LO}	-10	10	-10	10	-10	10	μA	$0\text{ V} \leq V_{out} \leq 7\text{ V}$ Dout = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = -5 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low Iout = 4.2 mA	

- Notes: 1. I_{CC} depends on output load condition when the device is selected I_{CC} max is specified at the output open condition.
 2. Address can be changed once or less while $\overline{\text{RAS}} = V_{IL}$.
 3. Address can be changed once or less while $\overline{\text{CAS}} = V_{IH}$.

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Capacitance ($T_a = 25^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 5\%$)

Parameter	Symbol	Typ	Max	Unit	Note
Input capacitance (Address)	C_{I1}	—	68	pF	1
Input capacitance (\overline{WE})	C_{I2}	—	76	pF	1
Input capacitance (\overline{RAS})	C_{I3}	—	43	pF	1
Input capacitance (\overline{CAS})	C_{I4}	—	29	pF	1
Output capacitance (DQ0 – 7, 9 – 16, 18 – 25, 29 – 30)	$C_{I/O}$	—	17	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS} = V_{IH}$ to disable Dout.

AC Characteristics

- Refer to the HM5117400A data sheet.

Physical Outline

Unit: mm

