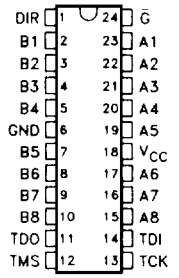
SN54BCT8245, SN74BCT8245
SCAN TEST DEVICE WITH OCTAL TRANSCEIVERS

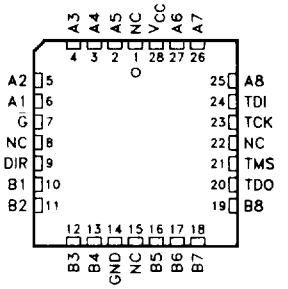
MAY 1989

- **Device is a member of Texas Instruments SCOPE™ Family of Testability Products**
- **Octal Test Integrated Circuit**
- **Compatible with the Proposed IEEE P1149.1 Serial Test Bus**
- **Functionally Equivalent to 54/74F245 and 54/74BCT245 in the Normal Function Mode**
- **Implements Optional "Test Reset" Signal on TAP by Recognizing a Double-High on TMS Pin**
- **Test Operation Synchronous to Test Access Port (TAP)**
- **16 Test Instructions—Conforms to the Proposed JTAG Boundary Scan—Provides Data Compression of Inputs—Provides Pseudo-Random Pattern Generation from Outputs—Output Toggle Boundary Mode—Outputs to High Impedance State Mode**
- **Package Options Include "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300 mil DIPs**

SN54BCT8245 ... JT PACKAGE
SN74BCT8245 ... DW OR NT PACKAGE
(TOP VIEW)



SN54BCT8245 ... FK PACKAGE
(TOP VIEW)



description

The SN54BCT8245 and SN74BCT8245 are members of Texas Instruments SCOPE™ testability IC family. This family of components blend test circuitry with standard logic functions to facilitate testing of complex circuit board assemblies. Scan access to the test circuitry is accomplished via the 4-wire Test Access Port (TAP) interface. In normal mode these devices are functionally equivalent to the SN54/74F245 and SN54/74BCT245 octal transceivers. In normal mode the test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary test cells. Activating the TAP in normal mode does not affect the functional operation of the SCOPE octal buffers.

In test mode the normal operation of the SCOPE octal buffer is inhibited and the test circuitry is enabled to observe and control the device's I/O boundary. When enabled, the test circuitry can perform boundary scan test operations as described in the proposed JTAG/P1149.1 specification. Additionally, the test circuitry can perform other testing functions such as: parallel signature analysis on data inputs and pseudo-random pattern generation from data outputs. All testing and scan operations are synchronized to the TAP interface.

The SN54BCT8245 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74BCT8245 is characterized for operation from 0°C to 70°C.

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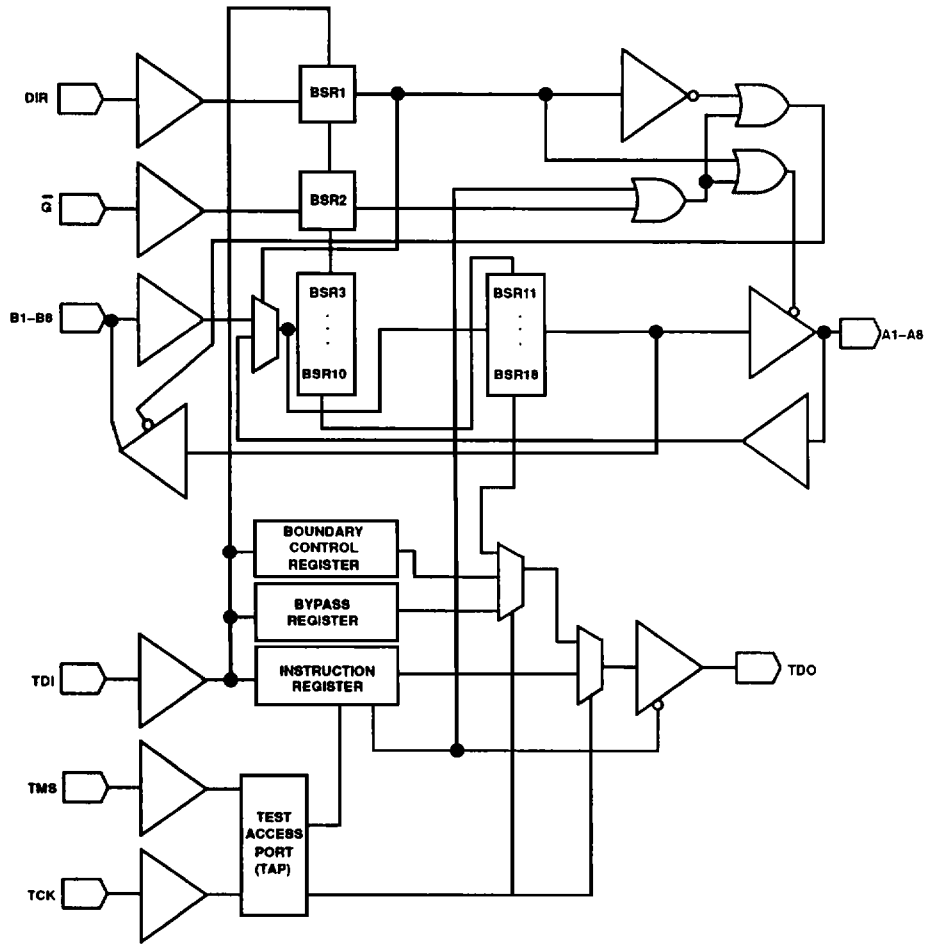
NORMAL MODE FUNCTION TABLE

ENABLE $\overline{G}$	DIRECTION CONTROL DIR	OPERATION
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

functional block diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} ..... −0.5 V to 7 V
Input voltage ..... −0.5 V to 7 V
Voltage applied to any output in the disabled or power-off state ..... −0.5 V to 5.5 V
Voltage applied to any output in the high state ..... −0.5 V to V_{CC}
Current into any output in the low state: SN54BCT8245 (A1 thru A8) ..... 40 mA
SN54BCT8245 (B1 thru B8) ..... 96 mA
SN74BCT8245 (A1 thru A8) ..... 48 mA
SN74BCT8245 (B1 thru B8) ..... 128 mA
Operating free-air temperature range: SN54BCT8245 ..... −55°C to 125°C
SN74BCT8245 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			SN54BCT8245			SN74BCT8245			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2		5.5	2		5.5	V
V_{IHH}	Double high-level input voltage	TMS	10.25	10.50	10.75	10.25	10.50	10.75	V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{IK}	Input clamp current				−18			−18	mA
I_{OH}	High-level output current	A1 thru A8			−3			−3	mA
		B1 thru B8			−12			−15	
I_{OL}	Low-level output current	A1 thru A8			20			24	mA
		B1 thru B8			48			64	
T_A	Operating free-air temperature		−55		125	0		70	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54BCT8245			SN74BCT8245			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V, I_I = −18 mA				−1.2			−1.2	V
V_{OH}	Any output	V_{CC} = 4.75 V, I_{OH} = −1 mA to −3 mA					2.7			V
	A1 thru A8	V_{CC} = 4.5 V	I_{OH} = −1 mA	2.5	3.4		2.5	3.4		
			I_{OH} = −3 mA	2.4	3.3		2.4	3.3		
	B1 thru B8	V_{CC} = 4.5 V	I_{OH} = −12 mA	2	3.2					
			I_{OH} = −15 mA				2	3.1		
V_{OL}	A1 thru A8	V_{CC} = 4.5 V	I_{OL} = 20 mA		0.3	0.5				V
			I_{OL} = 24 mA					0.35	0.5	
	B1 thru B8	V_{CC} = 4.5 V	I_{OL} = 48 mA		0.38	0.55				
			I_{OL} = 64 mA					0.42	0.55	
I_I	DIR and $\overline{G}$	V_{CC} = 5.5 V	V_I = 7 V			0.1			0.1	mA
	A and B	V_{CC} = 5.5 V	V_I = 5.5 V			1			1	
I_{IH}	A and B	V_{CC} = 5.5 V, V_I = 2.7 V				70			70	μA
	other	V_{CC} = 5.5 V, V_I = 2.7 V				20			20	
I_{IHH}	TMS	V_{CC} = 5.5 V, V_I = 10.50 V				1			1	mA
I_{IL}	A and B	V_{CC} = 5.5 V, V_I = 0.5 V				−0.65			−0.65	mA
	other	V_{CC} = 5.5 V, V_I = 0.5 V				−1.2			−1.2	
I_{OS}‡	A1 thru A8	V_{CC} = 5.5 V, V_O = 0		−60		−150	−60		−150	mA
	B1 thru B8	V_{CC} = 5.5 V, V_O = 0		−100		−225	−100		−225	
I_{CC}		V_{CC} = 5.5 V, Outputs open	Outputs high		5.5			5.5		mA
			Outputs low		52			52		
			Outputs disabled		2.3			2.3		
C_i		V_{CC} = 5.0 V, V_I = 2.5 V or 0.5 V								pF
C_{io}		V_{CC} = 5.0 V, V_O = 2.5 V or 0.5 V								pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

timing requirements (see Note 1)

		V_{CC} = 5 V, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX†				UNIT
		'BCT8245			SN54BCT8245		SN74BCT8245		
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{clock}	TCK	0							MHz
t_w	Pulse duration, TCK high or low								ns
t_{su}	Setup time, TMS before TCK ↑	9							ns
t_{su}	Setup time, TDI before TCK ↑	9							ns
t_{su}	Setup time, Any A or B before TCK ↑	9							ns
t_{su}	Setup time, $\overline{G}$ before TCK ↑	9							ns
t_h	Hold time, TMS after TCK ↑	1							ns
t_h	Hold time, TDI after TCK ↑	1							ns
t_h	Hold time, Any A or B after TCK ↑	1							ns
t_h	Hold time, $\overline{G}$ after TCK ↑	1							ns
t_{pu}	Wait time, power-up to TCK ↑	100							ns

† For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.

NOTE 1: See General Information for load circuits and waveforms.

'BCT8245 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†				UNIT
			'BCT8245			SN54BCT8245		SN74BCT8245		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	TCK			20						MHz
t_{PLH}	A or B	B or A		5.9						ns
t_{PHL}				6.5						
t_{PLH}	TCK ↓	A or B		11.5						ns
t_{PHL}				11						
t_{PLH}	TCK ↓	TDO		9.8						ns
t_{PHL}				9.7						
t_{PZH}	$\overline{G}$	A or B		6.2						ns
t_{PZL}				13						
t_{PZH}	TCK ↓	A or B		8						ns
t_{PZL}				7.7						
t_{PZH}	TCK ↓	TDO		14						ns
t_{PZL}				9.2						
t_{PHZ}	$\overline{G}$	A or B		7.5						ns
t_{PLZ}				13						
t_{PHZ}	TCK ↓	A or B		7						ns
t_{PLZ}				6.7						
t_{PHZ}	TCK ↓	TDO		13						ns
t_{PLZ}				7.8						

† For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
NOTE 1: See General Information for load circuits and waveforms.

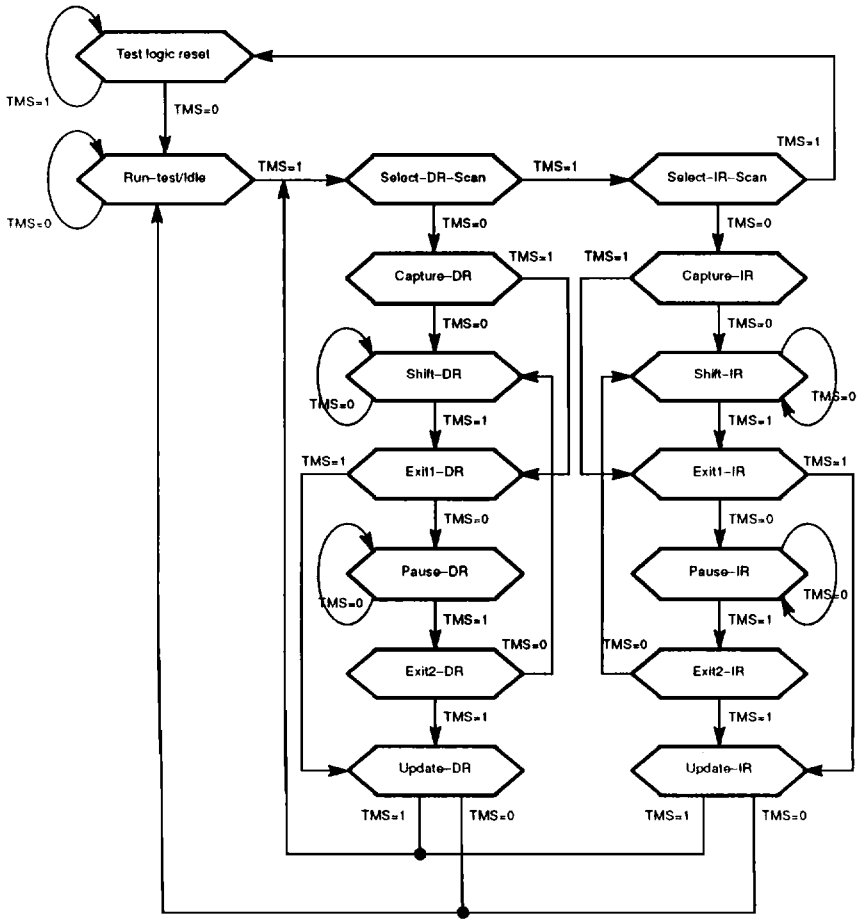

FIGURE 1. TAP STATE DIAGRAM

functional description

JTAG test information is conveyed by means of a 4-wire test bus. Test commands, test data, circuit state control instructions and synchronous control signals are all passed along the 4-wire bus. The function of the TAP is to extract the state control information and synchronous control signals from the 4-wire test bus, and generate the appropriate on-chip control signals for the JTAG test structures on the device. To accomplish this, the TAP cell monitors two signals from the 4-wire test bus—TCK (the JTAG Test Clock) and TMS (the JTAG Test Mode Select line). The functional block diagram on page 2 illustrates the JTAG 4-wire test bus and boundary scan architecture, and the relationship between the TAP cell, the 4-wire bus, and the various boundary scan test elements.

architectural elements

boundary scan register BSR0–BSR17

The boundary scan register contains eighteen (18) bits—one for each functional input or output pin of the device. FIGURE 2 illustrates the order of bits in the boundary scan register scan path. The boundary scan registers allow for board interconnect testing, defining conditions at the device logic periphery, and sampling data on the functional input or output pins without disturbing normal device operations.

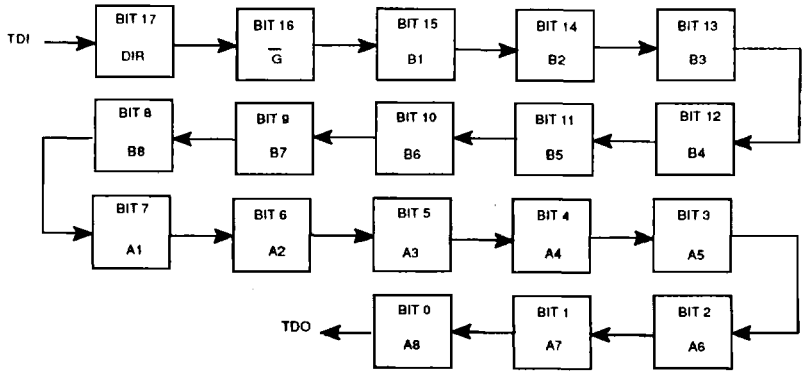

FIGURE 2. BOUNDARY SCAN REGISTER ORDER OF SCAN

bypass register

The bypass register contains one (1) bit for use when the device is in the bypass scan mode as defined in TABLE 3. FIGURE 3 illustrates the flow through the bypass register. This register provides a short one bit scan path through the device rather than scanning through the eighteen bit boundary scan register path. This is especially useful for decreasing test access times to a particular device on a board with several JTAG compatible devices which are not required for a specific test.

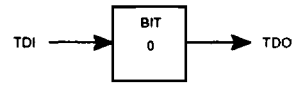

FIGURE 3. BYPASS REGISTER ORDER OF SCAN

test data register

The test data register contains two (2) bits used to control test operations occurring at the boundary. FIGURE 4 illustrates the order of bits in the test data register scan path.

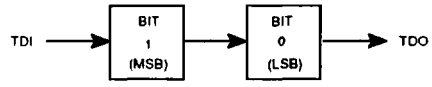

FIGURE 4. TEST DATA REGISTER ORDER OF SCAN

In addition to the boundary test instructions shown in TABLE 3, additional test operations shown in TABLE 1 can be performed when the run test opcode is installed in the instruction register. These test operations include: pseudo-random pattern generation (PRPG) and parallel signature analysis (PSA) as shown in TABLE 1 when the run test opcode is installed in the instruction register.

TABLE 1. RUN TEST OPCODES

OPCODE MSB → LSB	TEST
00	SAMPLE INPUTS/TOGGLE OUTPUTS
01	PRPG/16 BIT MODE
10	PSA/16 BIT MODE
11	SIMULTANEOUS PRPG AND PSA/8 BIT MODE

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example

In order to implement the sample inputs/toggle outputs opcode from TABLE 1, a series of operations must be performed. Refer to FIGURE 1 to trace these operations through the TAP state diagram. The select-IR path is used to shift opcodes into the instruction register. The select-DR path is used to shift data into the boundary scan register or bypass register, or to shift opcodes into the test data register. To shift data or opcodes into the registers, after entering the appropriate shift-DR or shift-IR state TMS must be held low for enough TCK pulses to shift the correct number of bits into the registers.

First, the boundary read opcode (test or normal mode) must be loaded into the instruction register using the select-IR scan path, then the boundary scan registers may be initialized using the select-DR scan path. Load the test data register scan opcode (test or normal mode) into the instruction register using the select-IR scan path, then the sample inputs/toggle outputs opcode (00) may be entered into the test data register using the select-DR-scan path. Finally, the boundary run test opcode (test or normal mode) must be entered into the instruction register using the select-IR scan path. Exiting the select-IR-scan path to the run-test/idle state starts the outputs toggling. As long as the device remains in the run-test/idle state, each TCK pulse will cause the device's function outputs to toggle to the opposite state.

tap bits

Tap bit settings used for PSA and PRPG test operations are shown in TABLE 2. The use of these tap bits as well as the shift operations necessary to perform 8-bit and 16-bit PSA and PRPG test operations is described in FIGURE 5 through FIGURE 7.

TABLE 2. TAP BIT SETTINGS FOR PSA AND PRPG TEST OPERATIONS

OPERATION	MODE	TAP BITS A → Y
PSA	8-BIT	B2, B3, B4, B8
	16-BIT	B7, A1, A4, A8
PRPG	8-BIT	A2, A3, A4, A8
	16-BIT	B7, A1, A4, A8

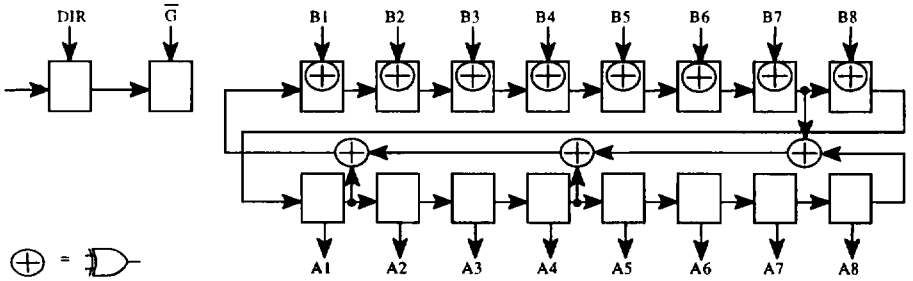

FIGURE 5. 16-BIT PSA CONFIGURATION DURING RUN TEST/IDLE STATE

A PSA operation on the 8 data inputs proceeds as the 8 data outputs are held static.

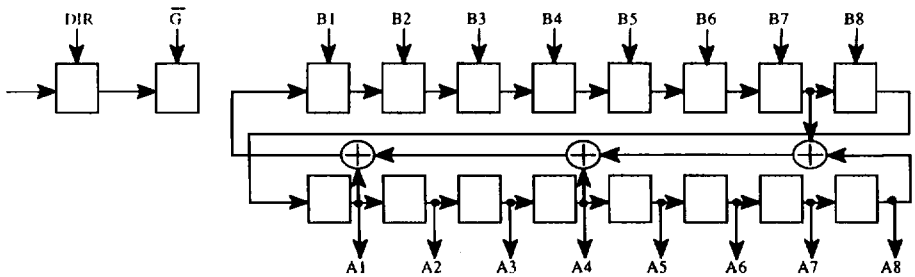

FIGURE 6. 16-BIT PRPG CONFIGURATION DURING RUN TEST/IDLE STATE

A PRPG operation from the 8 data outputs proceeds while the 8 data inputs are ignored.

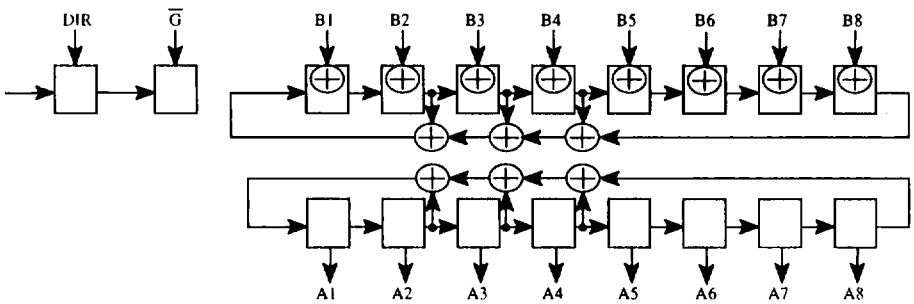

FIGURE 7. 8-BIT PSA AND PRPG CONFIGURATION DURING RUN TEST/IDLE STATE

Simultaneously, an 8-bit PSA operation proceeds on the 8 data inputs, while an 8-bit PRPG operation proceeds from the 8 data outputs.

Instruction register

The test device instruction register is 8 bits in length. When in the Shift-IR state, data can be scanned into the register from the most significant bit (MSB) to the least significant bit (LSB) as shown in FIGURE 8. The instruction register controls the internal device structures and test operations according to the opcodes listed in TABLE 3.

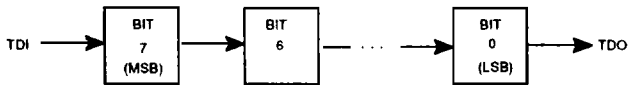

FIGURE 8. INSTRUCTION REGISTER ORDER OF SCAN

Instruction set

The 'BCT8245 uses the 8-bit serial instruction register as its instruction input. TABLE 3 summarizes the 8-bit opcodes and corresponding tests.

TABLE 3. OPCODES (see Note 1)

OPCODE BIT 7–BIT 0 MSB-LSB	FUNCTION
X0000000	BOUNDARY SCAN
X0000001	ID REGISTER SCAN
X0000010	SAMPLE BOUNDARY
X0000011	BOUNDARY SCAN
X0000100	BYPASS SCAN MODE
X0000101	BYPASS SCAN MODE
X0000110	CONTROL BOUNDARY TO HIGH IMPEDANCE
X0000111	CONTROL BOUNDARY TO 1/0
X0001000	BYPASS SCAN MODE
X0001001	BOUNDARY RUN TEST/TEST MODE
X0001010	BOUNDARY READ/NORMAL MODE
X0001011	BOUNDARY READ/TEST MODE
X0001100	BOUNDARY SELF TEST/NORMAL MODE
X0001101	BOUNDARY TOGGLE OUTPUTS/TEST MODE
X0001110	TEST DATA REGISTER SCAN/NORMAL MODE
X0001111	TEST DATA REGISTER SCAN/TEST MODE
ALL OTHER	BYPASS SCAN MODE

X = Parity Bit (Even Parity)
NOTE 1: If Bit 4 through Bit 6 are all 0, then Bit 0 through Bit 3 are decoded as shown in TABLE 3.

The test functions which are identified in TABLE 3 and performed by the test integrated circuits are defined as follows:

boundary scan

A boundary scan of the boundary scan register is performed according to the methodology designated by the proposed JTAG or the proposed IEEE P1149.1 specifications. This instruction performs a combination of sample boundary and control boundary to 1/0 tests as specified below.

ID register scan

The test circuit is placed in the bypass mode as defined by JTAG in the absence of an ID Register. A logic 0 is loaded into the bypass register before scanning.

sample boundary

Data appearing at the device's function inputs and outputs is sampled and scanned out the TDO pin. This operation is performed in a functional mode without disturbing normal device operations.

control boundary to high impedance

The device's function outputs are placed in the high impedance state. The bypass register is selected in the scan path. Function inputs remain operational.

control boundary to 1/0

Function inputs and outputs are controlled by the boundary register. The bypass register is selected in the scan path.

boundary run test

Test operations controlled by the test data register are performed while the device is in the idle mode. Operations performed in this mode include the following:

parallel signature analysis of inputs

Data appearing on the device's data inputs is compressed by a parallel signature analysis (PSA) operation with fixed tap bits. Data shall be compressed into sixteen bits. The initial seed value for the PSA operation should be scanned into the boundary scan register prior to performing the test operation.

pseudo-random pattern generation from outputs

A pseudo-random data pattern (PRPG) is output from the outputs of the test device. The initial seed value for the PRPG should be scanned into the data register prior to performing the test operation.

simultaneous PSA and PRPG

An 8-Bit PSA of inputs and an 8-Bit PRPG from outputs is performed simultaneously as specified above.

sample inputs/toggle outputs

The devices inputs are sampled on successive rising edges of TCK, while the device's function output pins are toggled simultaneously on successive falling edges of TCK while the device is in the idle mode. This test is intended to be used for parametric testing and pattern generation purposes. The initial pattern should be scanned into the boundary scan register prior to performing the test operation.

boundary read (test mode and normal mode)

Data is scanned in and out of the boundary scan register without first preloading the boundary condition. This function is particularly useful after a PSA operation—the results can be scanned out for review by the test controller.

test data register scan (test mode and normal mode)

The test data register is selected for scan access.

boundary self test

The boundary scan register is preloaded with the inverted contents of the latch memory elements of each boundary scan register bit. The boundary scan register is then scanned out. Prior to performing this test known data should be scanned into the boundary scan register.

boundary toggle outputs

The device's function output pins are toggled simultaneously on successive TCK clock inputs. This test is intended to be used for parametric testing and pattern generation purposes. The initial pattern should be scanned into the data register prior to performing the test operation.

bypass scan mode

The bypass register is selected in the scan path and the device is placed in the normal mode.