INTEGRATED CIRCUITS
UNITRODE

Complementary Switch FET Drivers

UC1714/5
UC2714/5
UC3714/5
PRELIMINARY

FEATURES

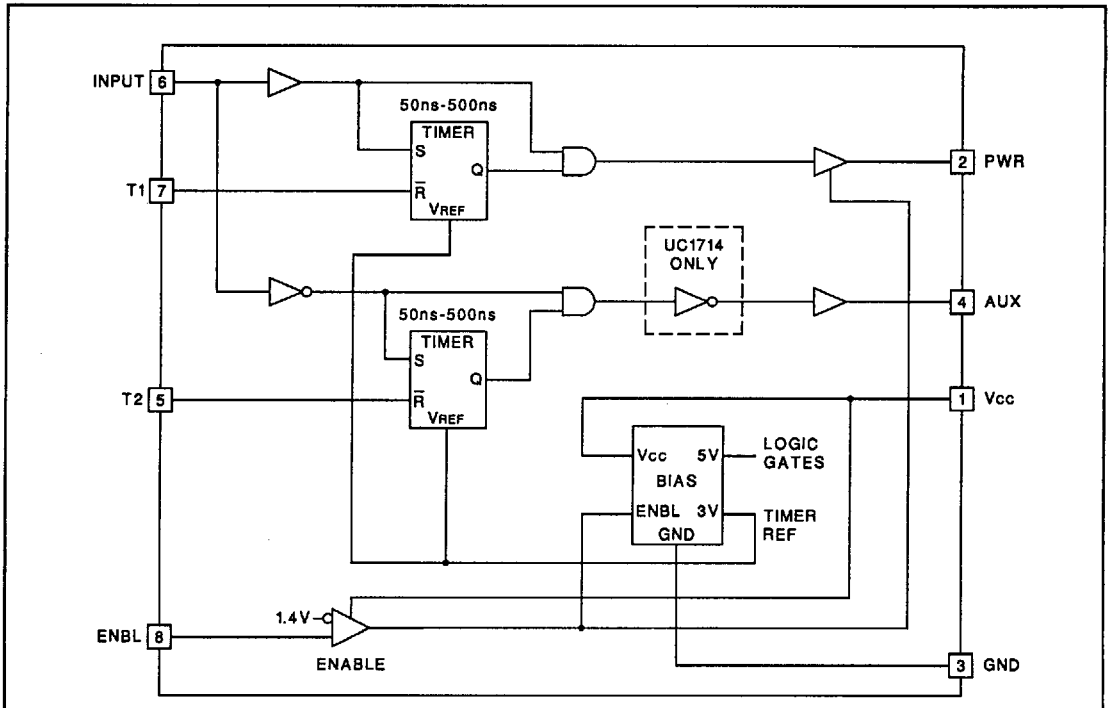
- Single Input (PWM and TTL Compatible)
- Auxiliary Output FET Driver, 0.5A Source/1A Sink
- High Current Power FET Driver, 1.0A Source/2A Sink
- Time Delays Between Power and Auxiliary Outputs Independently Programmable from 50ns to 500ns
- Time Delay or True Zero-Voltage Operation Independently Configurable for Each Output
- In-phase and Complementary Configuration
- Switching Frequency to 1MHz
- Typical 50ns Propagation Delays
- ENBL Pin Activates 120μA Sleep Mode
- Power Output is Active Low in Sleep Mode
- Synchronous Rectifier Driver

DESCRIPTION

These drivers are designed for complementary switch applications such as synchronous rectification and active clamp reset for zero voltage switching. ZVS, or "soft switching", offers the potential of greatly reduced switching losses which can lead to higher efficiency at higher switching frequencies. Its implementation requires an auxiliary switch which leads the primary power switch at turn on and trails it at turn off. In the UC1714 series, the auxiliary switch is in phase with the primary switch. In the UC1715, the auxiliary switch is out of phase with the primary switch. Each output has independently programmable time delays, but these delay terminals can also be used as voltage sensors for true zero voltage sensing.

These devices can be interfaced with all commonly available PWM controllers and, in addition to resonant switching, can be used for active reset or snubbing circuits and for synchronous rectifier drivers.

BLOCK DIAGRAM



Note: Pin numbers refer to J, N and D packages.

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ABSOLUTE MAXIMUM RATINGS

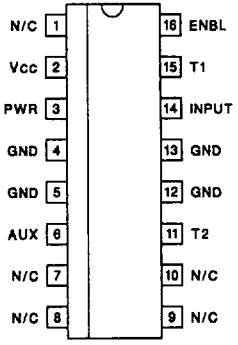
Supply Voltage Vcc 20V
Power Driver IOH
continuous ..... -200mA
peak ..... -1A
Power Driver IOL
continuous 400mA
peak 2A
Auxiliary Driver IOH
continuous ..... -100mA
peak ..... -500mA
Auxiliary Driver IOL
continuous 200mA
peak 1A
Input Voltage Range (INPUT, ENBL) ..... -0.3V to 20V
Storage Temperature Range ..... -65°C to 150°C
Operating Junction Temperature (Note 1) ..... 150°C
Lead Temperature (Soldering 10 seconds) ..... 300°C

Note 1: Unless otherwise indicated, voltages are referenced to ground and currents are positive into, negative out of, the specified terminals.

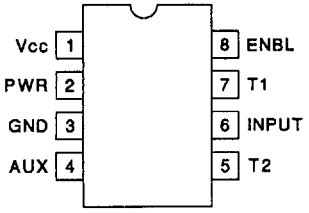
Note 2: Consult Packaging Section of databook for thermal limitations and specifications of packages.

CONNECTION DIAGRAMS

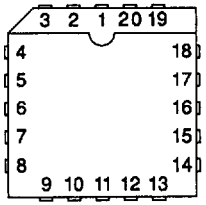
SOIC-16 (Top View)
DP Package



DIL-8, SOIC-8 (Top View)
J or N, D Packages



PLCC-20 (Top View)
Q Package



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1-2
Vcc	3
PWR	4
GND	5
N/C	6
AUX	7
N/C	8-13
T2	14
N/C	15
INPUT	16
T1	17
ENBL	18
N/C	19-20

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, Vcc = 15V, ENBL ≥ 2V, R_{T1} = 100kΩ from T1 to GND, R_{T2} = 100kΩ from T2 to GND, and -55°C < T_A < 125°C for the UC1714/5, -40°C < T_A < 85°C for the UC2714/5, and 0°C < T_A < 70°C for the UC3714/5, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Overall					
Vcc		7		20	V
Icc, nominal	ENBL = 2.0V		18	22	mA
Icc, sleep mode	ENBL = 0.8V		120	250	µA
Power Driver (PWR)					
Pre Turn-on PWR Output, Low	Vcc = 0V, I_{OUT} = 10mA		1.1	1.6	V
PWR Output Low, Sat.	INPUT = 0.8V, I_{OUT} = 40mA		0.3	0.8	V
	INPUT = 0.8V, I_{OUT} = 400mA		2.1	2.7	V
PWR Output High, Sat. (Vcc – V_{PWR})	INPUT = 2.0V, I_{OUT} = -20mA		2.1	3	V
	INPUT = 2.0V, I_{OUT} = -200mA		2.3	3	V
Rise Time	C_L = 2200pF		35		ns
Fall Time	C_L = 2200pF		30		ns
T1 Delay, PWR – AUX	INPUT rising edge, R_{T1} = 10kΩ (Note 4)		50	100	ns
T1 Delay, PWR – AUX	INPUT rising edge, R_{T1} = 100kΩ (Note 4)	300	500	700	ns
PWR Prop Delay	INPUT falling edge, 50% (Note 3)		35	85	ns

ELECTRICAL CHARACTERISTICS (cont.): Unless otherwise stated, Vcc = 15V, ENBL ≥ 2V, R_{T1} = 100kΩ from T1 to GND, R_{T2} = 100kΩ from T2 to GND, and –55°C < T_A < 125°C for the UC1714/5, –40°C < T_A < 85°C for the UC2714/5, and 0°C < T_A < 70°C for the UC3714/5, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Auxiliary Driver (AUX)					
AUX Output Low, Sat V_{AUX}	V_{IN} = 2.0V, I_{OUT} = 20mA		0.3	0.8	V
	V_{IN} = 2.0V, I_{OUT} = 200mA		1.8	2.5	V
AUX Output High, (Vcc – V_{AUX})	V_{IN} = 0.8V, I_{OUT} = -10mA		2.1	3.0	V
AUX Output High, Sat	V_{IN} = 0.8V, I_{OUT} = -100mA		2.3	3.0	V
Rise Time	C_L = 1000pF		45		ns
Fall Time	C_L = 1000pF		30		ns
T2 Delay, AUX - PWR	INPUT falling edge, R_{T2} = 10kΩ (Note 4)		50	100	ns
T2 Delay, AUX - PWR	INPUT falling edge, R_{T2} = 100kΩ (Note 4)	300	500	700	ns
AUX Prop Delay	INPUT rising edge, 50% (Note 3)		35	85	ns
Enable (ENBL)					
Input Threshold		0.8	1.2	2.0	V
Input Current, I_{IH}	ENBL = 15V		1	10	µA
Input Current, I_{IL}	ENBL = 0V		–1	–10	µA
T1					
Current Limit	T1 = 0V		–1	–2	mA
Nominal Voltage at T1		2.7	3	3.3	V
ZVS Delay	T1 = 2.5V, (Note 5)		50	100	ns
T2					
Current Limit	T2 = 0V		–1	–2	mA
Nominal Voltage at T2		2.7	3	3.3	V
ZVS Delay	T2 = 2.5V, (Note 5)		25	50	ns
Input (INPUT)					
Input Threshold		0.8	1.4	2.0	V
Input Current, I_{IH}	INPUT = 15V		1	10	µA
Input Current, I_{IL}	INPUT = 0V		–5	–20	µA

Note 3: Propagation delay times are measured from the 50% point of the input signal to the 10% point of the output signal's transition with no load on outputs.

Note 4: T1 (T2) Delay is defined as the time between the 10% transition point of AUX (PWR) and the 10% transition point of PWR (AUX) with no capacitive load on either output.

Note 5: ZVS Delay is defined as : for the PWR output, the 10% transistion point of its rising edge measured from the 50% point of the rising edge of INPUT and for the AUX, the 10% transition point of its rising edge on the UC1715 or the 90% transition point of its falling edge on the UC1714 measured from the 50% point of the falling edge of INPUT.

PIN DESCRIPTIONS

Vcc: The Vcc input range is from 7V to 20V. This pin should be bypassed with a capacitor to GND consistent with peak load current demands.

GND: This is the reference pin for all input voltages and the return point for all device currents. It carries the full peak sinking current from the outputs. Any tendency for the outputs to ring below GND voltage must be damped or clamped such that GND remains the most negative potential.

INPUT: The input switches at TTL logic levels (approximately 1.4V) but the allowable range is from 0 to 20V, allowing direct connection to most common IC PWM controller outputs. The rising edge immediately switches the AUX output, and initiates a timing delay, T1, before switching on the PWR output. Similarly, the INPUT falling edge immediately turns off the PWR output and initiates a timing delay, T2, before switching the AUX output.

It should be noted that if the input signal comes from a controller with FET drive capability, this signal provides another option. INPUT and PWR provide a delay only at the leading edge while INPUT and AUX provide the delay at the trailing edge.

PWR: The PWR output waits for the T1 delay after the INPUT's rising edge before switching on, but switches off immediately at INPUT's falling edge (neglecting propagation delays). This output is capable of sourcing 1A and

PIN DESCRIPTIONS (cont.)

sinking 2A of peak gate drive current. PWR output includes a passive, self-biased circuit which holds this pin active low during power-up and sleep mode.

AUX: The AUX switches immediately at INPUT's rising edge but waits through the T2 delay after INPUT's falling edge before switching. AUX is capable of sourcing 0.5A and sinking 1.0A of drive current. On the UC1714, the AUX output is in-phase with PWR, while in the UC1715, the two outputs are complementary. During power-up and sleep modes, AUX is inactive with a high impedance.

T1: A resistor to ground programs the time delay between AUX activation and PWR turn-on.

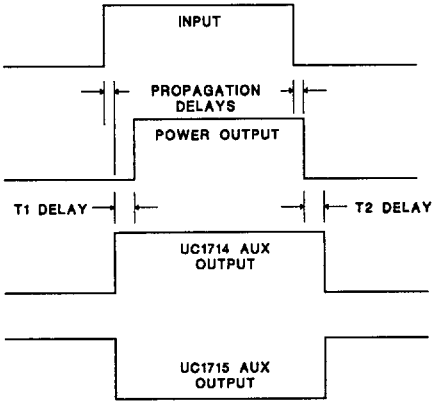
T2: This pin functions in the same way as T1 but controls the time delay between PWR turn-off and the return of the AUX output to an inactive state.

T1, T2: The resistor on each of these pins sets the charging current on internal timing capacitors to provide independent time control. The nominal voltage level at each pin is 3V and the current is internally limited to 1mA. The total delay from INPUT to each output includes a propagation delay in addition to the programmable timer but since the propagation delays are approximately equal, the relative time delay between the two outputs can be assumed to be solely a function of the programmed delays.

Either or both pins can alternatively be used for voltage sensing in lieu of delay programming. This is done by pulling the timer pins below their nominal voltage level which immediately activates the timer output.

ENBL: The ENBL input switches at TTL logic levels (approximately 1.2V), and its input range is from 0V to 20V. The ENBL input will place the device into sleep mode when it is a logical low. The current into Vcc during the sleep mode is typically 120μA.

Time Relationships (Notes 3, 4)



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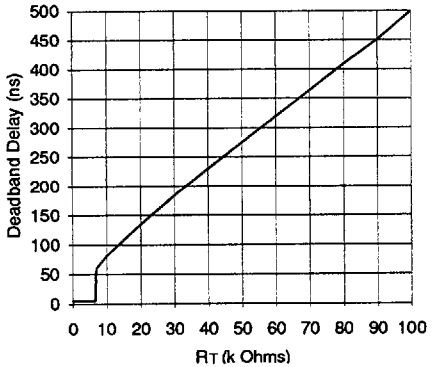
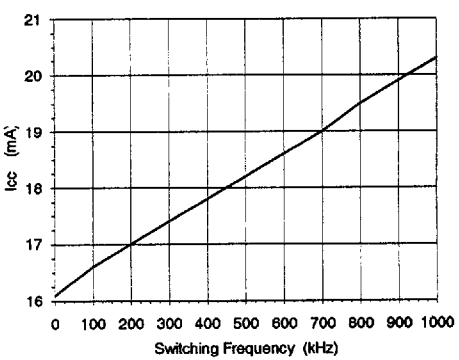
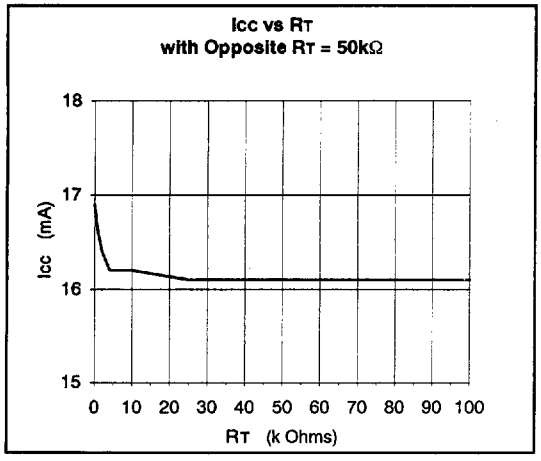
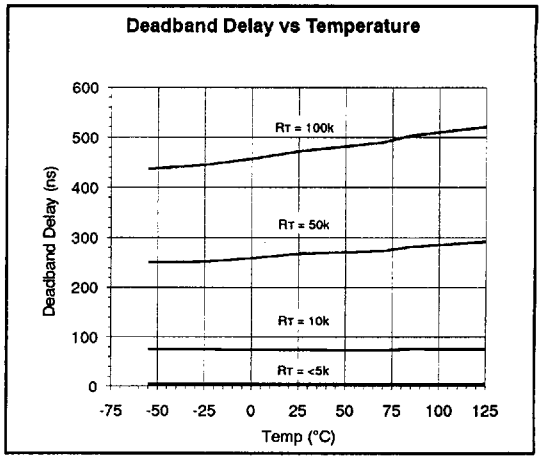
Deadband Delay vs RT



Icc vs Switching Frequency with No Load and 50% Duty Cycle RT1 = RT2 = 50kΩ







TYPICAL APPLICATIONS

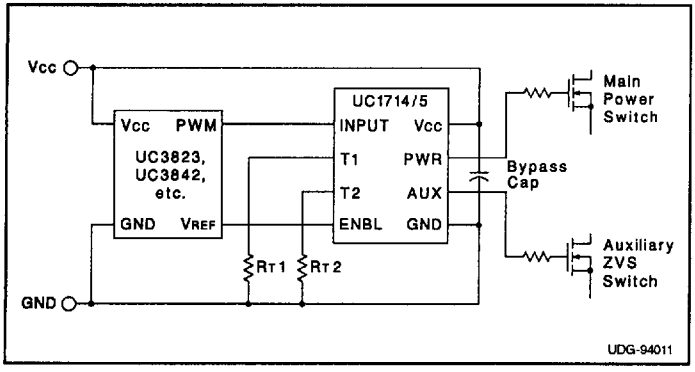


Figure 1. Typical Application With Timed Delays

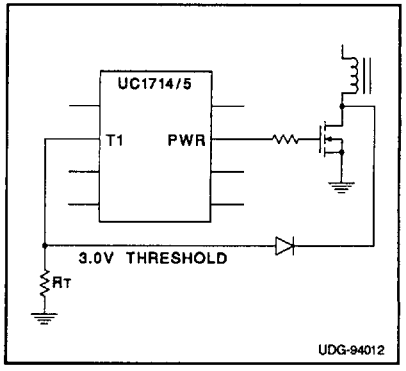


Figure 2. Using the Timer Input for Zero-Voltage Sensing

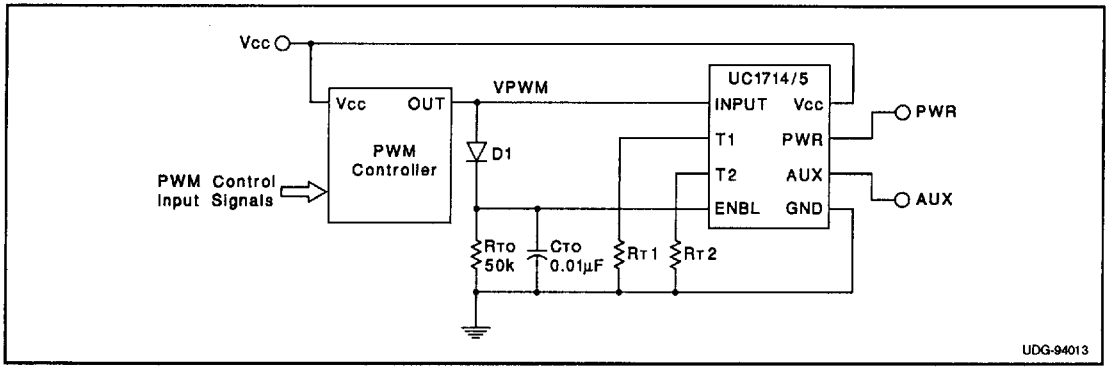


Figure 3. Self-actuated Sleep Mode with the Absence of an Input PWM Signal. Wake Up Occurs with the First Pulse while Turn-off is Determined by the RTO • CTO Time Constant

TYPICAL APPLICATIONS (cont.)

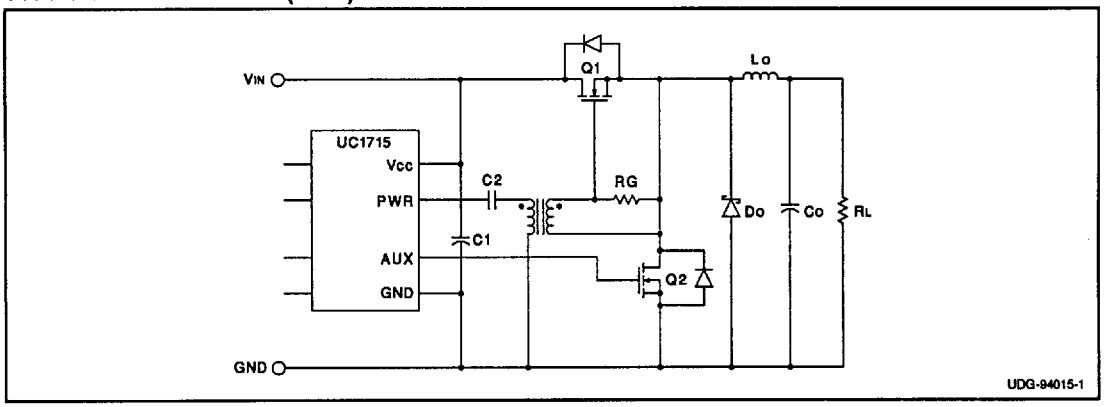


Figure 4. Using the UC1715 as a Complementary Synchronous Rectifier Switch Driver with N-Channel FETs

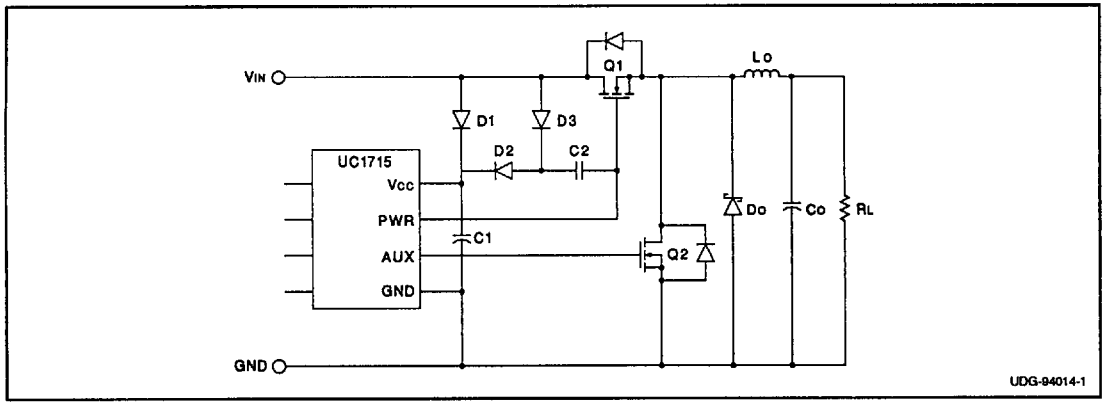


Figure 5. Synchronous Rectifier Application with a Charge Pump to Drive the High-Side N-Channel Buck Switch. VIN is Limited to 10V as Vcc will Rise to Approximately 2VIN.

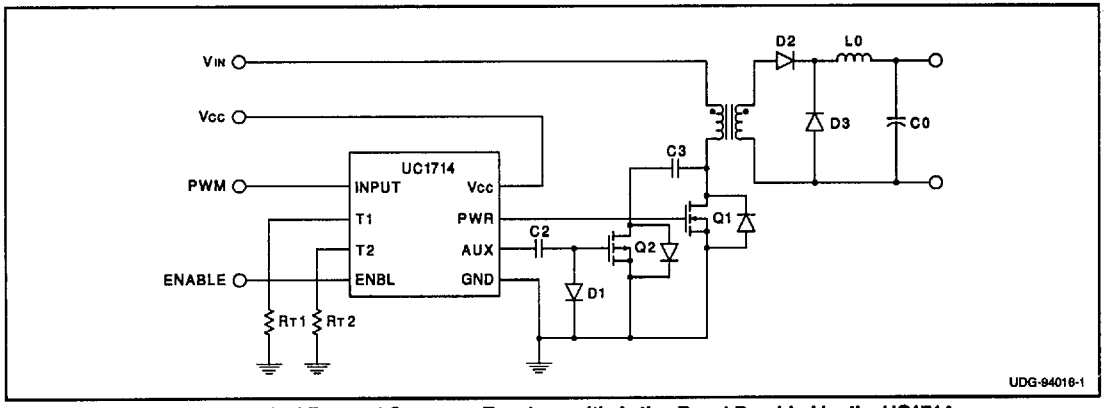


Figure 6. Typical Forward Converter Topology with Active Reset Provided by the UC1714 and a P-Channel Auxilliary Switch

TYPICAL APPLICATIONS (cont.)

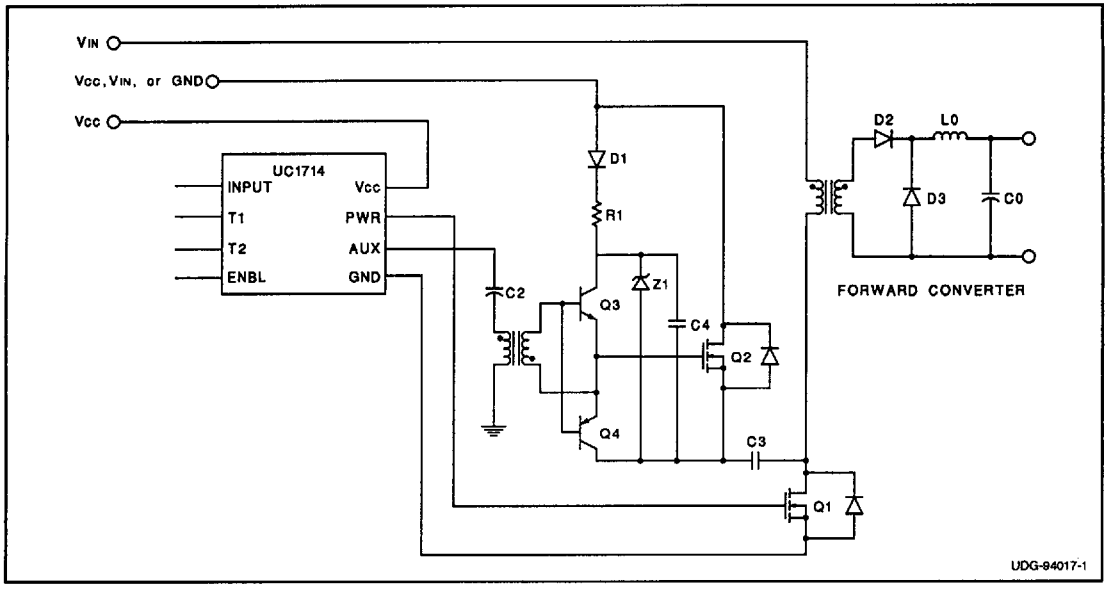


Figure 7. Using an N-Channel Active Reset Switch with a Floating Drive Command

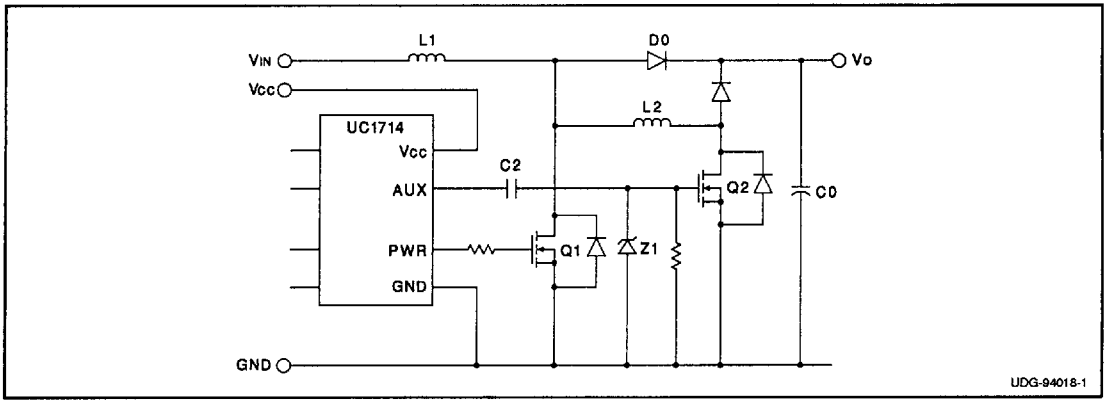


Figure 8. Zero-Voltage Turn-on of the Power Switch in a Boost Topology

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