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T-51-10-08

ADC0808/ADC0809

# ADC0808/ADC0809 8-Bit $\mu$ P Compatible A/D Converters with 8-Channel Multiplexer

## General Description

The ADC0808, ADC0809 data acquisition component is a monolithic CMOS device with an 8-bit analog-to-digital converter, 8-channel multiplexer and microprocessor compatible control logic. The 8-bit A/D converter uses successive approximation as the conversion technique. The converter features a high impedance chopper stabilized comparator, a 256R voltage divider with analog switch tree and a successive approximation register. The 8-channel multiplexer can directly access any of 8-single-ended analog signals.

The device eliminates the need for external zero and full-scale adjustments. Easy interfacing to microprocessors is provided by the latched and decoded multiplexer address inputs and latched TTL TRI-STATE® outputs.

The design of the ADC0808, ADC0809 has been optimized by incorporating the most desirable aspects of several A/D conversion techniques. The ADC0808, ADC0809 offers high speed, high accuracy, minimal temperature dependence, excellent long-term accuracy and repeatability, and consumes minimal power. These features make this device ideally suited to applications from process and machine control to consumer and automotive applications. For 16-channel multiplexer with common output (sample/hold port) see ADC0816 data sheet. (See AN-247 for more information.)

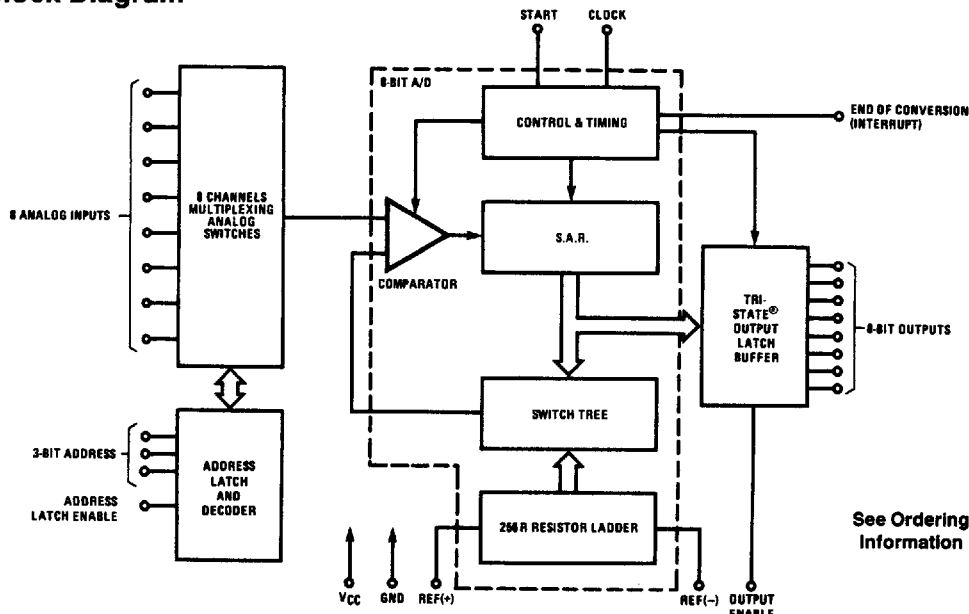
## Features

- Easy interface to all microprocessors
- Operates ratiometrically or with 5 V<sub>DC</sub> or analog span adjusted voltage reference
- No zero or full-scale adjust required
- 8-channel multiplexer with address logic
- 0V to 5V input range with single 5V power supply
- Outputs meet TTL voltage level specifications
- Standard hermetic or molded 28-pin DIP package
- 28-pin molded chip carrier package
- ADC0808 equivalent to MM74C949
- ADC0809 equivalent to MM74C949-1

## Key Specifications

- |                          |                               |
|--------------------------|-------------------------------|
| ■ Resolution             | 8 Bits                        |
| ■ Total Unadjusted Error | $\pm 1/2$ LSB and $\pm 1$ LSB |
| ■ Single Supply          | 5 V <sub>DC</sub>             |
| ■ Low Power              | 15 mW                         |
| ■ Conversion Time        | 100 $\mu$ s                   |

## Block Diagram



See Ordering Information

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**Absolute Maximum Ratings** (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ ) (Note 3)	6.5V
Voltage at Any Pin	-0.3V to ( $V_{CC} + 0.3V$ )
Except Control Inputs	
Voltage at Control Inputs	-0.3V to +15V
(START, OE, CLOCK, ALE, ADD A, ADD B, ADD C)	
Storage Temperature Range	-65°C to +150°C
Package Dissipation at $T_A = 25^\circ\text{C}$	875 mW
Lead Temp. (Soldering, 10 seconds)	
Dual-In-Line Package (plastic)	260°C
Dual-In-Line Package (ceramic)	300°C
Molded Chip Carrier Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
ESD Susceptibility (Note 11)	400V

**Operating Conditions** (Notes 1 & 2)

Temperature Range (Note 1)	$T_{MIN} \leq T_A \leq T_{MAX}$
ADC0808CJ	$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$
ADC0808CCJ, ADC0808CCN,	
ADC0809CCN	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$
ADC0808CCV, ADC0809CCV	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$
Range of $V_{CC}$ (Note 1)	$4.5 V_{DC} \text{ to } 6.0 V_{DC}$

**Electrical Characteristics**

**Converter Specifications:**  $V_{CC} = 5$   $V_{DC} = V_{REF+}$ ,  $V_{REF(-)} = \text{GND}$ ,  $T_{MIN} \leq T_A \leq T_{MAX}$  and  $f_{CLK} = 640$  kHz unless otherwise stated.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	ADC0808 Total Unadjusted Error (Note 5)	25°C $T_{MIN}$ to $T_{MAX}$			$\pm 1/2$ $\pm 3/4$	LSB LSB
	ADC0809 Total Unadjusted Error (Note 5)	0°C to 70°C $T_{MIN}$ to $T_{MAX}$			$\pm 1$ $\pm 1 1/4$	LSB LSB
	Input Resistance	From Ref(+) to Ref(-)	1.0	2.5		k $\Omega$
	Analog Input Voltage Range	(Note 4) V(+) or V(-)	GND-0.10		$V_{CC} + 0.10$	$V_{DC}$
$V_{REF(+)}$	Voltage, Top of Ladder	Measured at Ref(+)		$V_{CC}$	$V_{CC} + 0.1$	V
$\frac{V_{REF(+)} + V_{REF(-)}}{2}$	Voltage, Center of Ladder		$V_{CC}/2 - 0.1$	$V_{CC}/2$	$V_{CC}/2 + 0.1$	V
$V_{REF(-)}$	Voltage, Bottom of Ladder	Measured at Ref(-)	-0.1	0		V
$I_{IN}$	Comparator Input Current	$f_c = 640$ kHz, (Note 6)	-2	$\pm 0.5$	2	$\mu\text{A}$

**Electrical Characteristics**

**Digital Levels and DC Specifications:** ADC0808CJ  $4.5V \leq V_{CC} \leq 5.5V$ ,  $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$  unless otherwise noted  
ADC0808CCJ, ADC0808CCN, ADC0808CCV, ADC0809CCN and ADC0809CCV,  $4.75 \leq V_{CC} \leq 5.25V$ ,  $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>ANALOG MULTIPLEXER</b>						
$I_{OFF(+)}$	OFF Channel Leakage Current	$V_{CC} = 5V$ , $V_{IN} = 5V$ , $T_A = 25^\circ\text{C}$ $T_{MIN}$ to $T_{MAX}$		10	200 1.0	nA $\mu\text{A}$
$I_{OFF(-)}$	OFF Channel Leakage Current	$V_{CC} = 5V$ , $V_{IN} = 0$ , $T_A = 25^\circ\text{C}$ $T_{MIN}$ to $T_{MAX}$	-200 -1.0	-10		nA $\mu\text{A}$

**Electrical Characteristics** (Continued)

**Digital Levels and DC Specifications:** ADC0808CJ,  $4.5V \leq V_{CC} \leq 5.5V$ ,  $-55^{\circ}C \leq T_A \leq +125^{\circ}C$  unless otherwise noted  
 ADC0808CCJ, ADC0808CCN, ADC0808CCV, ADC0809CCN and ADC0809CCV,  $4.75 \leq V_{CC} \leq 5.25V$ ,  $-40^{\circ}C \leq T_A \leq +85^{\circ}C$  unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>CONTROL INPUTS</b>						
$V_{IN(1)}$	Logical "1" Input Voltage		$V_{CC} - 1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage				1.5	V
$I_{IN(1)}$	Logical "1" Input Current (The Control Inputs)	$V_{IN} = 15V$			1.0	$\mu A$
$I_{IN(0)}$	Logical "0" Input Current (The Control Inputs)	$V_{IN} = 0$	-1.0			$\mu A$
$I_{CC}$	Supply Current	$f_{CLK} = 640 \text{ kHz}$		0.3	3.0	mA
<b>DATA OUTPUTS AND EOC (INTERRUPT)</b>						
$V_{OUT(1)}$	Logical "1" Output Voltage	$I_O = -360 \mu A$	$V_{CC} - 0.4$			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$I_O = 1.6 \text{ mA}$			0.45	V
$V_{OUT(0)}$	Logical "0" Output Voltage EOC	$I_O = 1.2 \text{ mA}$			0.45	V
$I_{OUT}$	TRI-STATE Output Current	$V_O = 5V$ $V_O = 0$	-3		3	$\mu A$ $\mu A$

**Electrical Characteristics**

**Timing Specifications**  $V_{CC} = V_{REF(+)} = 5V$ ,  $V_{REF(-)} = GND$ ,  $t_r = t_f = 20 \text{ ns}$  and  $T_A = 25^{\circ}C$  unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{WS}$	Minimum Start Pulse Width	(Figure 5)		100	200	ns
$t_{WALE}$	Minimum ALE Pulse Width	(Figure 5)		100	200	ns
$t_s$	Minimum Address Set-Up Time	(Figure 5)		25	50	ns
$t_H$	Minimum Address Hold Time	(Figure 5)		25	50	ns
$t_D$	Analog MUX Delay Time From ALE	$R_S = 0\Omega$ (Figure 5)		1	2.5	$\mu S$
$t_{H1}, t_{H0}$	OE Control to Q Logic State	$C_L = 50 \text{ pF}$ , $R_L = 10k$ (Figure 8)		125	250	ns
$t_{H1}, t_{H0}$	OE Control to Hi-Z	$C_L = 10 \text{ pF}$ , $R_L = 10k$ (Figure 8)		125	250	ns
$t_c$	Conversion Time	$f_c = 640 \text{ kHz}$ , (Figure 5) (Note 7)	90	100	116	$\mu S$
$f_c$	Clock Frequency		10	640	1280	kHz
$t_{EOC}$	EOC Delay Time	(Figure 5)	0		$8 + 2 \mu S$	Clock Periods
$C_{IN}$	Input Capacitance	At Control Inputs		10	15	pF
$C_{OUT}$	TRI-STATE Output Capacitance	At TRI-STATE Outputs, (Note 12)		10	15	pF

**Note 1:** Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

**Note 2:** All voltages are measured with respect to GND, unless otherwise specified.

**Note 3:** A zener diode exists, internally, from  $V_{CC}$  to GND and has a typical breakdown voltage of  $7 V_{DC}$ .

**Note 4:** Two on-chip diodes are tied to each analog input which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the  $V_{CC}$  supply. The spec allows 100 mV forward bias of either diode. This means that as long as the analog  $V_{IN}$  does not exceed the supply voltage by more than 100 mV, the output code will be correct. To achieve an absolute  $0V_{DC}$  to  $5V_{DC}$  input voltage range will therefore require a minimum supply voltage of  $4.900 V_{DC}$  over temperature variations, initial tolerance and loading.

**Note 5:** Total unadjusted error includes offset, full-scale, linearity, and multiplexer errors. See Figure 3. None of these A/Ds requires a zero or full-scale adjust. However, if an all zero code is desired for an analog input other than 0.0V, or if a narrow full-scale span exists (for example: 0.5V to 4.5V full-scale) the reference voltages can be adjusted to achieve this. See Figure 13.

**Note 6:** Comparator input current is a bias current into or out of the chopper stabilized comparator. The bias current varies directly with clock frequency and has little temperature dependence (Figure 6). See paragraph 4.0.

**Note 7:** The outputs of the data register are updated one clock cycle before the rising edge of EOC.

**Note 8:** Human body model, 100 pF discharged through a 1.5 k $\Omega$  resistor.

### Functional Description

**Multiplexer.** The device contains an 8-channel single-ended analog signal multiplexer. A particular input channel is selected by using the address decoder. Table I shows the input states for the address lines to select any channel. The address is latched into the decoder on the low-to-high transition of the address latch enable signal.

TABLE I

SELECTED ANALOG CHANNEL	ADDRESS LINE		
	C	B	A
IN0	L	L	L
IN1	L	L	H
IN2	L	H	L
IN3	L	H	H
IN4	H	L	L
IN5	H	L	H
IN6	H	H	L
IN7	H	H	H

### CONVERTER CHARACTERISTICS

#### The Converter

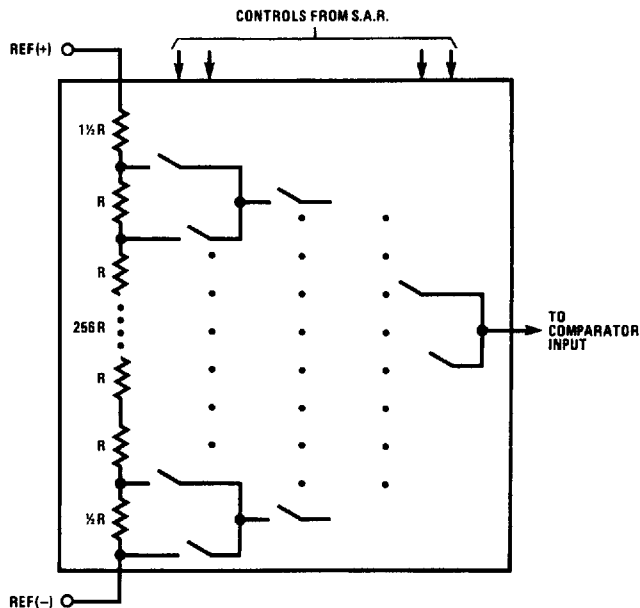
The heart of this single chip data acquisition system is its 8-bit analog-to-digital converter. The converter is designed

to give fast, accurate, and repeatable conversions over a wide range of temperatures. The converter is partitioned into 3 major sections: the 256R ladder network, the successive approximation register, and the comparator. The converter's digital outputs are positive true.

The 256R ladder network (*Figure 1*) was chosen over the conventional R/2R ladder because of its inherent monotonicity, which guarantees no missing digital codes. Monotonicity is particularly important in closed loop feedback control systems. A non-monotonic relationship can cause oscillations that will be catastrophic for the system. Additionally, the 256R network does not cause load variations on the reference voltage.

The bottom resistor and the top resistor of the ladder network in *Figure 1* are not the same value as the remainder of the network. The difference in these resistors causes the output characteristic to be symmetrical with the zero and full-scale points of the transfer curve. The first output transition occurs when the analog signal has reached + 1/2 LSB and succeeding output transitions occur every 1 LSB later up to full-scale.

The successive approximation register (SAR) performs 8 iterations to approximate the input voltage. For any SAR type converter, n-iterations are required for an n-bit converter. *Figure 2* shows a typical example of a 3-bit converter. In the ADC0808, ADC0809, the approximation technique is extended to 8 bits using the 256R network.



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FIGURE 1. Resistor Ladder and Switch Tree

### Functional Description (Continued)

The A/D converter's successive approximation register (SAR) is reset on the positive edge of the start conversion (SC) pulse. The conversion is begun on the falling edge of the start conversion pulse. The conversion is begun on the falling edge of the start conversion pulse. A conversion in process will be interrupted by receipt of a new start conversion pulse. Continuous conversion may be accomplished by tying the end-of-conversion (EOC) output to the SC input. If used in this mode, an external start conversion pulse should be applied after power up. End-of-conversion will go low between 0 and 8 clock pulses after the rising edge of start conversion. The most important section of the A/D converter is the comparator. It is this section which is responsible for the ultimate accuracy of the entire converter. It is also the

comparator drift which has the greatest influence on the repeatability of the device. A chopper-stabilized comparator provides the most effective method of satisfying all the converter requirements.

The chopper-stabilized comparator converts the DC input signal into an AC signal. This signal is then fed through a high gain AC amplifier and has the DC level restored. This technique limits the drift component of the amplifier since the drift is a DC component which is not passed by the AC amplifier. This makes the entire A/D converter extremely insensitive to temperature, long term drift and input offset errors.

Figure 4 shows a typical error curve for the ADC0808 as measured using the procedures outlined in AN-179.

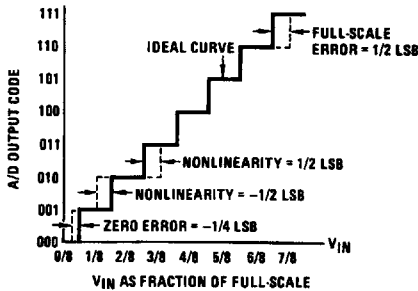


FIGURE 2. 3-Bit A/D Transfer Curve

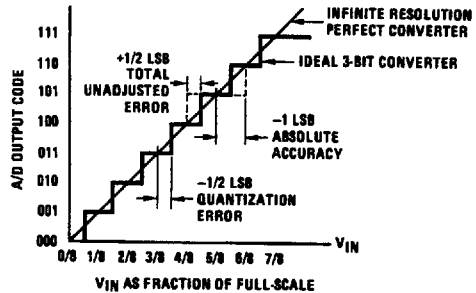


FIGURE 3. 3-Bit A/D Absolute Accuracy Curve

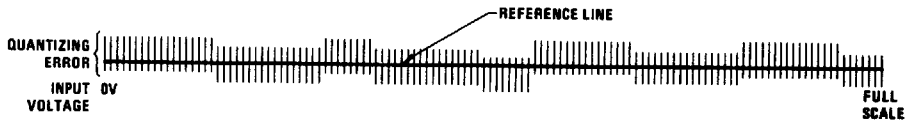


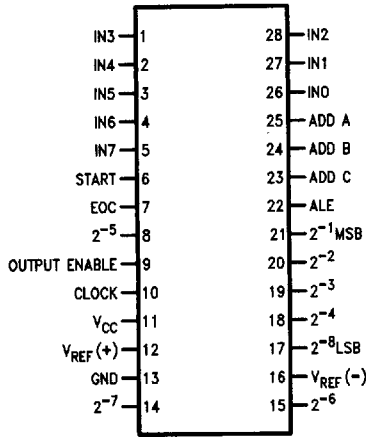
FIGURE 4. Typical Error Curve

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ADC0808/ADC0809

### Connection Diagrams

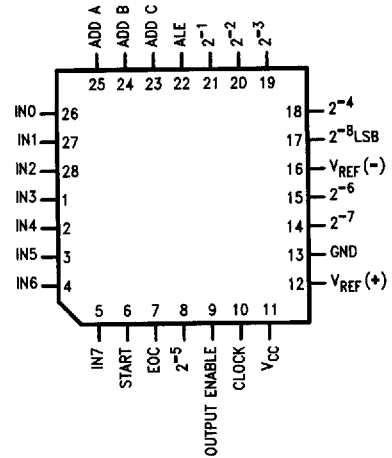
Dual-In-Line Package



TL/H/5672-11

Order Number ADC0808CCN, ADC0809CCN,  
ADC0808CCJ or ADC0808CJ  
See NS Package J28A or N28A

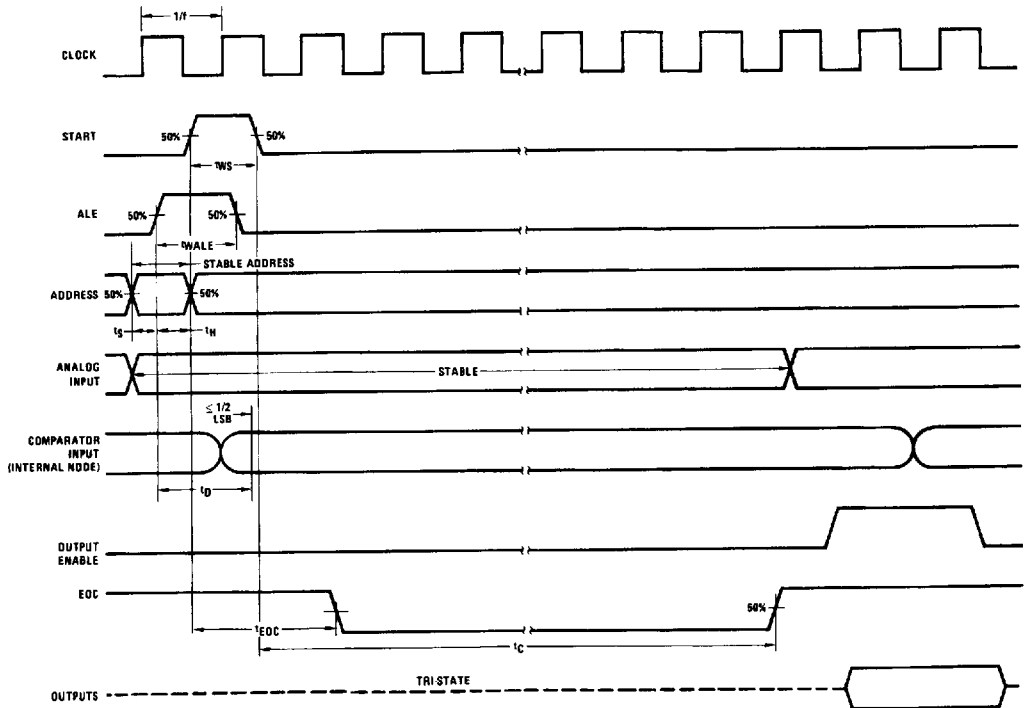
Molded Chip Carrier Package



TL/H/5672-12

Order Number ADC0808CCV or ADC0809CCV  
See NS Package V28A

### Timing Diagram



TL/H/5672-4

FIGURE 5

### Typical Performance Characteristics

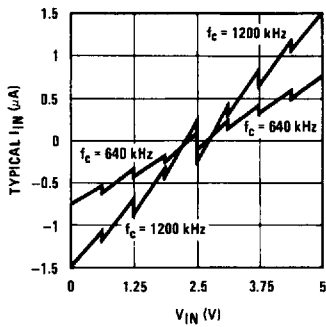


FIGURE 6. Comparator  $I_{IN}$  vs  $V_{IN}$  ( $V_{CC} = V_{REF} = 5V$ )

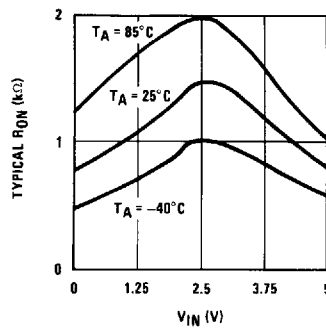
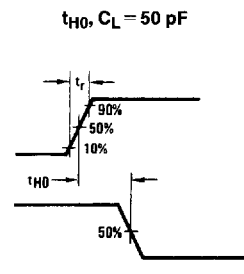
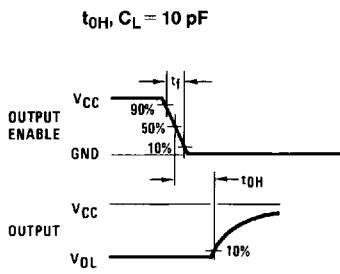
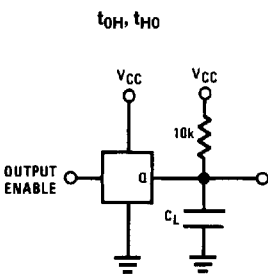
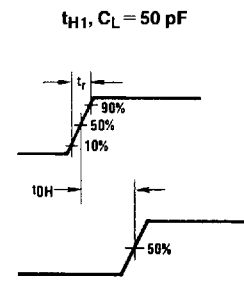
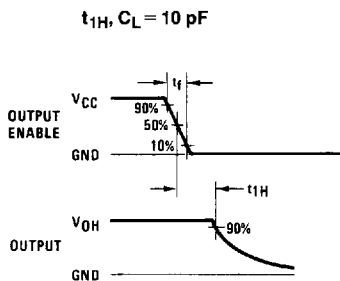
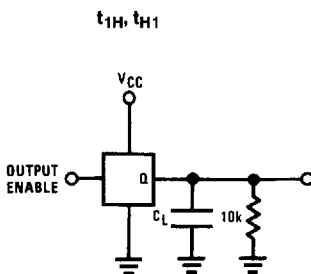


FIGURE 7. Multiplexer  $R_{ON}$  vs  $V_{IN}$  ( $V_{CC} = V_{REF} = 5V$ )

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### TRI-STATE Test Circuits and Timing Diagrams



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FIGURE 8

## Applications Information

### OPERATION

#### 1.0 RATIOMETRIC CONVERSION

The ADC0808, ADC0809 is designed as a complete Data Acquisition System (DAS) for ratiometric conversion systems. In ratiometric systems, the physical variable being measured is expressed as a percentage of full-scale which is not necessarily related to an absolute standard. The voltage input to the ADC0808 is expressed by the equation

$$\frac{V_{IN}}{V_{fs} - V_Z} = \frac{D_X}{D_{MAX} - D_{MIN}} \quad (1)$$

$V_{IN}$  = Input voltage into the ADC0808

$V_{fs}$  = Full-scale voltage

$V_Z$  = Zero voltage

$D_X$  = Data point being measured

$D_{MAX}$  = Maximum data limit

$D_{MIN}$  = Minimum data limit

A good example of a ratiometric transducer is a potentiometer used as a position sensor. The position of the wiper is directly proportional to the output voltage which is a ratio of the full-scale voltage across it. Since the data is represented as a proportion of full-scale, reference requirements are greatly reduced, eliminating a large source of error and cost for many applications. A major advantage of the ADC0808, ADC0809 is that the input voltage range is equal to the supply range so the transducers can be connected directly across the supply and their outputs connected directly into the multiplexer inputs, (Figure 9).

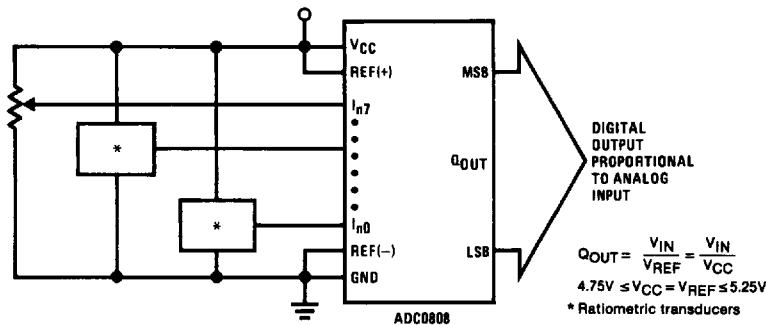
Ratiometric transducers such as potentiometers, strain gauges, thermistor bridges, pressure transducers, etc., are suitable for measuring proportional relationships; however, many types of measurements must be referred to an absolute standard such as voltage or current. This means a system reference must be used which relates the full-scale voltage to the standard volt. For example, if  $V_{CC} = V_{REF} = 5.12V$ , then the full-scale range is divided into 256 standard steps. The smallest standard step is 1 LSB which is then 20 mV.

#### 2.0 RESISTOR LADDER LIMITATIONS

The voltages from the resistor ladder are compared to the selected into 8 times in a conversion. These voltages are coupled to the comparator via an analog switch tree which is referenced to the supply. The voltages at the top, center and bottom of the ladder must be controlled to maintain proper operation.

The top of the ladder, Ref(+), should not be more positive than the supply, and the bottom of the ladder, Ref(-), should not be more negative than ground. The center of the ladder voltage must also be near the center of the supply because the analog switch tree changes from N-channel switches to P-channel switches. These limitations are automatically satisfied in ratiometric systems and can be easily met in ground referenced systems.

Figure 10 shows a ground referenced system with a separate supply and reference. In this system, the supply must be trimmed to match the reference voltage. For instance, if a 5.12V is used, the supply should be adjusted to the same voltage within 0.1V.



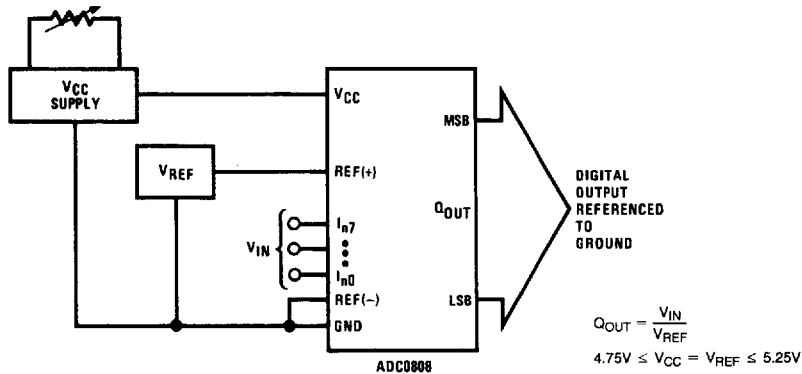
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FIGURE 9. Ratiometric Conversion System

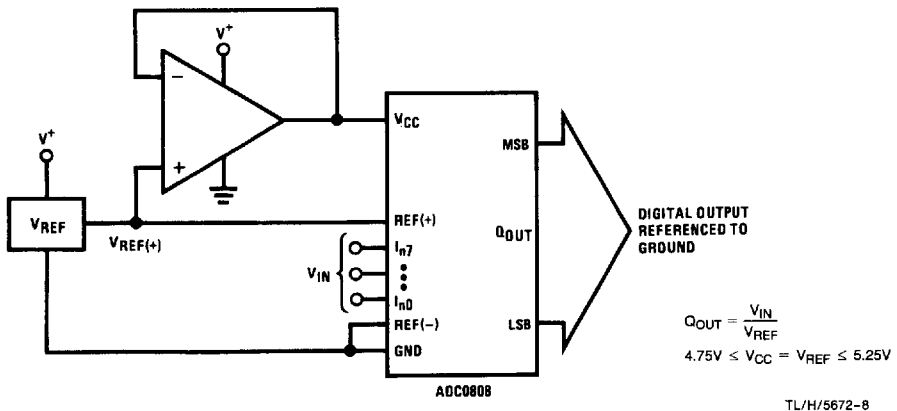
**Applications Information** (Continued)

The ADC0808 needs less than a milliamp of supply current so developing the supply from the reference is readily accomplished. In Figure 11 a ground referenced system is shown which generates the supply from the reference. The buffer shown can be an op amp of sufficient drive to supply the milliamp of supply current and the desired bus drive, or if a capacitive bus is driven by the outputs a large capacitor will supply the transient supply current as seen in Figure 12. The LM301 is overcompensated to insure stability when loaded by the 10  $\mu$ F output capacitor.

The top and bottom ladder voltages cannot exceed  $V_{CC}$  and ground, respectively, but they can be symmetrically less than  $V_{CC}$  and greater than ground. The center of the ladder voltage should always be near the center of the supply. The sensitivity of the converter can be increased, (i.e., size of the LSB steps decreased) by using a symmetrical reference system. In Figure 13, a 2.5V reference is symmetrically centered about  $V_{CC}/2$  since the same current flows in identical resistors. This system with a 2.5V reference allows the LSB bit to be half the size of a 5V reference system.



**FIGURE 10. Ground Referenced Conversion System Using Trimmed Supply**

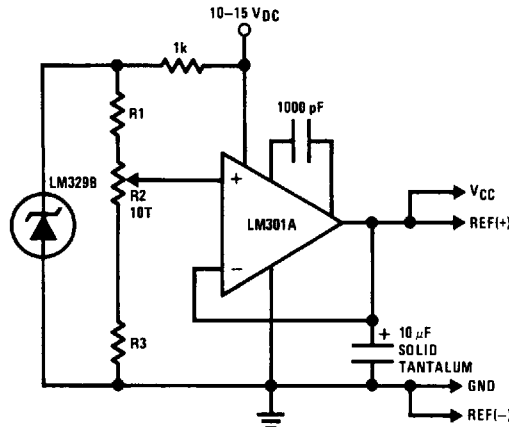


**FIGURE 11: Ground Referenced Conversion System with Reference Generating  $V_{CC}$  Supply**

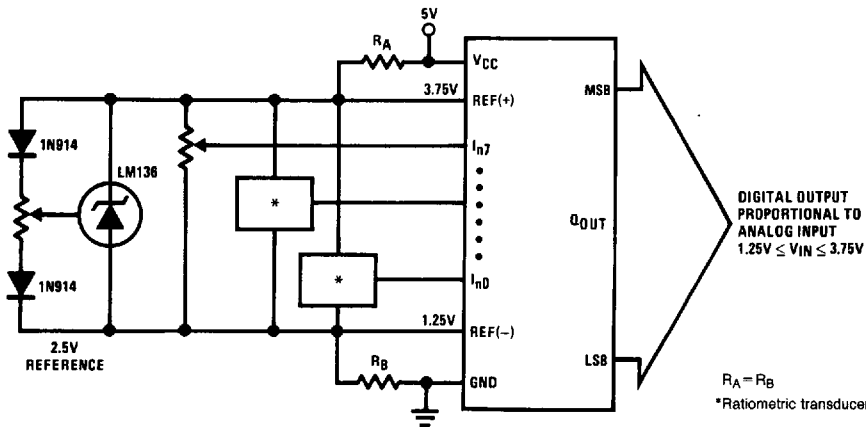
TL/H/5672-8

ADC0808/ADC0809

**Applications Information** (Continued)



**FIGURE 12. Typical Reference and Supply Circuit**



**FIGURE 13. Symmetrically Centered Reference**

TL/H/5672-9

**3.0 CONVERTER EQUATIONS**

The transition between adjacent codes N and N + 1 is given by:

$$V_{IN} = \left\{ (V_{REF(+)} - V_{REF(-)}) \left[ \frac{N}{256} + \frac{1}{512} \right] \pm VTUE \right\} + V_{REF(-)} \quad (2)$$

The center of an output code N is given by:

$$V_{IN} \left\{ (V_{REF(+)} - V_{REF(-)}) \left[ \frac{N}{256} \right] \pm VTUE \right\} + V_{REF(-)} \quad (3)$$

The output code N for an arbitrary input are the integers within the range:

$$N = \frac{V_{IN} - V_{REF(-)}}{V_{REF(+)} - V_{REF(-)}} \times 256 \pm \text{Absolute Accuracy} \quad (4)$$

where:  $V_{IN}$  = Voltage at comparator input

$V_{REF(+)}$  = Voltage at Ref(+)

$V_{REF(-)}$  = Voltage at Ref(-)

$VTUE$  = Total unadjusted error voltage (typically  $V_{REF(+)} \div 512$ )

**4.0 ANALOG COMPARATOR INPUTS**

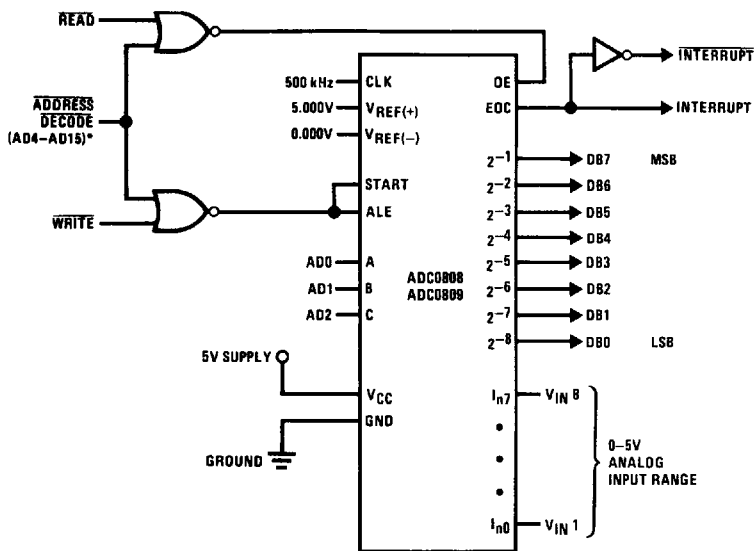
The dynamic comparator input current is caused by the periodic switching of on-chip stray capacitances. These are connected alternately to the output of the resistor ladder/switch tree network and to the comparator input as part of the operation of the chopper stabilized comparator.

The average value of the comparator input current varies directly with clock frequency and with  $V_{IN}$  as shown in Figure 6.

If no filter capacitors are used at the analog inputs and the signal source impedances are low, the comparator input current should not introduce converter errors, as the transient created by the capacitance discharge will die out before the comparator output is strobed.

If input filter capacitors are desired for noise reduction and signal conditioning they will tend to average out the dynamic comparator input current. It will then take on the characteristics of a DC bias current whose effect can be predicted conventionally.

### Typical Application



TL/H/5672-10

\*Address latches needed for 8085 and SC/MP interfacing the ADC0808 to a microprocessor

MICROPROCESSOR INTERFACE TABLE

PROCESSOR	READ	WRITE	INTERRUPT (COMMENT)
8080	MEMR	MEMW	INTR (Thru RST Circuit)
8085	RD	WR	INTR (Thru RST Circuit)
Z-80	RD	WR	INT (Thru RST Circuit, Mode 0)
SC/MP	NRDS	NWDS	SA (Thru Sense A)
6800	VMA*φ2•R/W	VMA*φ•R/W	IRQA or IRQB (Thru PIA)

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### Ordering Information

TEMPERATURE RANGE		-40°C to +85°C			-55°C to +125°C
Error	± 1/2 LSB Unadjusted	ADC0808CCN	ADC0808CCV	ADC0808CCJ	ADC0808CJ
	± 1 LSB Unadjusted	ADC0809CCN	ADC0809CCV		
Package Outline		N28A Molded DIP	V28A Molded Chip Carrier	J28A Ceramic DIP	J28A Ceramic DIP