TC74HC690AP/AF・TC74HC691AP/AF
TC74HC692AP/AF・TC74HC693AP/AF

SYNCHRONOUS PRESETTABLE 4-BIT COUNTER WITH OUTPUT REGISTER
(MULTIPLEXED 3-STATE OUTPUTS)

TC74HC690AP/AF DECADE, ASYNCHRONOUS CLEAR
TC74HC691AP/AF BINARY, ASYNCHRONOUS CLEAR
TC74HC692AP/AF DECADE, SYNCHRONOUS CLEAR
TC74HC693AP/AF BINARY, SYNCHRONOUS CLEAR

The TC74HC690A-693A is a high speed CMOS COUNTER/REGISTER fabricated with silicon gate C²MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

690A/692A are BCD DECADE COUNTER, 691A/693A are 4-BIT BINARY COUNTER, these devices have registers respectively.

If the LOAD input ($\overline{LOAD}$) is held low, DATA input (A-D) are loaded in internal counter on the positive edge of the counter clock input (CCK). In counter mode, the internal counter counts up on the positive edge of counter clock. Counter clear input ($\overline{CCLR}$) is active low. The counter clear function of the 692A/693A is synchronous to CCK, while the 690A/691A are cleared asynchronously.

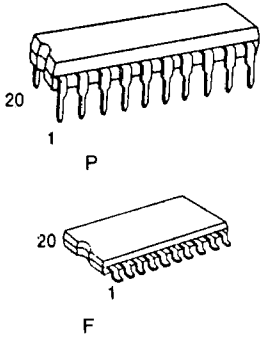
The internal counter's outputs are stored in the output register on the positive edge of register clock (RCK). Register clear ($\overline{RCLR}$) is active low. The register clear function of the 692A/693A is synchronous to RCK, while the 690A/691A are cleared asynchronously. At this point, internal counter outputs do not change. The outputs (QA-QD) are selected from the internal counter outputs or register outputs by output select ($R/\overline{C}$).

Two enable inputs(ENT and ENP) and carry output(RCO) are provided to enable easy cascading of counters without using external gate.

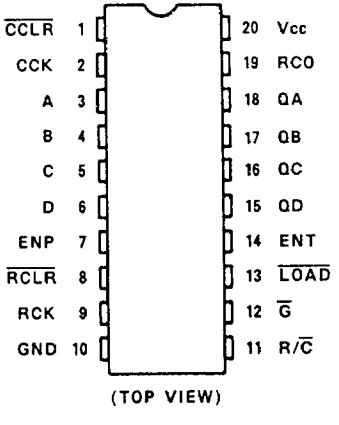
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

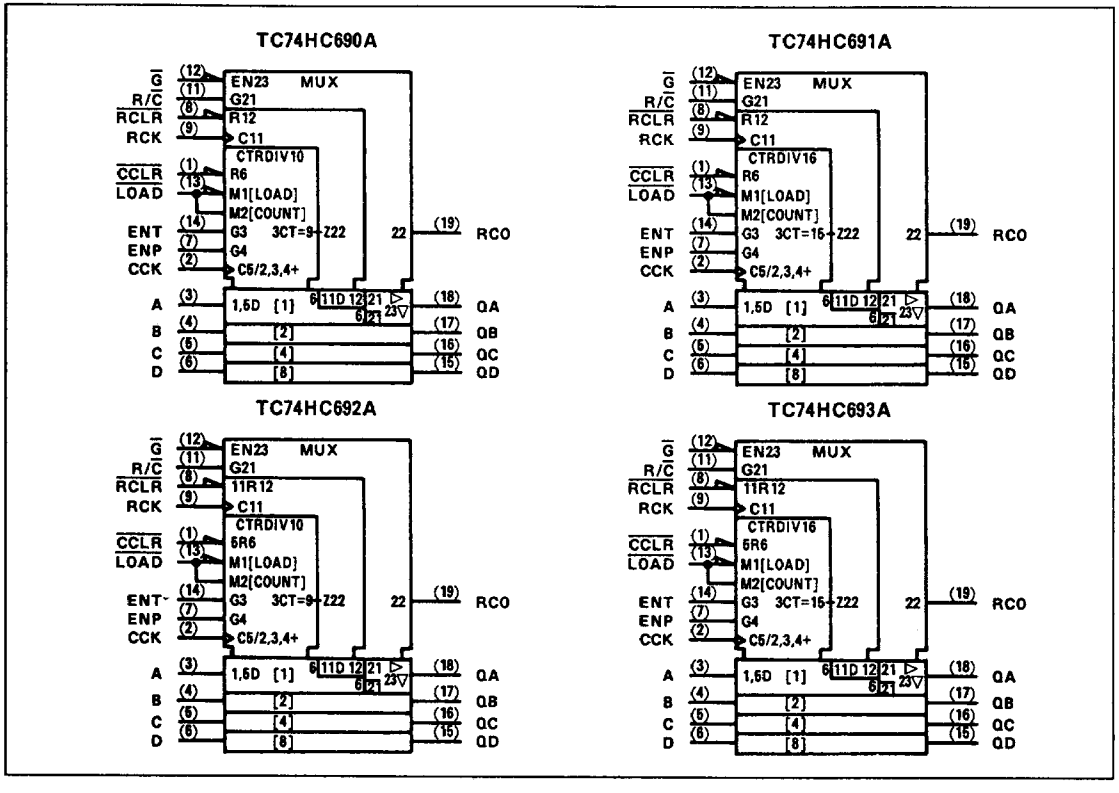
- High Speed ····· f_{MAX}=63MHz(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ····· 15 LSTTL Loads For QA~QD
  10 LSTTL Loads For RCO
- Symmetrical Output Impedance ····· $|I_{OH}|=I_{OL}$=6mA(Min.)
  For QA~QH
  $|I_{OH}|=I_{OL}$=4mA(Min.)
  For RCO
- Balanced Propaation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ····· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS690-693



ピン接続図



IEC LOGIC SYMBOL



INPUTS											OUTPUTS				FUNCTION
					690A/691A		692A/693A								
$\overline{CCLR}$	$\overline{LOAD}$	ENP	ENT	$\overline{RCLR}$	CCK	RCK	CCK	RCK	R/$\overline{C}$	$\overline{G}$	QA	QB	QC	CD	
X	X	X	X	X	X	X	X	X	X	H	Z	Z	Z	Z	HIGH IMPEDANCE
L	X	X	X	X	X	X	↓	X	L	L	L	L	L	L	COUNTER CLEAR
H	L	X	X	X	↓	X	↓	X	L	L	a	b	c	d	LOAD DATA
H	H	L	X	X	↓	X	↓	X	L	L	NO CHANGE				COUNT DISABLE
H	H	X	L	X	↓	X	↓	X	L	L					NO CHANGE
H	H	H	H	X	↓	X	↓	X	L	L	COUNT UP				COUNT UP
H	X	X	X	X	↑	X	↑	X	L	L	NO CHANGE				NO COUNT
X	X	X	X	L	X	X	X	↓	H	L	L	L	L	L	REGISTER CLEAR
X	X	X	X	H	X	↓	X	↓	H	L	a'	b'	c'	d'	LOAD REGISTER
X	X	X	X	X	X	↑	X	↑	H	L	NO CHANGE				NO CHANGE

X : DON'T CARE

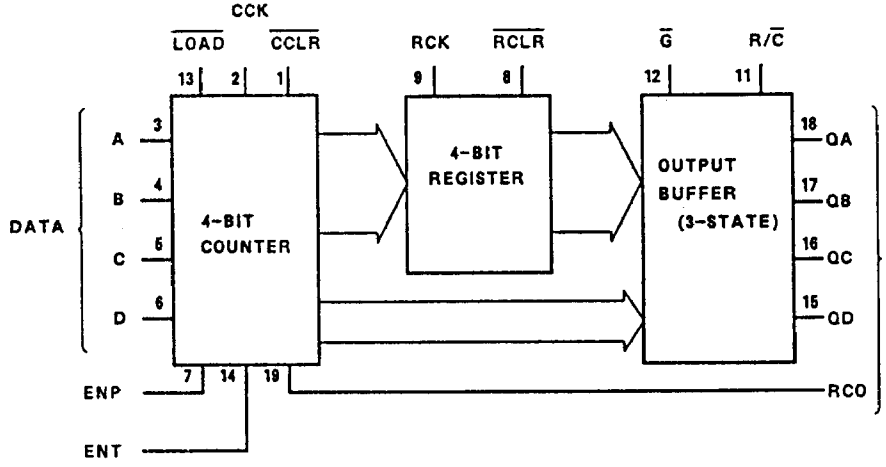
Z : High Impedance

a ~ d : The level of steady state input voltage at inputs A ~ D respectively.

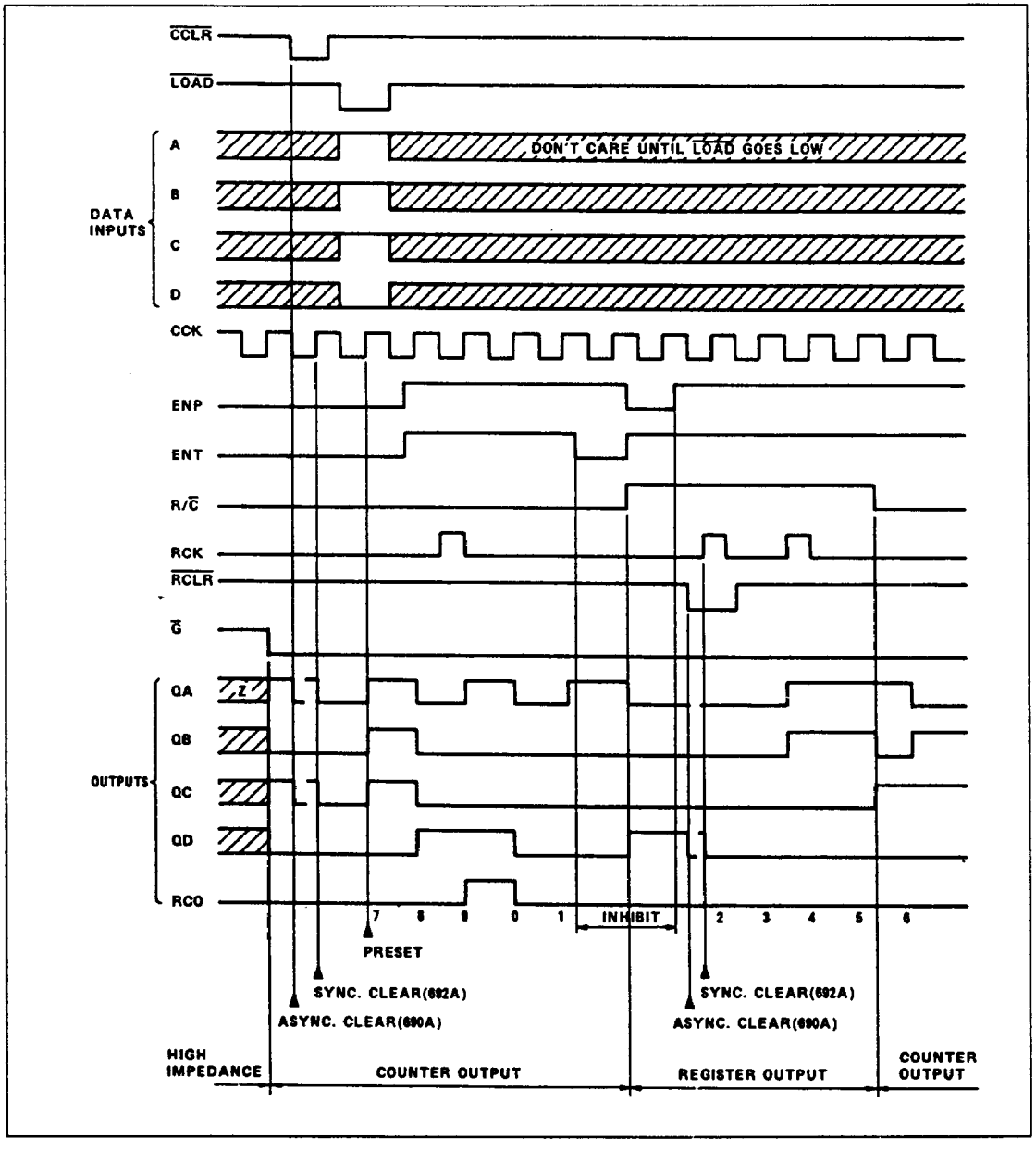
a' ~ d' : The level of internal counter outputs respectively, before the most recent postive edge of the register clock.

HC690A/692A ; RCO=QA • QD • ENT

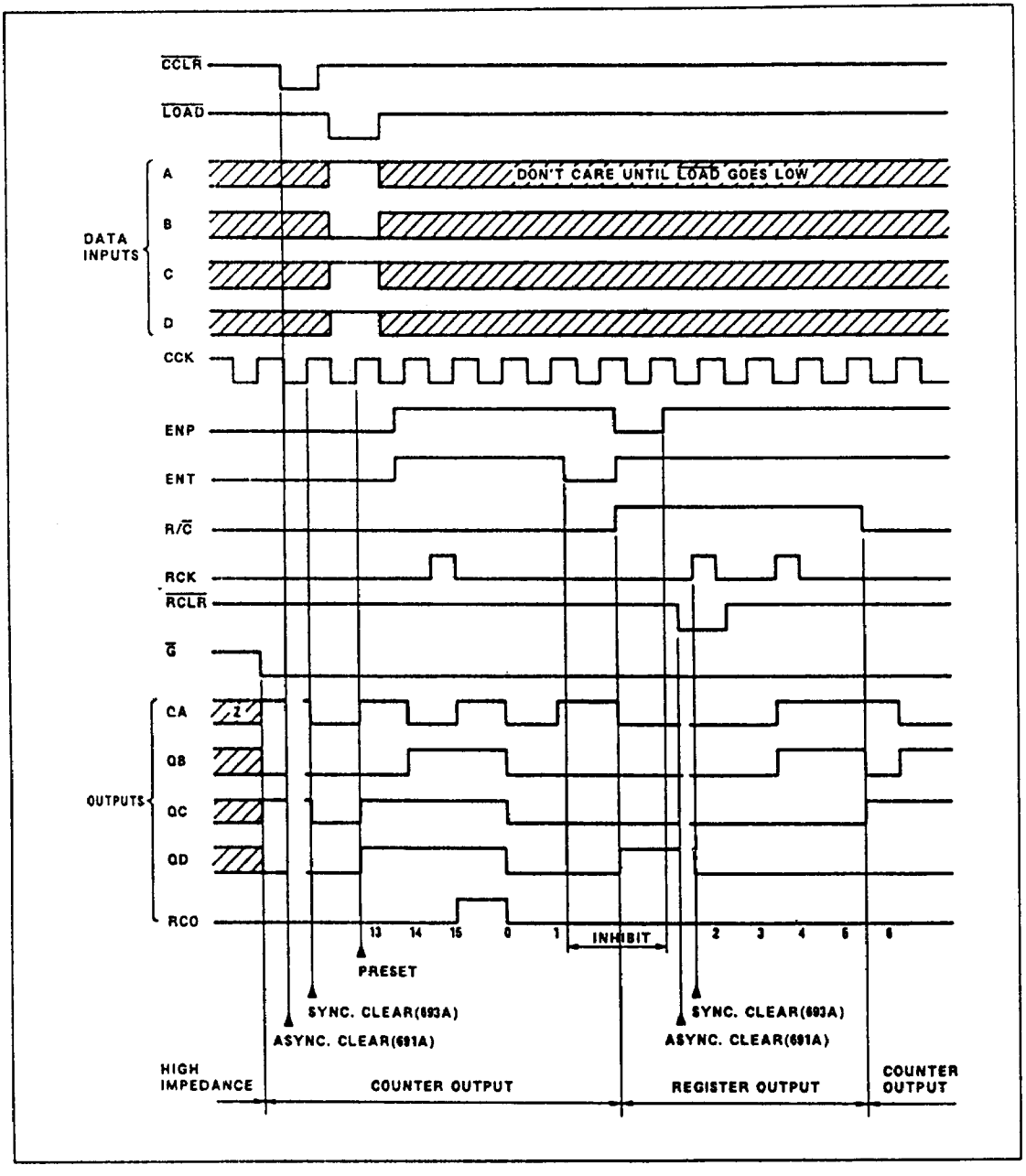
HC691A/693A ; RCO=QA • QB • QC • QD • ENT



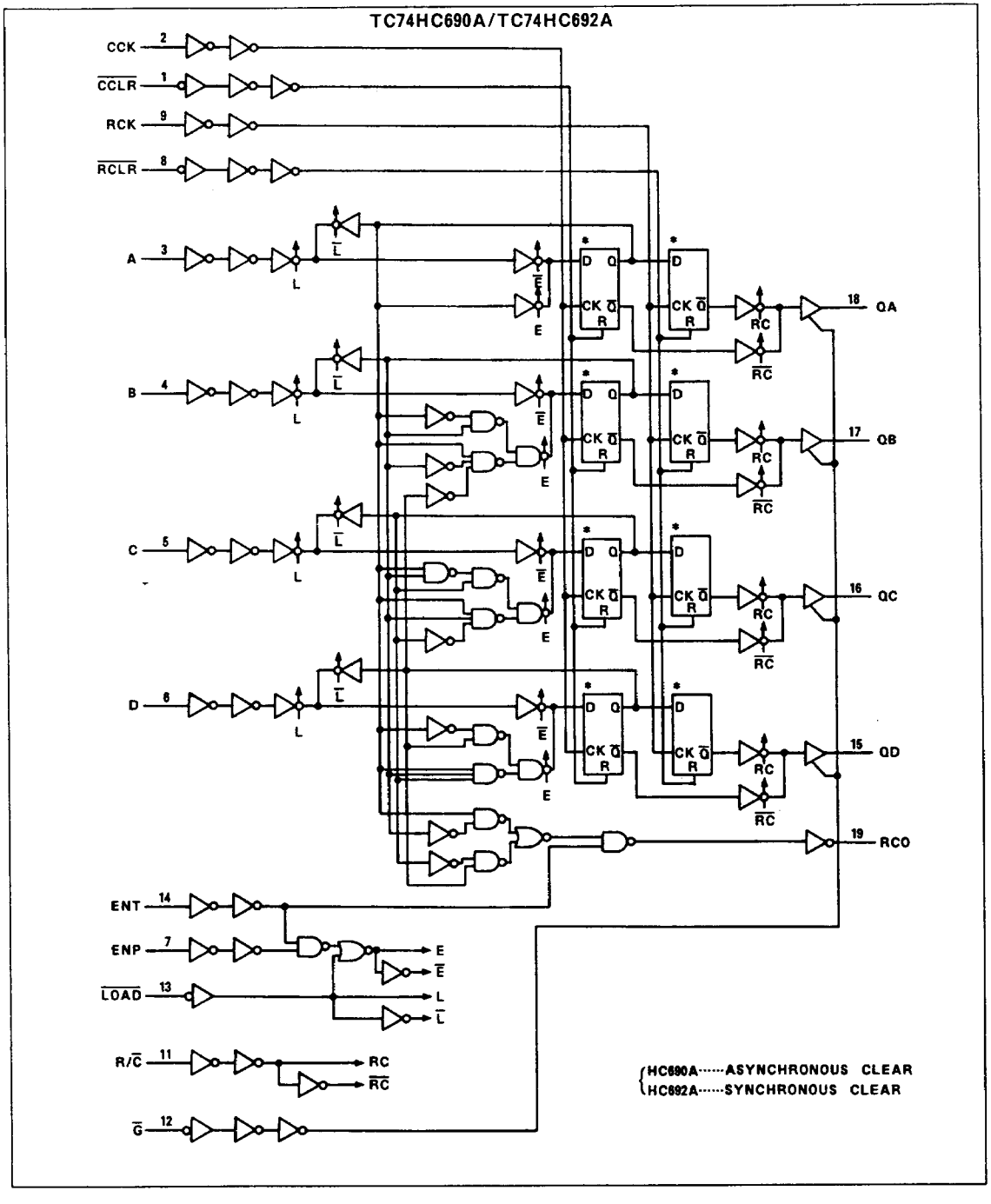
TIMING CHART (TC74HC690A/692A ; DECADE COUNTER)



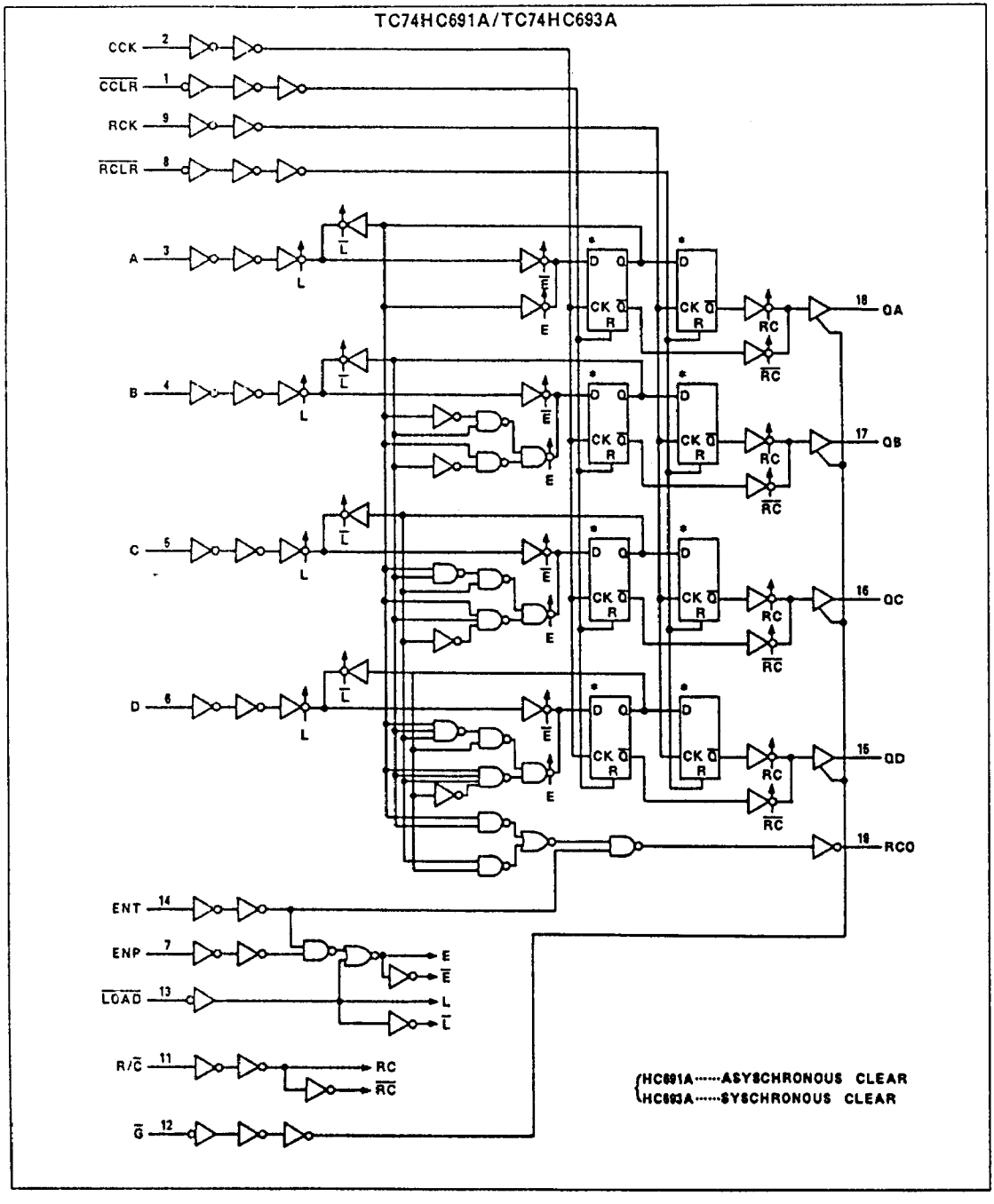
TIMING CHART (TC74HC691A/693A ; BINARY COUNTER)



SYSTEM DIAGRAM



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current (RCO) / ($Q_A \sim Q_H$)	I_{OUT}	± 25 / ± 35	mA
DC V_{CC}/Ground Current	I_{CC}	± 75	mA
Power Dissipation	P_D	500(DIP)*/180(SOIC)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃～ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	℃
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000$(V_{CC}=2.0V) $0 \sim 500$(V_{CC}=4.5V) $0 \sim 400$(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION			V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ～85℃ MIN.	Ta=−40 ～85℃ MAX.	UNIT
High-Level Input Voltage	V_{IH}				2.0	1.5	–	–	1.5	–	V
					4.5	3.15	–	–	3.15	–	
					6.0	4.2	–	–	4.2	–	
Low-Level Input Voltage	V_{IL}				2.0	–	–	0.5	–	0.5	V
					4.5	–	–	1.35	–	1.35	
					6.0	–	–	1.8	–	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}		I_{OH} =−20 μA	2.0	1.9	2.0	–	1.9	–	V
					4.5	4.4	4.5	–	4.4	–	
					6.0	5.9	6.0	–	5.9	–	
			RCO	I_{OH} =−4 mA	4.5	4.18	4.31	–	4.13	–	
				I_{OH} =−5.2mA	6.0	5.68	5.80	–	5.63	–	
			$Q_A \sim Q_H$	I_{OH} =−6 mA	4.5	4.18	4.31	–	4.31	–	
				I_{OH} =−7.8mA	6.0	5.68	5.80	–	5.63	–	
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}		I_{OL} =20 μA	2.0	–	0.0	0.1	–	0.1	V
					4.5	–	0.0	0.1	–	0.1	
					6.0	–	0.0	0.1	–	0.1	
			RCO	I_{OL} =4 mA	4.5	–	0.17	0.26	–	0.33	
				I_{OL} =5.2mA	6.0	–	0.18	0.26	–	0.33	
			$Q_A \sim Q_H$	I_{OL} =6 mA	4.5	–	0.17	0.26	–	0.33	
				I_{OL} =7.8mA	6.0	–	0.18	0.26	–	0.33	
3-State Output Off-State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND			6.0	–	–	±0.5	–	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND			6.0	–	–	±0.1	–	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND			6.0	–	–	4.0	–	40.0	

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ～85℃ LIMIT	UNIT
Minimum Pulse Width (CK)	$t_{W(H)}$ $t_{W(L)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	12	15	
Minimum Pulse Width ($\overline{CCLR}$,RCLR) *	$t_{W(L)}$		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	12	15	
Minimum Set-up Time ($\overline{CCLR}$,RCLR) **	t_s		2.0	−	100	125	
			4.5	−	20	25	
			6.0	−	16	20	
Minimum Set-up Time ($\overline{LOAD}$,ENT,ENP)	t_s		2.0	−	150	190	
			4.5	−	30	38	
			6.0	−	24	25	
Minimum Set-up Time (A,B,C,D)	t_s		2.0	−	125	155	
			4.5	−	25	31	
			6.0	−	20	25	
Minimum Set-up Time (CCK-RCK)	t_s		2.0	−	125	155	
			4.5	−	25	31	
			6.0	−	20	25	
Minimum Hold Time	t_h		2.0	−	0	0	
			4.5	−	0	0	
			6.0	−	0	0	
Minimum Removal Time *	trem		2.0	−	50	65	
			4.5	−	10	13	
			6.0	−	8	10	
Clock Frequency	f		2.0	−	4	3.5	MHz
			4.5	−	22	18	
			6.0	−	26	21	

AC ELECTRICAL CHARACTERISTICS(C_L =15pF,V_{CC}=5V,Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time (RCO)	t_{TLH} t_{THL}		−	4	8	ns
Propagation Delay Time (CCK-RCO)	t_{pLH} t_{pHL}		−	18	32	
Propagation Delay Time (ENT-RCO)	t_{pLH} t_{pHL}		−	8	15	
Propagation Delay Time ($\overline{CCLR}$-RCO) *	t_{pHL}		−	19	34	
Maximum Clock Frequency	f_{MAX}		24	63	−	MHz

*: for TC74HC690A/691A only

**: for TC74HC692A/693A only

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	CL	V_{CC}	Ta=25℃ MIN.	TYP.	MAX.	Ta=−40 ~85℃ MIN.	MAX.	UNIT
Output Transition Time (Q)	t_{TLH} t_{THL}		50	2.0	−	25	60	−	75	ns
				4.5	−	7	12	−	15	
				6.0	−	6	10	−	13	
Output Transition Time (RCO)	t_{TLH} t_{THL}		50	2.0	−	30	75	−	95	
				4.5	−	8	15	−	19	
				6.0	−	7	13	−	16	
Propagation Delay Time (CCK−Q)	t_{pLH} t_{pHL}		50	2.0	−	84	215	−	270	
				4.5	−	27	43	−	54	
				6.0	−	22	34	−	43	
			150	2.0	−	99	255	−	320	
				4.5	−	32	51	−	64	
				6.0	−	26	41	−	51	
Propagation Delay Time (RCK−Q)	t_{pLH} t_{pHL}		50	2.0	−	84	215	−	270	
				4.5	−	28	43	−	54	
				6.0	−	22	34	−	43	
			150	2.0	−	99	255	−	320	
				4.5	−	33	51	−	64	
				6.0	−	26	41	−	51	
Propagation Delay Time (R/$\overline{C}$−Q)	t_{pLH} t_{pHL}		50	2.0	−	63	170	−	215	
				4.5	−	21	34	−	43	
				6.0	−	17	27	−	34	
			150	2.0	−	78	210	−	265	
				4.5	−	26	42	−	53	
				6.0	−	21	34	−	42	
Propagation Delay Time ($\overline{CCLR}$−Q) *	t_{pHL}		50	2.0	−	93	250	−	315	
				4.5	−	31	50	−	63	
				6.0	−	25	40	−	50	
			150	2.0	−	108	290	−	365	
				4.5	−	36	58	−	73	
				6.0	−	29	46	−	58	
Propagation Delay Time ($\overline{RCLR}$−Q) *	t_{pHL}		50	2.0	−	90	250	−	315	
				4.5	−	30	50	−	63	
				6.0	−	24	40	−	50	
			150	2.0	−	105	290	−	365	
				4.5	−	35	58	−	73	
				6.0	−	28	46	−	58	
Propagation Delay Time (CCK−RCO)	t_{pLH} t_{pHL}		50	2.0	−	72	185	−	230	
				4.5	−	23	37	−	46	
				6.0	−	19	30	−	37	
Propagation Delay Time (ENT−RCO)	t_{pLH} t_{pHL}		50	2.0	−	36	95	−	120	
				4.5	−	12	19	−	24	
				6.0	−	10	15	−	19	
Propagation Delay Time ($\overline{CCLR}$−RCO)*	t_{pHL}		50	2.0	−	75	195	−	245	
				4.5	−	25	39	−	49	
				6.0	−	20	31	−	39	

*: for TC74HC690A/691A only

AC ELECTRICAL CHARACTERISTICS(C_L =50pF, Input $t_r = t_f$ =6ns)

PARAMETER	SYMBOL	TEST CONDITION	CL	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Enable time ($\overline{G}$−Q)	t_{pZL} t_{pZH}	R_L =1kΩ	50	2.0	−	48	120	−	150	ns
				4.5	−	16	24	−	30	
				6.0	−	13	19	−	24	
			150	2.0	−	63	160	−	200	
				4.5	−	21	32	−	40	
				6.0	−	17	26	−	32	
Output Disable time ($\overline{G}$−Q)	t_{pLZ} t_{pHZ}	R_L =1kΩ	50	2.0	−	34	145	−	180	
				4.5	−	18	29	−	36	
				6.0	−	14	23	−	29	
Maximum Ciock Frequency	f_{MAX}		50	2.0	4	17	−	3.5	−	MHz
				4.5	22	52	−	18	−	
				6.0	26	65	−	21	−	
Input Capacitance	C_{IN}				−	5	10	−	10	pF
Output Capacitance	C_{OUT}				−	13	−	−	−	
Power Dissipation Capacitance	C_{PD} (1)				−	63	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$