



DIGITAL DELAY LINES

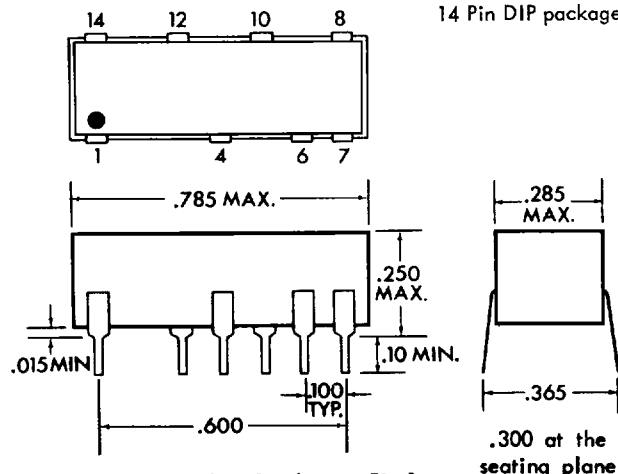
HIGH SPEED CMOS

5 TAPS • 14 PIN PACKAGE

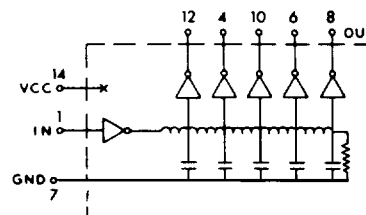
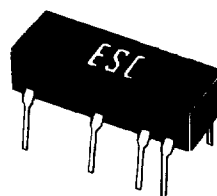
SERIES 14CMTD

This series of digital hybrid delay lines are contained in a 14 Pin DIP package using High Speed CMOS series circuits.

NOTE • NEW!
FAX NO. 201-947-0406



White Dot locates Pin 1



Intermediate delay values available upon request.

Model No.	Delay (ns)	Delay/Tap (ns)
14CMTD32	32	*5
14CMTD36	36	*6
14CMTD40	40	*7
14CMTD44	44	*8
14CMTD48	48	*9
14CMTD52	52	*10
14CMTD60	60	12
14CMTD75	75	15
14CMTD100	100	20
14CMTD125	125	25
14CMTD150	150	30
14CMTD175	175	35
14CMTD200	200	40
14CMTD250	250	50
14CMTD300	300	60
14CMTD350	350	70
14CMTD400	400	80
14CMTD420	420	84
14CMTD440	440	88
14CMTD450	450	90
14CMTD500	500	100

DC PARAMETERS		LIMITS	
		Min.	Max.
V _{oh}	V _{cc} =min I _{oh} =4.0mA	4.0V	-
V _{ol}	V _{cc} =min I _{ol} =4.0mA	-	.3V
V _{ih}	V _{cc} =min-max	2.0V	-
V _{il}	V _{cc} =min-max	-	.8V
I _L	V _{cc} =max	-	+/-1.0μA
I _{cc}	V _{cc} =max outputs low	-	15mA
max load	V _{cc} =max V _{oh} =4.0V	10 LSTTL Loads	

SPECIFICATIONS:

- Supply voltage: 5.0VDC ±10%
- Delay tolerances: ±2ns or ±5% wig
- Rise Time: 5ns max
- Minimum Pulse Width: 40% of Total Delay
- Maximum Duty Cycle: 50%
- Five equally spaced taps
- Operating temp. range: 0°C to +70°C
- Terminals: Electro tin plated alloy 42
.020w x .010th

TEST CONDITIONS:

- V_{cc}=5.0VDC, Temp. 25° ±5°C
- Time delay measured at the 1.5V level
- Rise time measured from .75V to 2.4V
- Input test pulse:
 - Pulse voltage: 3.0V
 - Pulse rise time: 2ns
 - Pulse width: 1.5 x max T_d
 - Pulse spacing: 5 x max T_d

* Residual Delay first tap -12ns, following taps are referenced to pin 12 (first tap).
 ** Also available for -55°C to +125°C operation. The dimensions will change to .82L X .40W X .36H.
 Specify Series 14CMTD when ordering.