

3 1/2-Digit A/D Converter Set

FEATURES

- Buffered Reference Input
- MOSFET Input
- Auto-Zero System
- Auto-Polarity
- Over and Under Range Signals

BENEFITS

- High Gain Stability
- Reduced Signal Loading
- Reduced Offset and Drift Over Temperature
- Reduced External Parts Count
- Easily Interfaced

APPLICATIONS

- High Performance Digital Voltmeters
- Digital Panel Meters
- Digital Instrumentation Readouts
- μ P A/D Interface Subsystem
- Auto-Zeroed Microvolt or Strain Gauge Systems

DESCRIPTION

The LD110 and LD111A form a precision 3 1/2 digit A/D converter system for use in display and microprocessor based data acquisition applications. Based on Siliconix's "Quantized Feedback" technique, intrinsic features include auto-polarity, auto-zero, and ratiometric operation. Except for a stable reference, no critical components are required to achieve rated performance. The technique used offers superior linearity, normal mode rejection, and stability due to the simultaneous integration of the unknown input and the reference voltages. Unlike other conversion techniques, the integrator output voltage never represents more than 100 counts. Thus, critical, high resolution performance is not required of either the integrator or the comparator.

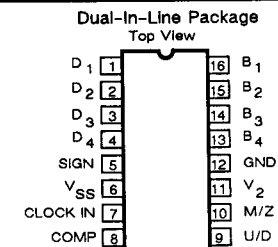
The monolithic LD111A high performance analog processor contains a bipolar comparator, a bipolar integrating amplifier, a bipolar reference amplifier, two MOSFET input unity gain amplifiers, several P-channel enhancement mode analog switches and the necessary level shifting drivers to allow the analog and digital processors to be directly interfaced. The high impedance input and reference buffer amplifiers eliminate source loading errors and provide the outstanding temperature coefficient inherent in this system. Break-before-make switch action ensures that neither the analog input nor the reference voltages will be shorted to ground at any time.

The PMOS LD110 synchronous digital processor combines the counting, storage and data multiplexing functions with the random logic necessary to control the quantized charge-balancing

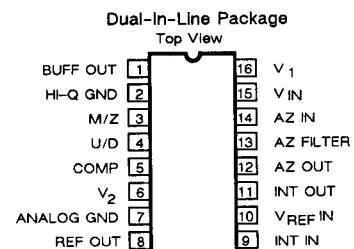
function of the analog processor. Seventeen static latches store the 3 1/2 digits of BCD data as well as overrange, underrange and polarity information. Nine push-pull output buffers (capable of driving one standard TTL load each) provide the sign, digit strobe and multiplexed BCD data outputs, all of which are active high. The digit scan is an interlaced format of digits 1, 3, 2, and 4.

Both devices are supplied in the 16-pin plastic DIP, and are specified for operation over the commercial, C suffix (0 to 70°C) temperature range.

PIN CONFIGURATION

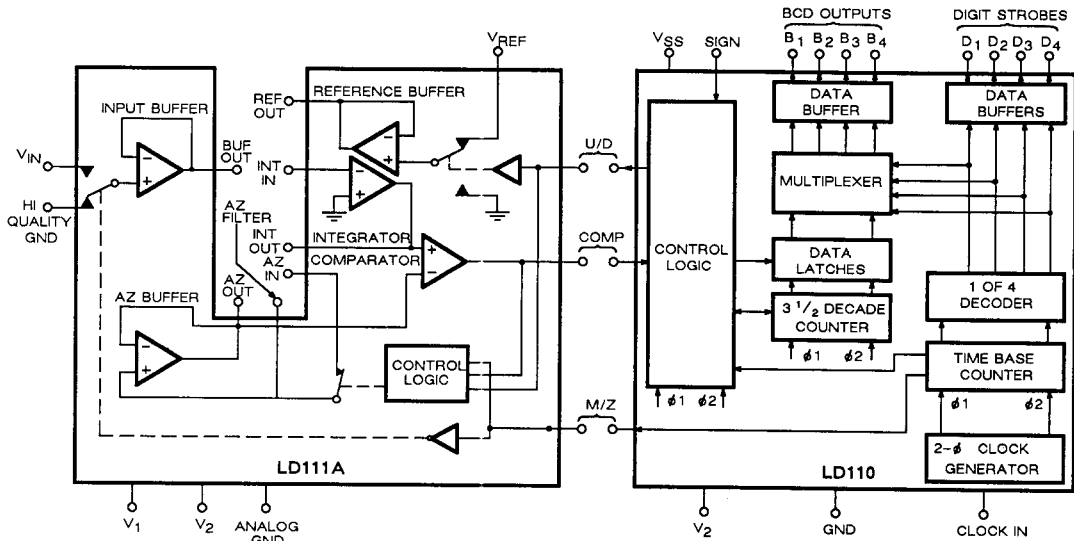


Order Number: LD110CJ



Order Number: LD111ACJ

FUNCTIONAL BLOCK DIAGRAM



SWITCH STATES ARE FOR A LOGIC "0" AT U/D AND M/Z INPUTS

ABSOLUTE MAXIMUM RATINGS

I_{IN} (Pin 15, 2)	± 1 mA
$V_1 - V_2$ (LD111A)	30 V
V_{SS}	5 V
$V_{SS} - V_2$ (LD110)	20 V
V On Any Pin Relative to V_{SS} (LD110)	0.3 V to -20 V

V_{REF}	V_1
Operating Temperature	0 to 70°C
Storage Temperature	-65 to 125°C
Power Dissipation (Package) *	750 mW

* Device mounted with all leads welded or soldered to PC Board. Derate 6.3 mW/°C above 25°C.

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ELECTRICAL CHARACTERISTICS^a

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_1 = 12$ V, $V_2 = -12$ V $V_{SS} = 5$ V $V_{REF} = 8.2$ V $R_1 = 100$ k Ω	LIMITS: $T_A = 25$ °C			UNIT
			TYP ^d	MIN ^b	MAX ^b	
SYSTEM						
Analog Input Range	V_{ANALOG}		-2	2	V	
Linearity			0.02		% rdg	
Noise		Noise apparent when going from one steady reading to another.	0.1		LSB _{p-p}	

Not Recommended for New Designs

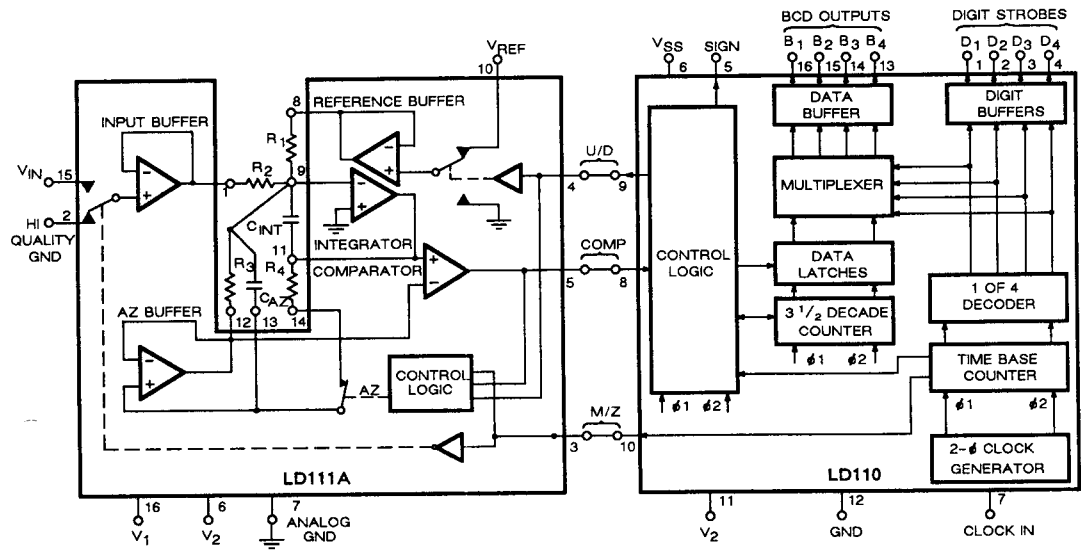
ELECTRICAL CHARACTERISTICS ^a							
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V ₁ = 12 V, V ₂ = -12 V V _{SS} = 5 V V _{REF} = 8.2 V R ₁ = 100 kΩ	LIMITS: T _A = 25 °C			UNIT	
			TYP ^d	MIN ^b	MAX ^b		
SYSTEM (Cont'd)							
Gain T.C.			5			ppm/°C	
Normal Mode Rejection	NMR	f _{NOISE} = 60 Hz	40			dB	
Clock Frequency	f _{in}	50 % Duty Cycle	30.7	2	250	kHz	
ON Resistance Auto Zero Switch	r _{DS(ON)}	V _{AZ(IN)} = -4.0 V I _S = -30 μA	6		20	kΩ	
INPUT							
Clock Input Current LOW	I _{CL}	V _{CLOCK(IN)} = 0.4 V		-500		μA	
Input Bias Current	I _{IN}		4			pA	
COMP, LD110	I _{INL}	V _{IN} = -12 V	-700	-1500	-50	μA	
AMPLIFIER							
Reference Buffer	I _{SOURCE}	V _{OUT} = 0 V	V _{INL(U/D)} = 0.8 V	-800		-400	μA
AZ Buffer	I _{SINK}		V _{AZ} = -4 V	800			
Input Buffer	I _{SINK}		V _{IN} = -2 V	800	400		
	I _{SOURCE}		V _{IN} = 2 V	-100		-50	
AZ Buffer	V _{OS}			-100	100	mV	
OUTPUT							
Measure/Zero Voltage, Low	V _{OL1}	I _{OL} = 150 μA			0.6	V	
Measure/Zero Voltage, High	V _{OH1}	I _{OH} = -200 μA		2.4			
Up/Down Logic Voltage, Low	V _{OL2}	I _{OL} = 250 μA			0.6		
Up/Down Logic Voltage, High	V _{OH2}	I _{OH} = -200 μA		2.4			
Analog Comparator Voltage	V _{OH3}	I _{OH} = -100 μA		2.4			

ELECTRICAL CHARACTERISTICS ^a						
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V ₁ = 12 V, V ₂ = -12 V V _{SS} = 5 V V _{REF} = 8.2 V R ₁ = 100 kΩ	LIMITS: T _A = 25 °C			UNIT
			TYP ^d	MIN ^b	MAX ^b	
OUTPUT (Cont'd)						
Digits, Bits Voltage, Low	V _{OL3}	I _{OL} = 1.6 mA			0.6	V
Sign Voltage, Low	V _{OL4}				0.65	
Data Bits Voltage, High	V _{OH4}	I _{OH} = -200 μA		2.4		
Digits, Sign Voltage, High	V _{OH5}	I _{OH} = -800 μA		2.4		
SUPPLY						
V ₁ Supply Current LD111A	I ₁		2.2		4	mA
V ₂ Supply Current LD111A	I _{2A}		-1.8	-4		
V ₂ Supply Current LD110	I _{2D}		-17	-23		
V _{SS} Supply Current LD110	I _{SS}		17.4		24	
Power Supply Rejection Ratio, V ₁	PSRR ₁		85	80		dB
Power Supply Rejection Ratio, V ₂	PSRR ₂		65	60		
Reference Voltage Rejection		R _{REF} = R ₂ = 100 kΩ V _{IN} = 2 V	1			% Δ rdg per Δ V _{REF}

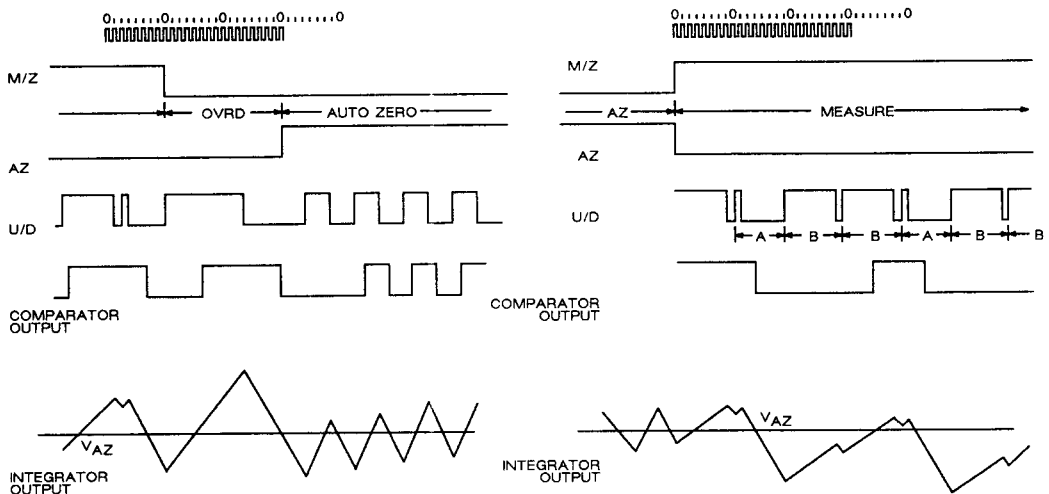
NOTES:

- Refer to PROCESS OPTION FLOWCHART for additional information.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

FUNCTIONAL OPERATION



SWITCH STATES ARE FOR A LOGIC "0" AT U/D AND M/Z INPUTS



FUNCTIONAL OPERATION (Cont'd)

