

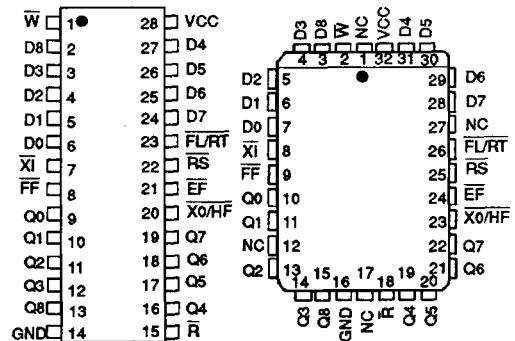
### FEATURES

- First-in, first-out memory-based architecture
- Flexible 2048 x 9 organization
- Low-power HCMOS technology
- Asynchronous and simultaneous read/write
- Bidirectional applications
- Fully expandable by word width or depth
- Empty and full warning flags
- Half-full flag capability in single-device mode
- Retransmit capability
- High performance
- Available in 50ns, 65ns, 80ns, and 120ns access times
- Industrial temperature range -40°C to +85°C available, designated N, in 50ns, 65ns, 80ns, and 120ns access.

### DESCRIPTION

The DS2011 FIFO Chip implements a first-in, first-out algorithm featuring asynchronous read/write operations, full, empty, and half-full flags, and unlimited expansion capability in both word size and depth. The DS2011 is functionally and electrically equivalent to the

### PIN ASSIGNMENT



28-Pin DIP  
(300 and 600 Mil)  
See Mech. Drawings  
Sect. 16, Pgs. 1 & 4

32-Pin PLCC  
See Mech. Drawing  
Sect. 16, Pg. 11

### PIN DESCRIPTION

$\overline{W}$	- WRITE
$\overline{R}$	- READ
$\overline{RS}$	- RESET
$\overline{FL/RT}$	- First Load/Retransmit
$D_{0-8}$	- Data In
$Q_{0-8}$	- Data Out
$\overline{XI}$	- Expansion In
$\overline{XO/HF}$	- Expansion Out/Half Full
$\overline{FF}$	- Full Flag
$\overline{EF}$	- Empty Flag
$V_{CC}$	- 5 Volts
$GND$	- Ground
$NC$	- No Connect

DS2009 512 x 9 FIFO Chip, with the exceptions listed in the notes for DC Electrical Characteristics of the DS2009 data sheet. Refer to the DS2009 data sheet for detailed device description.