TENTATIVE TOSHIBA HYBRID DIGITAL INTEGRATED CIRCUIT

4,194,304 WORDS × 64 BITS SYNCHRONOUS DRAM MODULE

DESCRIPTION

The THMY6440A1AEG is a 4,194,304 words by 64 bits Synchronous DRAM module which assembled 16 pcs of TC59S1608AFT with Unbuffer on the printed circuit board.

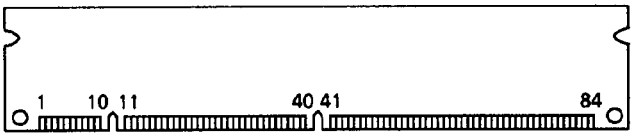
FEATURES

- 4,194,304 words by 64 bits (2bank) organization
- Single power supply of 3.3V±0.15V
- Low power
  - 3,312mW MAX. Operating (Single bank) (-10)
  - 3,257mW MAX. Operating (Single bank) (-12A)
  - 2,981mW MAX. Operating (Single bank) (-12)
  - 717.6mW MAX. Standby
- Architecture : Pipeline
- Auto refresh and Self refresh capability.
- All inputs and outputs LVTTL compatible
- 4,096 refresh cycles / 64ms
- Package : 168pin DIMM (Gold Contact)
- Based on Intel 1.0 (4-Clock)

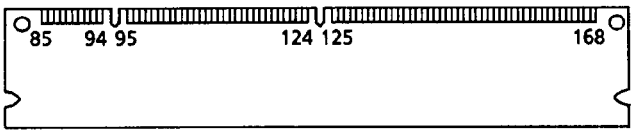
ITEM (TARGET SPEC)	-10	-12A	-12
t_{CK} Clock Cycle Time (CL = 2)	15ns	15ns	18ns
t_{RAS} Active to Precharge Command Peliod (MIN.)	60ns	60ns	72ns
t_{CAC} Access Time from Read Command (MAX.)	24ns	24ns	27.5ns
t_{AC} Access Time from CLK (CL = 2)	9ns	9ns	9.5ns
t_{RC} Ref/Active to Ref/Active Command Peliod (MIN.)	100ns	100ns	120ns

PIN CONNECTION (TOP VIEW)

FRONT SIDE



BACK SIDE



PIN NAMES

A0~A10	Address Inputs
BA0	Bank Select
DQ0~DQ63	Data Input/Outputs
/CS0~3	Chip Select
/RAS	Row Address Strobe
/CAS	Colum Address Strobe
/WE	Write Enable
DQMB0~7	Output Disable / Write Mask
CLK0~3	Clock Input
CKE0, 1	Clock Enable
SDA	Serial Data for PD
SCL	Clock for PD
SA0~2	Address for PD
VDD	Power (+3.3V)
VSS	Ground
NC	No Connection

1	VSS	85	VSS	22	NC	106	NC	43	VSS	127	VSS	64	VSS	148	VSS
2	DQ0	86	DQ32	23	VSS	107	VSS	44	NC	128	CKE0	65	DQ21	149	DQ53
3	DQ1	87	DQ33	24	NC	108	NC	45	/CS2	129	/CS3	66	DQ22	150	DQ54
4	DQ2	88	DQ34	25	NC	109	NC	46	DQMB2	130	DQMB6	67	DQ23	151	DQ55
5	DQ3	89	DQ35	26	VDD	110	VDD	47	DQMB3	131	DQMB7	68	VSS	152	VSS
6	VDD	90	VDD	27	/WE	111	/CAS	48	NC	132	NC	69	DQ24	153	DQ56
7	DQ4	91	DQ36	28	DQMB0	112	DQMB4	49	VDD	133	VDD	70	DQ25	154	DQ57
8	DQ5	92	DQ37	29	DQMB1	113	DQMB5	50	NC	134	NC	71	DQ26	155	DQ58
9	DQ6	93	DQ38	30	/CS0	114	/CS1	51	NC	135	NC	72	DQ27	156	DQ59
10	DQ7	94	DQ39	31	NC	115	/RAS	52	NC	136	NC	73	VDD	157	VDD
11	DQ8	95	DQ40	32	VSS	116	VSS	53	NC	137	NC	74	DQ28	158	DQ60
12	VSS	96	VSS	33	A0	117	A1	54	VSS	138	VSS	75	DQ29	159	DQ61
13	DQ9	97	DQ41	34	A2	118	A3	55	DQ16	139	DQ48	76	DQ30	160	DQ62
14	DQ10	98	DQ42	35	A4	119	A5	56	DQ17	140	DQ49	77	DQ31	161	DQ63
15	DQ11	99	DQ43	36	A6	120	A7	57	DQ18	141	DQ50	78	VSS	162	VSS
16	DQ12	100	DQ44	37	A8	121	A9	58	DQ19	142	DQ51	79	CLK2	163	CLK3
17	DQ13	101	DQ45	38	A10	122	BA0	59	VDD	143	VDD	80	NC	164	NC
18	VDD	102	VDD	39	NC	123	NC	60	DQ20	144	DQ52	81	NC	165	SA0
19	DQ14	103	DQ46	40	VDD	124	VDD	61	NC	145	NC	82	SDA	166	SA1
20	DQ15	104	DQ47	41	VDD	125	CLK1	62	NC	146	NC	83	SCL	167	SA2
21	NC	105	NC	42	CLK0	126	NC	63	CKE1	147	NC	84	VDD	168	VDD

961001EBA1

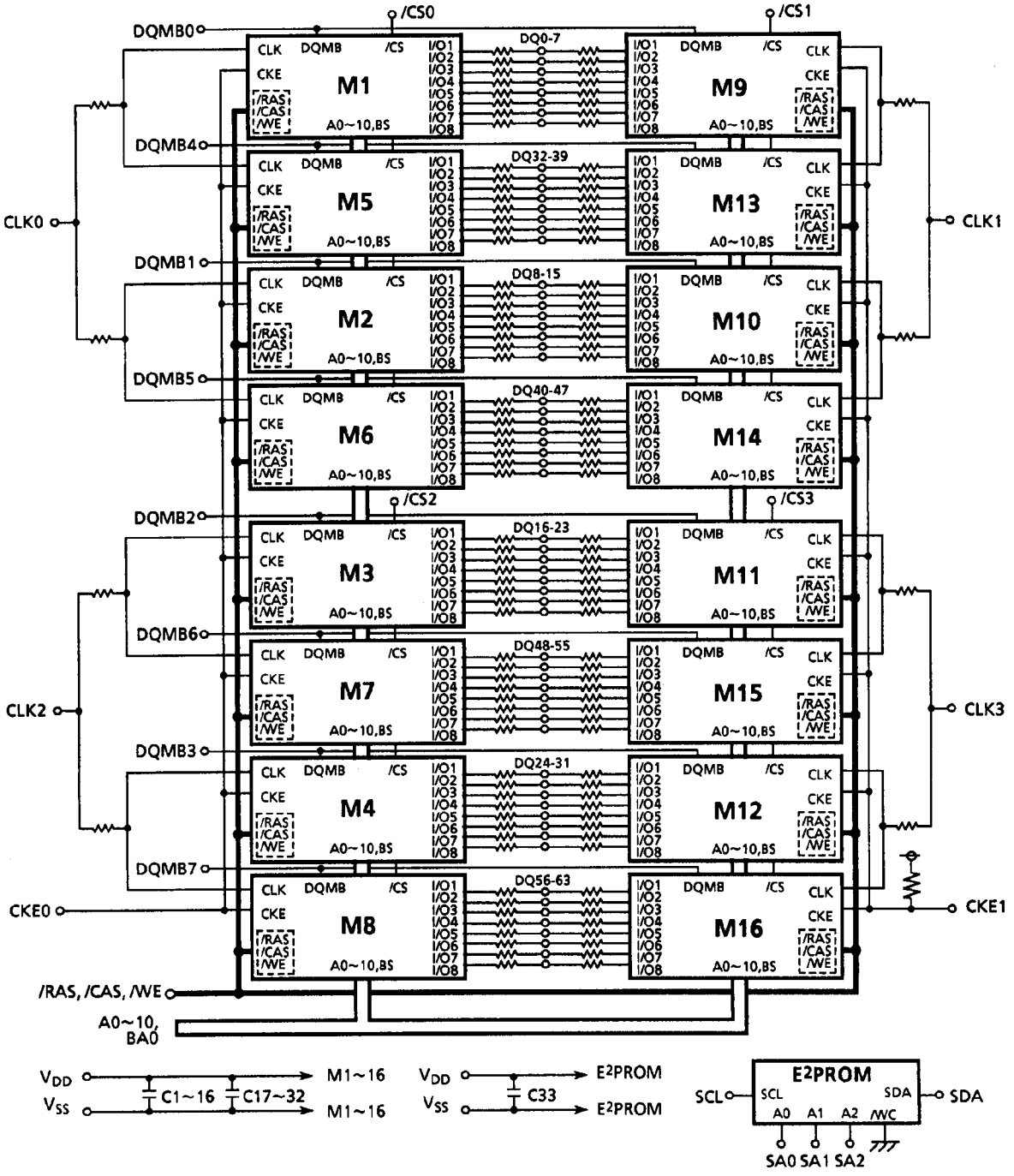
Serial Presence Detect (Rev.1)

Byte Number	Function Described	-10		-12A		-12	
		Entry Value	Entry	Entry Value	Entry	Entry Value	Entry
0	Defines # bytes Written into Serial Memory at Module mfgr	128bytes	80h	128bytes	80h	128bytes	80h
1	Total # bytes of SPD Memory Device	256bytes	08h	256bytes	08h	256bytes	08h
2	Fundamental Memory Type (FPM, EDO, SDRAM...) from Appendix A	SDRAM	04h	SDRAM	04h	SDRAM	04h
3	# Row Addresses on this Assembly	RA0-RA10	0Bh	RA0-RA10	0Bh	RA0-RA10	0Bh
4	# Column Addresses on this Assembly	CA0-CA8	09h	CA0-CA8	09h	CA0-CA8	09h
5	# Module Banks on this Assembly	2Bank	02h	2Bank	02h	2Bank	02h
6	Data Width of this Assembly...	x64	40h	x64	40h	x64	40h
7	...Data Width Continuation	x64	00h	x64	00h	x64	00h
8	Voltage Interface Standard of this Assembly	LVTTL	01h	LVTTL	01h	LVTTL	01h
9	SDRAM Cycle Time at Max. Supported CAS Latency (CL), CL = X	CL = 3, 10ns	A0h	CL = 3, 12ns	C0h	CL = 3, 12ns	C0h
10	SDRAM Access from Clock @ CL = X	CL = 3, 8.5ns	85h	CL = 3, 9.0ns	90h	CL = 3, 9.0ns	90h
11	DIMM Configuration Type (Non-parity, Parity, ECC)	Non-Parity	00h	Non-Parity	00h	Non-Parity	00h
12	Refresh Rate/Type	15.625μs/self	80h	15.625μs/self	80h	15.625μs/self	80h
13	SDRAM Width, Primary DRAM	x8	08h	x8	08h	x8	08h
14	Error Checking SDRAM Data Width	N/A	00h	N/A	00h	N/A	00h
15	Minimum Clock Delay, Back to Back Random Column Addresses	1CLK	01h	1CLK	01h	1CLK	01h
16	Burst Lengths Supported		8Fh		8Fh		8Fh
17	# Banks on each SDRAM Device	2Bank	02h	2Bank	02h	2Bank	02h
18	CAS # Latencies Supported		07h		07h		07h
19	CS # Latency		01h		01h		01h
20	WE # Latency		01h		01h		01h
21	SDRAM Module Attributes		00h		00h		00h
22	SDRAM Device Attributes : General		0Eh		0Eh		0Eh
23	Minimum Clock Cycle Time at CL- X-1	CL = 2, 15ns	F0h	CL = 2, 15ns	F0h	CL = 2, 18ns	30h
24	Maximum Data Access Time from Clock @ CL X-1	CL = 2, 9.0ns	90h	CL = 2, 9.0ns	90h	CL = 2, 9.5ns	95h
25	Minimum Clock Cycle Time at CL X-2	CL = 1, 30ns	78h	CL = 1, 30ns	78h	CL = 1, 36ns	90h
26	Maximum Data Access Time from Clock @ CL X-2	CL = 1, 24ns	60h	CL = 1, 24ns	60h	CL = 1, 27.5ns	6Eh
27	Minimum Row Precharge Time	30ns	1Eh	30ns	1Eh	36ns	24h
28	Minimum Row Active to Row Active Delay	20ns	14h	24ns	18h	24ns	18h
29	Minimum RAS to CAS Delay	30ns	1Eh	30ns	1Eh	36ns	24h
30	Minimum RAS Pulse Width	60ns	3Ch	60ns	3Ch	72ns	48h
31	Module/Bank Density	16MB	04h	16MB	04h	16MB	04h
32-61	Superset Information (may be used in future)		FFh		FFh		FFh
62	SPD Revision	Rev.1	01h	Rev.1	01h	Rev.1	01h
63	Checksum for bytes 0-62		04h		33h		B6h

Option

64	Manufacturers JEDEC ID Code per JEP-106E						
65-71							
72	Manufacturing Location						
73-90	Manufacturer's Part Number						
91-92	Revision Code						
93-94	Manufacturing Date						
95-98	Assembly Serial Number						
99-125	Manufacturer Specific Data						
126	Reserved	Intel Specification	66h	Intel Specification	66h	Intel Specification	66h
127	Reserved	Intel Specification	06h	Intel Specification	06h	Intel Specification	06h
128-255							

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNITS	NOTES
V_{IN}	Input Voltage	$-0.3 \sim V_{CC}+0.3$	V	1
V_{OUT}	Output Voltage	$-0.3 \sim V_{CC}+0.3$	V	1
VDD	Power Supply Voltage	$-0.3 \sim 4.6$	V	1
T_{OPR}	Operating Temperature	0~70	°C	1
T_{STG}	Storage Temperature	−55~125	°C	1
P_D	Power Dissipation	37	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
VDD	Supply Voltage	3.15	3.3	3.45	V	2
V_{IH}	LVTTL Input High Voltage	2.0	–	VDD + 0.3	V	2
V_{IL}	LVTTL Input Low Voltage	−0.3	–	0.8	V	2

CAPACITANCE (V_{CC} = 3.3V, f = 1MHz, Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_1	Input Capacitance (A0~A10)	–	80	pF
C_2	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, BA0)	–	80	pF
C_3	Input Capacitance (CLK0~3)	–	38	pF
C_4	Input Capacitance ($\overline{CS}$0~3)	–	25	pF
C_5	Input Capacitance (DQMB0~7)	–	18	pF
C_{DQ}	Input / Output Capacitance (DQ0~DQ63)	–	19	pF

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 3.3V ± 0.15V, Ta = 0~70°C)

SYMBOL	ITEM		-10		-12A		-12		UNIT	NOTE
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
I_{CC1}	OPERATING CURRENT Active-Precharge Command Cycling without Burst Operation (t_{CK} = MIN. t_{RC} = MIN.)	1 bank operation	-	960	-	944	-	864	mA	3, 5
I_{CC1B}		2 bank interleave operation	-	1280	-	1264	-	1144		
I_{CC2}	STANDBY CURRENT (t_{CK} = MIN. $\overline{CS}$ = V_{IH}, $V_{IH/L}$ = V_{IH} (MIN.) / V_{IL} (MAX.) bank : inactive state)	CKE = V_{IH}	-	480	-	448	-	448	mA	3
I_{CC2P}		CKE = V_{IL} (Power Down Mode)	-	32	-	32	-	32		
I_{CC2S}	STANDBY CURRENT (CLK = V_{IL} $\overline{CS}$ = V_{IH}, $V_{IH/L}$ = V_{IH} (MIN.) / V_{IL} (MAX.) bank : inactive state)	CKE = V_{IH}	-	208	-	208	-	208	mA	
I_{CC2PS}		CKE = V_{IL} (Power Down Mode)	-	32	-	32	-	32		
I_{CC3}	NO OPERATING CURRENT (t_{CK} = MIN. $\overline{CS}$ = V_{IH}(MIN.) bank : active state (2 bank))	CKE = V_{IH}	-	840	-	784	-	784	mA	3, 5
I_{CC3P}		CKE = V_{IL} (Power Down Mode)	-	48	-	48	-	48		
I_{CC4}	BURST OPERATING CURRENT (t_{CK} = MIN. $\overline{CS}$ = V_{IH}(MIN.) Read / Write command cycling)		-	1320	-	1224	-	1224	mA	3, 4, 5
I_{CC5}	AUTO REFRESH CURRENT (t_{CK} = MIN. Auto Refresh command cycling)		-	760	-	744	-	704	mA	3, 5
I_{CC6}	SELF REFRESH CURRENT (Self Refresh mode CKE = 0.2V)		-	32	-	32	-	32	mA	3
$I_{I(L)}$	INPUT LEAKAGE CURRENT (0V ≤ V_{IN} ≤ V_{DD}, All Other Pins Not Under Test = 0V)		-5	5	-5	5	-5	5	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ V_{DD})		-5	5	-5	5	-5	5	μA	
V_{OH}	OUTPUT LEVEL LVTTL Output "H" Level Voltage (I_{OUT} = -2mA)		2.4	-	2.4	-	2.4	-	V	
V_{OL}	OUTPUT LEVEL LVTTL Output "L" Level Voltage (I_{OUT} = 2mA)		-	0.4	-	0.4	-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A. C. OPERATING CONDITIONS

(V_{CC} = 3.3V ± 0.15V, Ta = 0~70°C) (Notes 6, 7, 8)

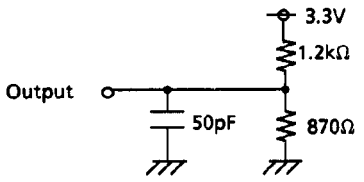
SYMBOL	PARAMETER		-10		-12A		-12		UNIT	NOTE
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Ref/Active-Ref/Active Command Period		100		100		120		ns	10
t_{RAS}	Active- Precharge Command Period		60	100000	60	100000	72	100000		
t_{RCD}	Active-Read/Write Command Delay Time		30		30		36			
t_{CCD}	Read/Write(a) -Read/Write(b) Command Period		10		12		12			
t_{RP}	Precharge-Active Command Period		30		30		36			
t_{RRD}	Active(a)-Active(b) Command Period		20		24		24			
t_{CAC}	Accesss Time from Read Command			24		24		27.5		
t_{WR}	Write Recovery Time	CL* = 1	30		30		36			
		CL* = 2	15		15		18			
		CL* = 3	1CLK + 10		1CLK + 12		1CLK + 12			
t_{CK}	CLK Cycle Time	CL* = 1	30	1000	30	1000	36	1000		
		CL* = 2	15	1000	15	1000	18	1000		
		CL* = 3	10	1000	12	1000	12	1000		
t_{CH}	CLK High Level Width		3		4		4			11
t_{CL}	CLK Low Level Width		3		4		4			
t_{AC}	Access Time from CLK	CL* = 1		24		24		27.5		
		CL* = 2		9		9		9.5		
		CL* = 3		8.5		9		9		
t_{OH}	Output Data Hold Time		3		3		3			
t_{HZ}	Output Data High Impedance Time		3	10	3	12	3	12		9
t_{LZ}	Output Data Low Impedance Time		0		0		0			
t_{SB}	Power Down Mode Entry Time		0	10	0	12	0	12		
t_T	Transition Time of CLK (Rise and Fall)		1	10	1	10	1	10		
t_{DS}	Data-in Set-up Time		3		3		3			
t_{DH}	Data-in Hold Time		1		1		1			
t_{AS}	Address Set-up Time		3		3		3			
t_{AH}	Address Hold Time		1		1		1			
t_{CKS}	CKE Set-up Time		3		3		3			
t_{CKH}	CKE Hold Time		1		1		1			
t_{CMS}	Commnd Set-up Time		3		3		3			
t_{CMH}	Command Hold Time		1		1		1			
t_{REF}	Refresh Time			64		64		64	ms	
t_{RSC}	Mode Register set Cycle Time		20		24		24		ns	10

* CL is $\overline{CAS}$ Latency.

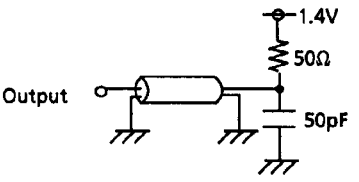
NOTE :

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to Vss.
3. These parameters depend on the cycle rate and these values are measured by the cycle rate under the minimum value of t_{CK} and t_{RC}. Input signals are changed one time during t_{CK}.
4. These parameters depend on the output loading. Specified values are obtained with the output open.
5. These values are measured with the following conditions.
   Front side (or back side) : the measuring conditions on the data sheet
   Back side (or front side) : Standby (measured with $I_{CC}2$ conditions)
6. Power - up sequence is described in NOTE 12.
7. A. C. TEST CONDITIONS

Reference Level of Output Signals	1.4V / 1.4V
Output Load	Reference to the Under Output Load (B)
Input Signal Levels	2.4V / 0.4V
Transition Time (Rise and Fall) of Input Signals	2ns
Reference Level of Input Signals	1.4V



A.C. TEST LOAD (A)



A.C. TEST LOAD (B)

8. Transition times are measured between V_{IH} and V_{IL}. Transition (rise and fall) of input signals are fixed slope.
9. t_{HZ} define the time at which the outputs achieve the open circuit condition and are not reference levels.

10. These parameters account for the number of clock cycle and depend on the operating frequency of the clock, as follows :
    the number of clock cycle = specified value of timing / clock period
    (count fractions as a whole number)

11. t_{CH} is the pulse width of CLK measured from the positive edge to the negative edge referenced to V_{IH} (min.). t_{CL} is the pulse width of CLK measured from the negative edge to the positive edge referenced to V_{IL} (max.).

12. Power up Sequence

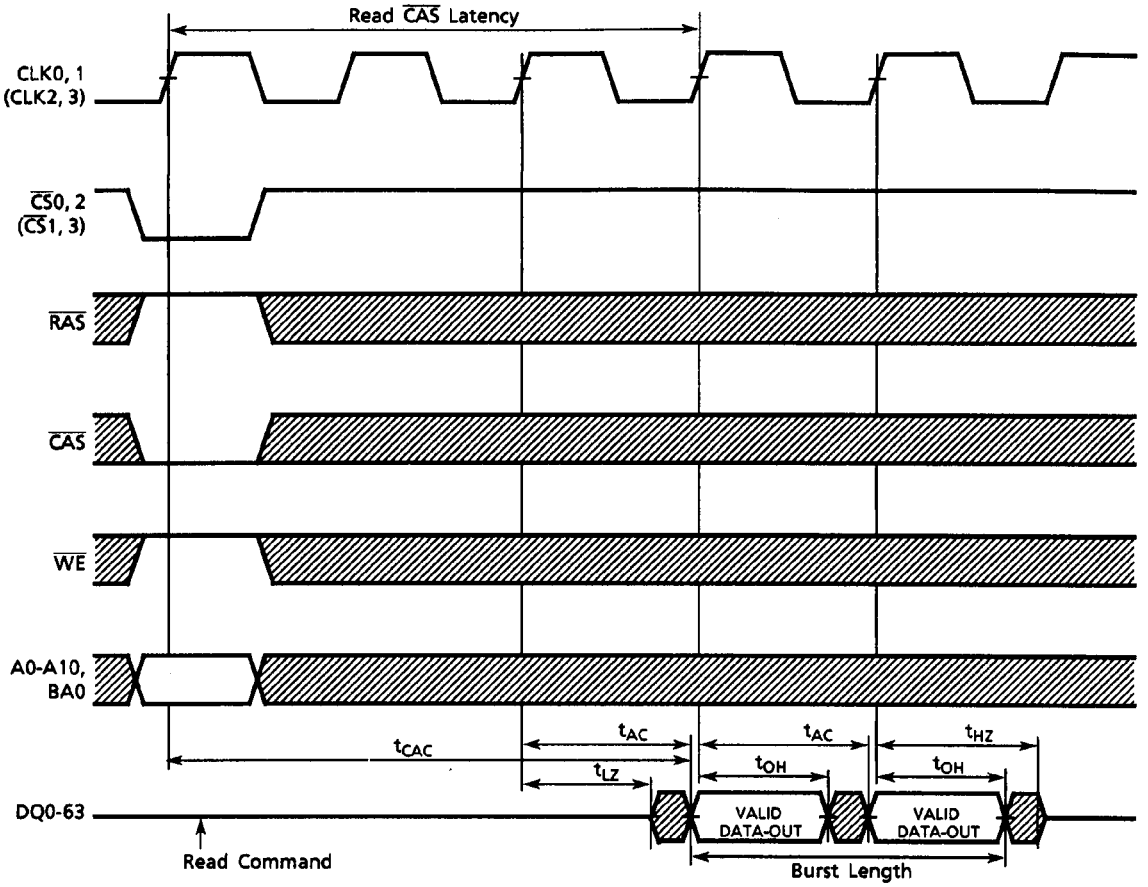
    Power up must be performed in the following sequence.

    1) Power must be applied to V_{DD} when all input signals are held "NOP" state. The CLK signal must be started at the same time.
    2) After power - up a pause of 200μseconds minimum is required. Then, it is required that DQMB and CKE signals are held "high" (V_{DD} levels) to ensure the DQ output to be in the high impedance.
    3) Both banks must be precharged.
    4) Mode register set command must be asserted to initialize the Mode register.
    5) A minimum of 8 Auto - Refresh dummy cycles must be required to stabilize the internal circuitly of the device.

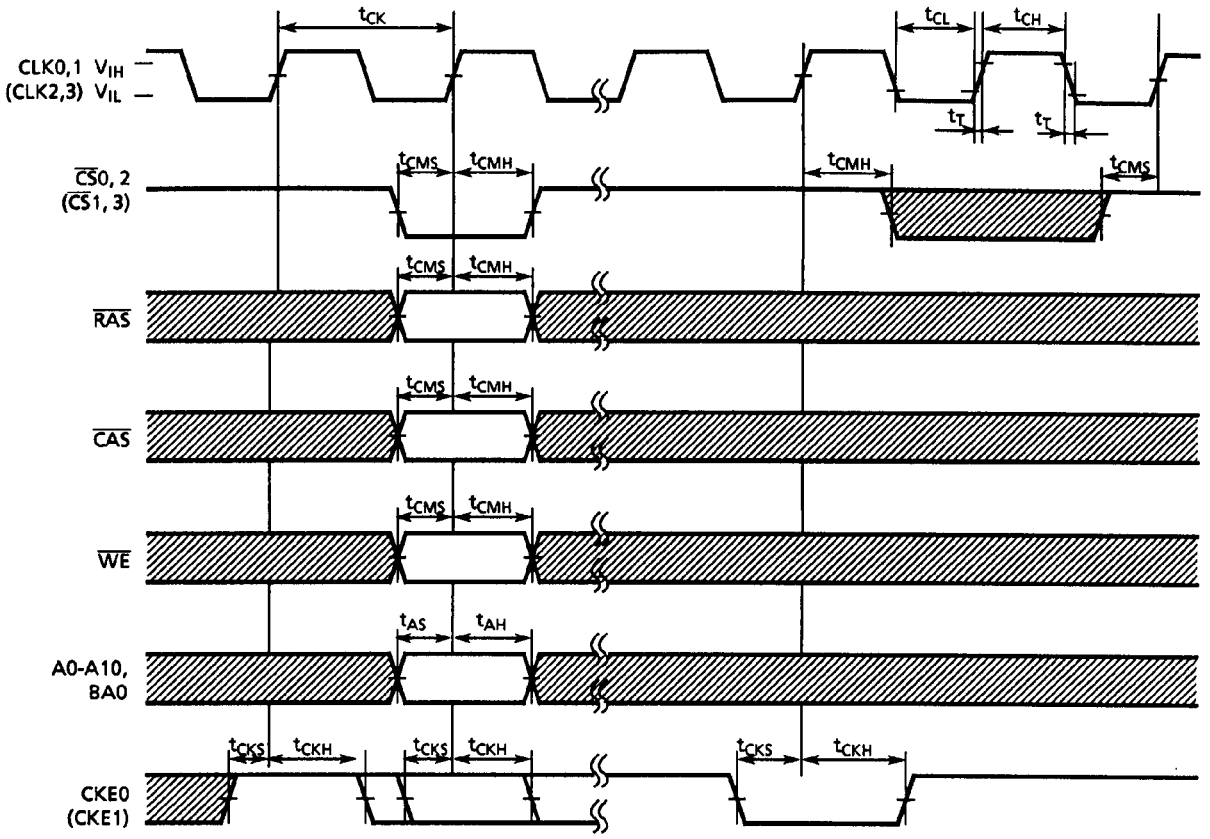
    The sequence of Mode register set and Auto-Refresh dummy cycles may be exchanged.

TIMING WAVEFORM

Read Timing

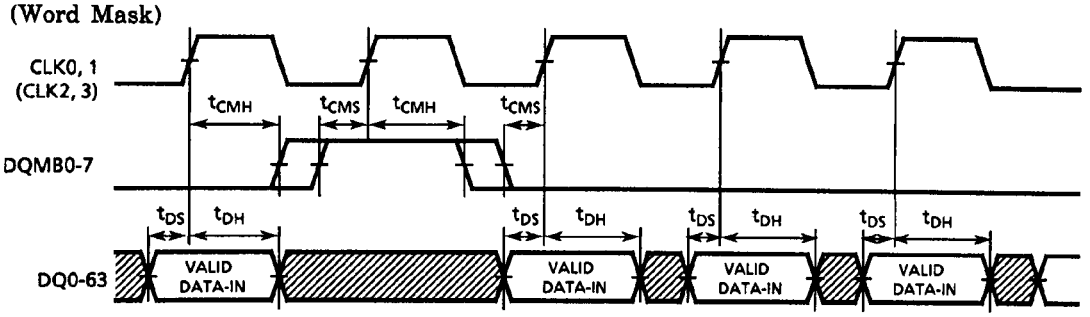


Command Input Timing

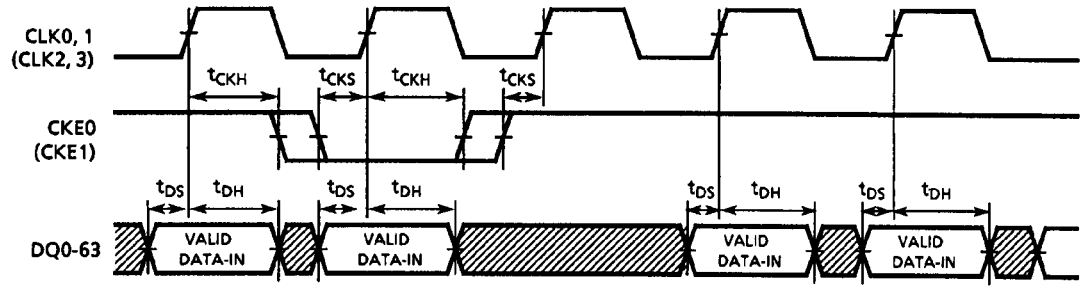


Control Timing of Input Data

(Word Mask)

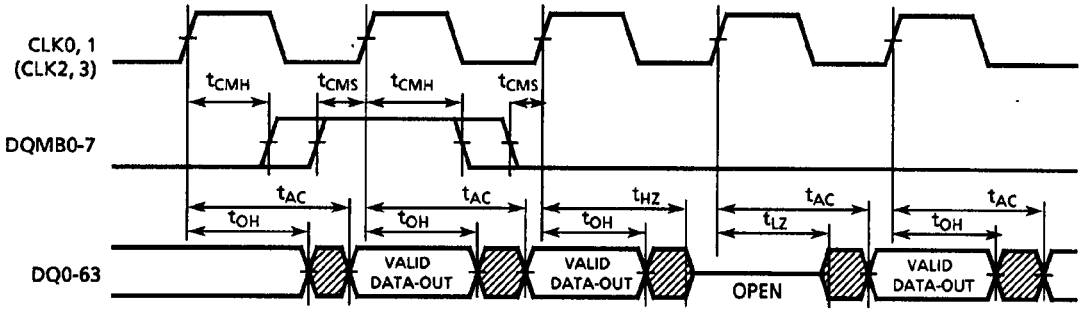


(Clock Mask)

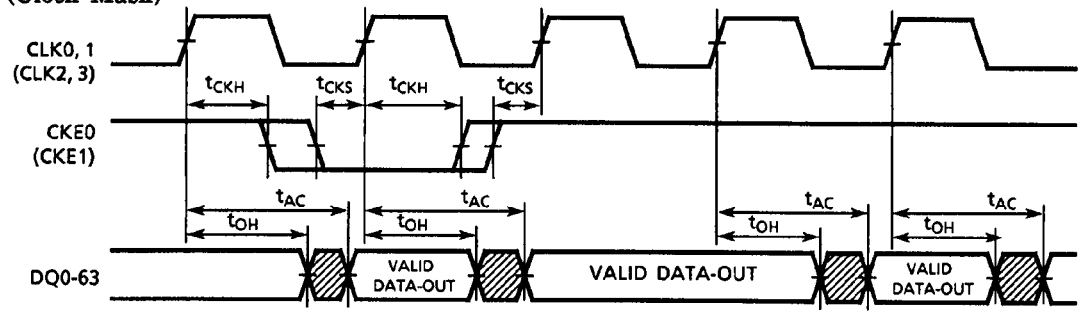


Control Timing of Output Data

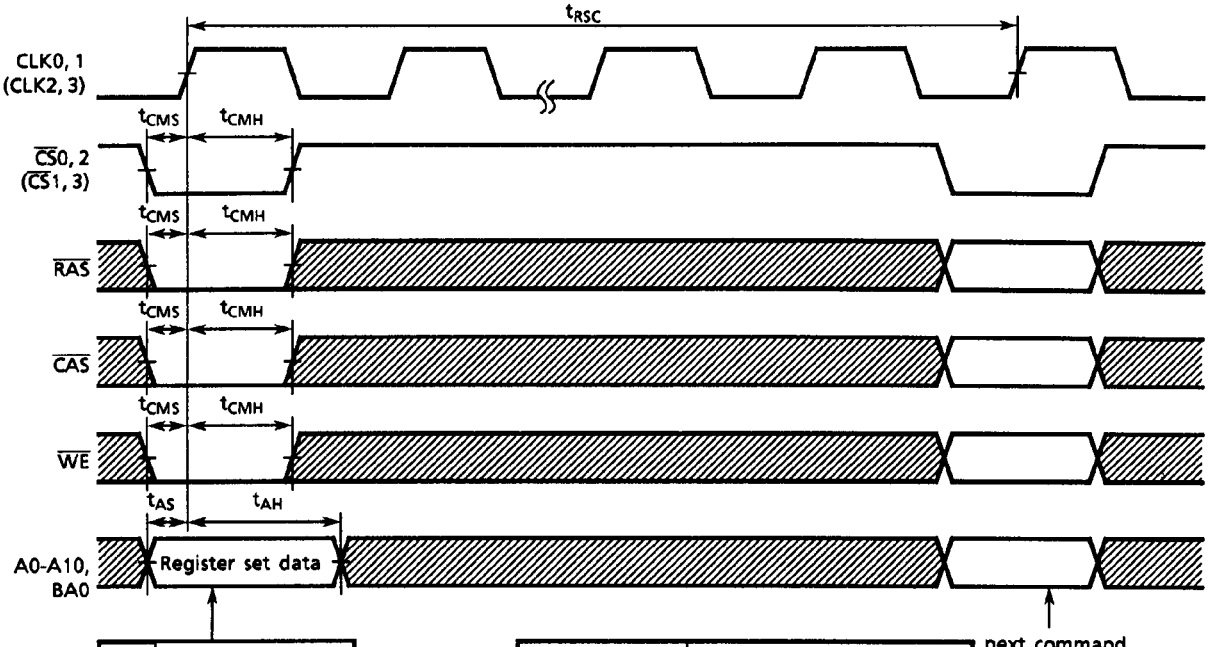
(Output Enable)



(Clock Mask)



Mode Resister Set Cycle



A0	Burst Length	
A1		
A2		
A3	Addressing Mode	
A4	CAS Latency	
A5		
A6		
A7	"0"	(Test Mode)
A8	"0"	Reserved
A9	Write Mode	
A10	"0"	Reserved
BA0	"0"	

			Burst Length	
A2	A1	A0	Sequential	Interleave
0	0	0	1	1
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1		
1	1	0		
1	1	1	Full Page	

A3	Addressing Mode
0	Sequential
1	Interleave

A6	A5	A4	CAS Latency
0	0	0	Reserved
0	0	1	1
0	1	0	2
0	1	1	3
1	x	x	Reserved

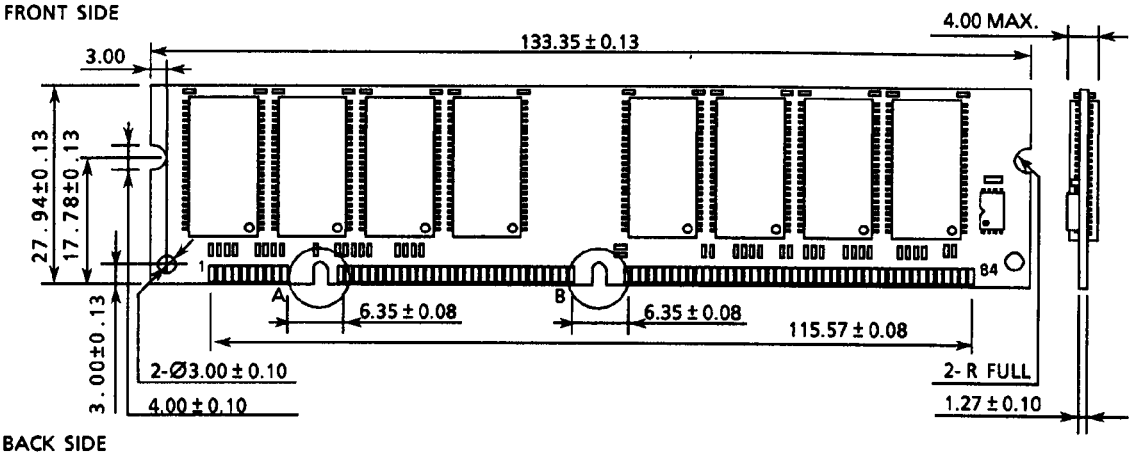
A9	Single Write Mode
0	Burst read and Burst write
1	Burst read and Single write

OUTLINE DRAWING

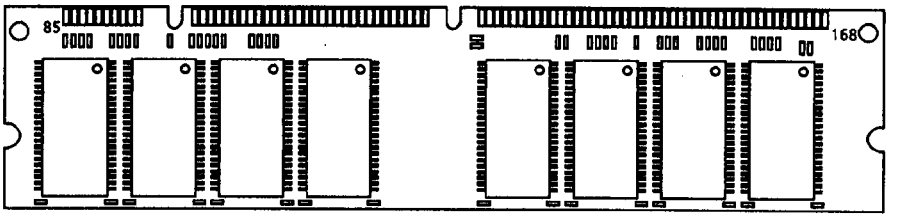
THMY6440A1AEG

Unit : mm

FRONT SIDE

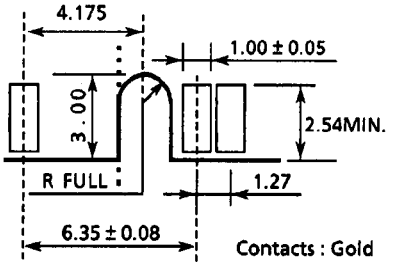


BACK SIDE



DETAIL OF CONTACTS

A : Unbuffered type keying



B : 3.3V type keying