Signetics

SAA3028
Remote Control Receiver/Transcoder

Product Specification

Linear Products

DESCRIPTION

The SAA3028 is intended for use in general purpose (RC-5) remote control systems. The main function of this integrated circuit is to convert RC-5 biphase coded signals into equivalent binary values. Two input circuits are available: one for RC-5 coded signals only; the other selectable to accept RC-5 coded signals only, or RC-5 (extended) coded signals only. The input used is that at which an active code is first detected. Coded signals not in RC-5/RC-5(ext) format are rejected. Data input and output is by serial transfer, the output interface being *compatible for I^2C bus operation.*

FEATURES

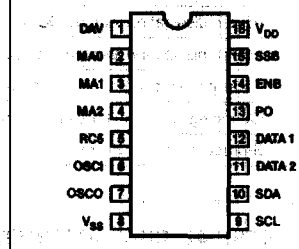
- **Converts RC-5 or RC-5(ext) biphase coded signals into binary equivalents**
- **Two data inputs: one fixed (RC-5); one selectable (RC-5/RC-5(ext))**
- **Rejects all codes not in RC-5/RC-5(ext) format**
- **I^2C output interface capability**
- **Power-off facility**
- **Master/slave addressable for multi-transmitter/receiver applications in RC-5(ext) mode**
- **Power-on reset for defined start-up**

APPLICATION

- **Remote control systems**

PIN CONFIGURATION

N Package



TOP VIEW

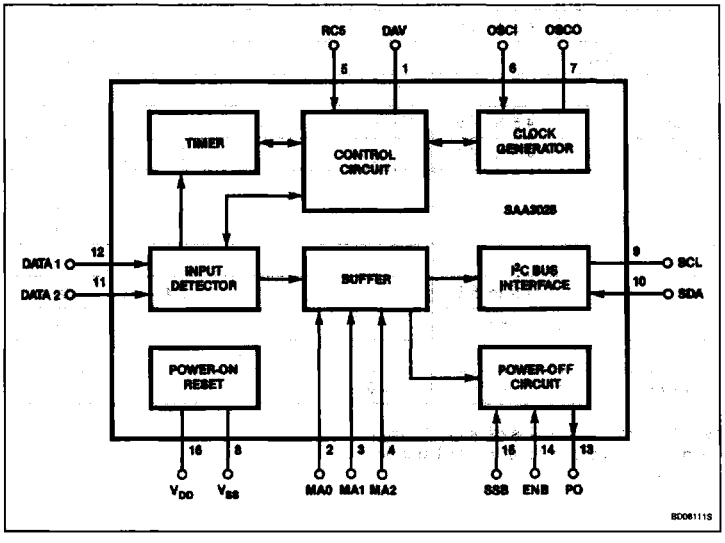
CD12040S

PIN NO.	SYMBOL	DESCRIPTION
1	DAV	Data valid output with open drain N-channel transistor
2	MA0	Master address inputs
3	MA1	Master address inputs
4	MA2	Master address inputs
5	RC5	Data 2 input select
6	OSCI	Oscillator input
7	OSCO	Oscillator output
8	V_{SS}	Negative supply (ground)
9	SCL	Serial clock line (I^2C bus)
10	SDA	Serial data line (I^2C bus)
11	DATA 2	Data 2 input
12	DATA 1	Data 1 input
13	PO	Power-off signal output with open drain N-channel transistor
14	ENB	Enable input
15	SSB	Set standby input
16	V_{DD}	Positive supply (+5V)

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP (SOT-38Z)	−25°C to 85°C	SAA3028N

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}	Supply voltage range with respect to V_{SS}	−0.5 to +15	V
V_I	Input voltage range	−0.5 to (V_{DD} + 0.5)	V[1]
$\pm I_I$	Input current	10	mA
V_O	Output voltage range	−0.5 to (V_{DD} + 0.5)	V[1]
$\pm I_O$	Output current	10	mA
P_O	Power dissipation output OSCO	50	mW
P_O	Power dissipation per output (all other outputs)	100	mW
P_{TOT}	Total power dissipation per package	200	mW
T_A	Operating ambient temperature range	−25 to +85	°C
T_{STG}	Storage temperature range	−55 to +150	°C

NOTE:
1. V_{DD}+0.5 not to exceed 15V.

DC ELECTRICAL CHARACTERISTICS V_{SS}=0V; T_A = −25°C to 85°C, unless otherwise specified.

SYMBOL	PARAMETER	V_{DD} (V)	LIMITS			UNIT
			Min	Typ	Max	
V_{DD}	Supply voltage		4.5		5.5	V
I_{DD}	Supply current; quiescent at T_A = 25°C	5.5			200	μA
Inputs MA0, MA1, MA2, DATA 1, DATA 2, RC5, SCL, ENB, SSB, OSCI						
V_{IH}	Input voltage HIGH	4.5 to 5.5	0.7 × V_{DD}		V_{DD}	V
V_{IL}	Input voltage LOW	4.5 to 5.5	0		0.3 × V_{DD}	V
I_I	Input leakage current at V_I = 5.5V; T_A = 25°C	5.5			1	μA
$-I_I$	Input leakage current at V_I = 0V; T_A = 25°C	5.5			1	μA
Outputs DAV, PO						
V_{OL}	Output voltage LOW at I_{OL} = 1.6mA	4.5 to 5.5			0.4	V
I_{OR}	Output leakage current at V_O = 5.5V; T_A = 25°C	5.5			1	μA
OSCO						
V_{OH}	Output voltage HIGH at $-I_{OH}$ = 0.2mA	4.5 to 5.5	V_{DD} − 0.5			V
V_{OL}	Output voltage LOW at I_{OL} = 0.3mA	4.5 to 5.5			0.4	V
	Output leakage current at T_A = 25°C;					
I_{OR}	V_O = 5.5V	5.5			1	μA
I_{OR}	V_O = 0V	5.5			1	μA
SDO						
V_{OL}	Output voltage LOW at I_{OL} = 2mA	4.5 to 5.5			0.4	V
I_{OR}	Output leakage current at V_O = 5.5V; T_A = 25°C	5.5			1	μA
Oscillator						
f_{OSCI}	Maximum oscillator frequency (Figure 6)	4.75	500			kHz

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

FUNCTIONAL DESCRIPTION

Input Function

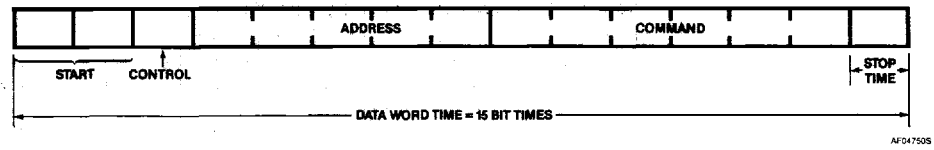
The two data inputs are accepted into the buffer as follows:

DATA 1: Only biphase coded signals which conform to the RC-5 format are accepted at this input.

DATA 2: This input performs according to the logic state of the select input RC5. When RC5 = HIGH, DATA 2 input will accept only RC-5 coded signals. When RC5 = LOW, DATA 2 input will accept only RC-5(ext) coded signals.

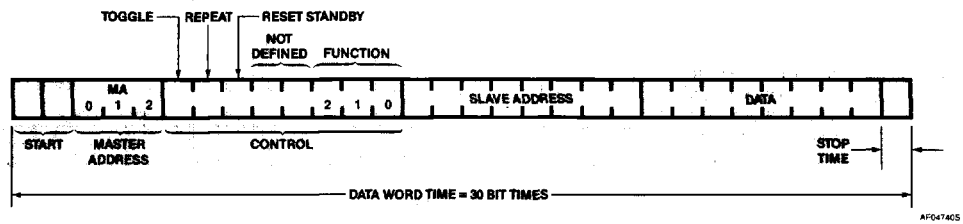
The input detector selects the input, DATA 1 or DATA 2, in which a HIGH-to-LOW transition is first detected. The selected input is then accepted by the buffer for code conversion. All signals received that are not in the RC-5 or RC-5(ext) format are rejected.

Formats of RC-5 and RC-5(ext) biphase coded signals are shown in Figures 1 and 2, respectively; the codes commence from the left of the formats shown. The bit-times of the biphase codes are defined in Figure 3.



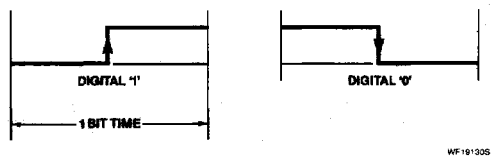
NOTE:
Stop time = 1.5 bit-times (nominal).

Figure 1. RC-5 Code Format: the First Start Bit is Used Only for Detection and Input Gain-Setting



NOTE:
Stop time = 1.5 bit-times (nominal).

Figure 2. RC-5 (extended) Code Format: the First Start Bit is Used Only for Detection and Input Gain-Setting



NOTE:
RC-5 bit-time = $2^7 \times t_{OSC}$ = 1.778ms (typical), RC-5(ext) bit-time = $2^6 \times t_{OSC}$ = 0.89ms (typical), where t_{OSC} = the oscillator period time.

Figure 3. Biphase Code Definition

More information is added to the input data held in the buffer in order to make it suitable for transmission via the I^2C interface. The information now held in the buffer is as shown in the table.

RC-5 BUFFER CONTENTS		RC-5(EXT) BUFFER CONTENTS	
• Data valid indicator	1 Bit	• Data valid indicator	1 Bit
• Format indicator	1 Bit	• Format indicator	1 Bit
• Input indicator	1 Bit	• Input indicator	1 Bit
• Control	1 Bit	• Master address	3 Bits
• Address data	5 Bits	• Control	8 Bits
• Command data	6 Bits	• Slave address	8 Bits
		• Data	8 Bits

The information assembled in the buffer is subjected to the following controls before being made available at the I_2C interface:

ENB = HIGH — Enables the set standby input SSB.

SSB = LOW — Causes power-off output PO to go HIGH.

PO = HIGH — This occurs when the set standby input SSB = LOW and allows the existing values in the buffer to be overwritten by the new binary equivalent values. After ENB = LOW, SSB is don't care.

PO = LOW — This occurs according to the type of code being processed, as follows:
RC-5: When the binary equivalent value is transferred to the buffer.
RC-5(ext): When the reset standby bit is active and the master address bits are equal in value to the MA0, MA1, MA2 inputs.
At power-on, PO is reset to LOW.

DAV = HIGH — This occurs when the buffer contents are valid. If the buffer is not empty, or an output transfer is taking place, then the new binary values are discarded.

Output Function

The data is assembled in the buffer in the format shown in Figure 4 for RC-5 binary equivalent values, or in the format shown in Figure 5 for RC-5(ext) binary equivalent values. The data is output serially, starting from the left of the formats shown in Figures 4 and 5.

The output signal DAV, derived in the buffer from the data valid bit, is provided to facilitate use of the transcoder on an interrupt basis. This output is reset to LOW during power-on.

The I^2C interface allows transmission on a bidirectional, two-wire I^2C bus. The interface is a slave transmitter with a built-in slave address, having a fixed 7-bit binary value of 0100110. Serial output of the slave address onto the I^2C bus starts from the left-hand bit.

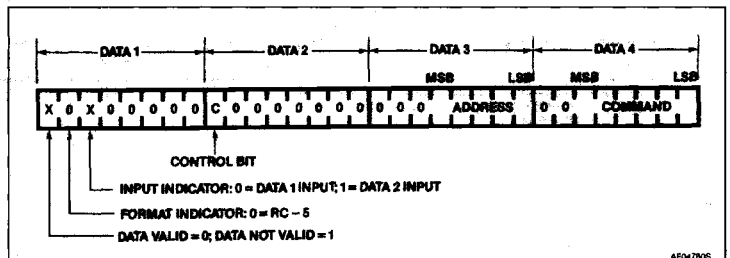


Figure 4. RC-5 Binary Equivalent Value Format

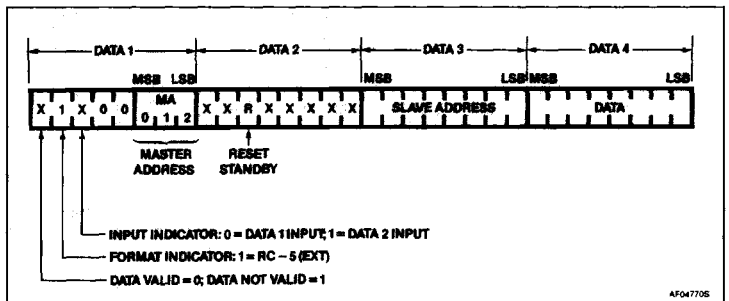
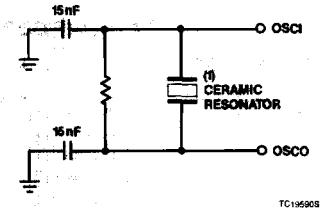


Figure 5. RC-5(ext) Binary Equivalent Value Format

Oscillator

The oscillator can comprise a ceramic resonator circuit as shown in Figure 6. The typical frequency of oscillation is 455kHz.



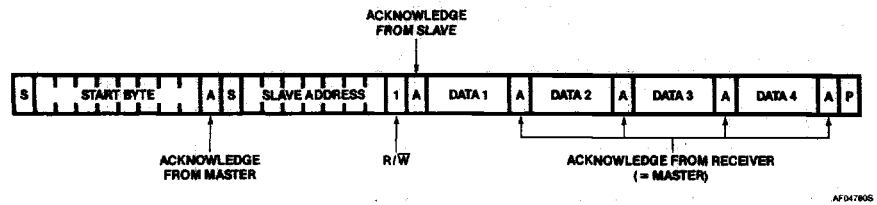
NOTE:
(1) Catalog number of ceramic resonator: 2422 540 98008.

Figure 6. Oscillator Circuit

FUNCTIONAL DESCRIPTION

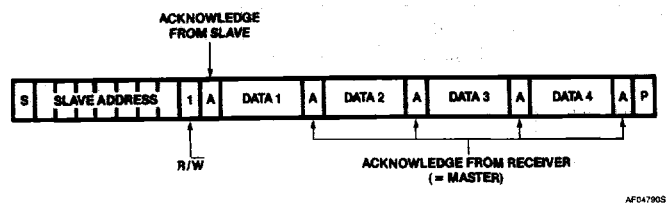
I²C Bus Transmission

Formats for I²C transmission in low-and high-speed modes are shown respectively in Figures 7 and 8.



NOTES:
When R/$\overline{W}$ bit = 0, the slave generates a NACK (negative acknowledge), leaves the data line HIGH and waits for a stop (P) condition.
When the receiver generates a NACK, the slave leaves the data line HIGH and waits for P (the slave acting as if all data has been transmitted).
When all data has been transmitted, the data line remains HIGH and the slave waits for P.

Figure 7. Format for Transmission in I²C Low-Speed Mode



NOTES:
When R/$\overline{W}$ bit = 0, the slave generates a NACK (negative acknowledge), leaves the data line HIGH and waits for a stop (P) condition.
When the receiver generates a NACK, the slave leaves the data line HIGH and waits for P (the slave acting as if all data has been transmitted).
When all data has been transmitted, the data line remains HIGH and the slave waits for P.

Figure 8. Format for Transmission in I²C High-Speed Mode