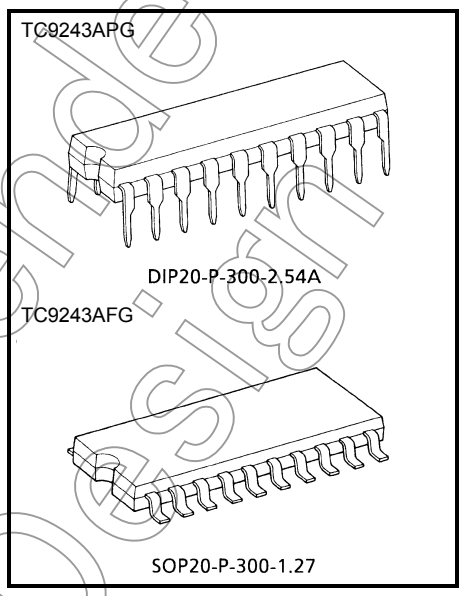
TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC9243APG, TC9243AFG

Infrared Remote-Control Signal Transmission LSI

The TC9243APG and TC9243AFG are infrared remote-control signal transmission LSIs suitable for remote control of audio systems, TVs, VTRs, CD players, etc.

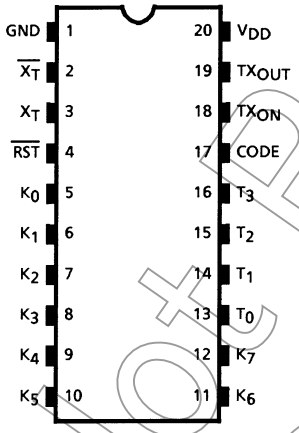


Weight
DIP20-P-300-2.54A: 1.4 g (typ.)
SOP20-P-300-1.27: 0.48 g (typ.)

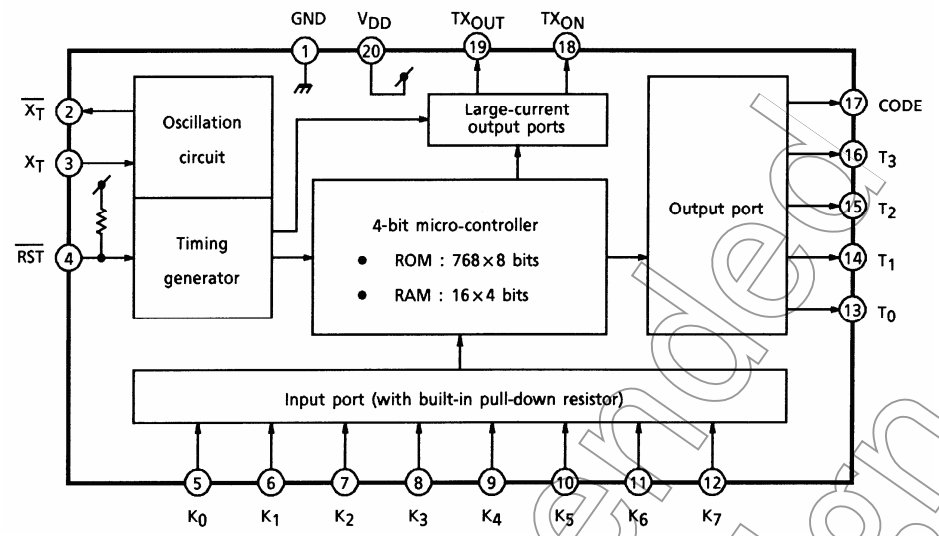
Features

- Wide range of operating supply voltages, enabling low-voltage operation:
  V_{DD} = 2.0 to 4.0 V
- Thirty-two (32) basic functions are available.
  Support of multiple keying enables up to 112 instructions (28 × 4) to be output.
- Interference with other equipment can be prevented because seven (7) bits out of eight (8) bits of system code are presettable.
- Equipped with transmission display output pin.
- Low current dissipation: $I_{QD} \leq 1$ μA (during standby)
- Two types of package, DIP and flat type, are available:
  DIP20: TC9243APG
  SOP20: TC9243AFG

Pin Assignment



Block Diagram



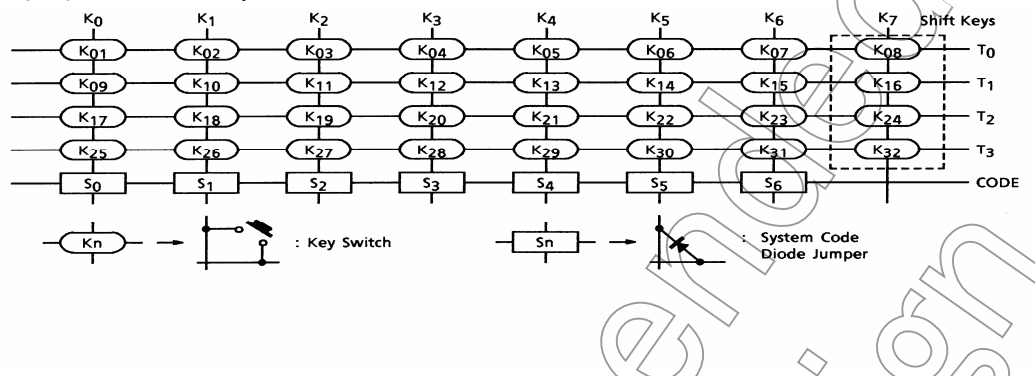
Pin Function

Pin No.	Symbol	Pin Name	Function and Operation
1	GND	Power Terminal	For applying the supply voltage (V_{DD} = 2.0 to 4.0 V)
20	V_{DD}		
2	$\overline{X_T}$	Oscillator Terminal	Input/output terminals for the ceramic oscillators, with built-in amplifier circuit and feedback resistor
3	X_T		
4	$\overline{RST}$	Reset Input	When this pin is set at "L" level, the inside is initialized. Equipped with a built-in pull-up resistor.
5~12	K_0~K_7	Key Inputs	Input terminals for the key matrix. Each pin has a built-in pull-down resistor.
13~16	T_0~T_3	Key Scan Output	Key matrix scan output terminals. CMOS output.
17	CODE	Code Scan Output	Scan output terminals for code setting. P-ch open drain output.
18	TX_{ON}	Transmission Display Output	Transmission display LED driving output terminal
19	TX_{OUT}	Transmission Output	Infrared LED driving output terminal

Operations

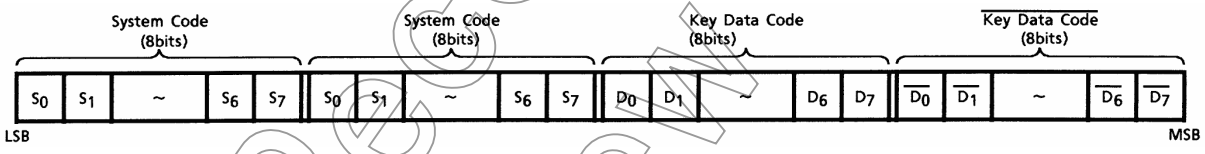
1. Key Matrix

The TC9243APG and TC9243AFG enable the setting of a maximum of thirty-two (32) keys through combining the "K_0~K_7" and "T_0~T_3" keys. Furthermore, System Codes are settable in seven (7) bits through combining the "K_0~K_6" and "CODE" keys.



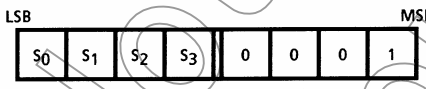
- The keys "K_{08}", "16", "24" and "32" (the shift keys) can be pushed simultaneously with other keys (the normal keys).
  However, the simultaneous keying of either shift keys or normal keys is prohibited.
- The system code setting is done through the use of the diode jumper between the "CODE" lines and the "K_0~K_6" lines.
  With the diode jumper, the data code will become "1".
  However, if the setting of the "CODE" and "K_0~K_6" keys is only at one point, the keys are connectable directly without using the diode jumper.
  Furthermore, the "S_7" key is fixed at "1" and cannot be changed.

2. Data Format



Note 1: "80H~8FH" out of the system codes are free codes.

Although freely available in principle, these codes may already be used by other equipment. There is, therefore, a risk of interference occurring.



Other system codes have been customized and their general use is therefore prohibited.
Toshiba will assume no responsibility for interference and other problems that may result from the use of other system codes.

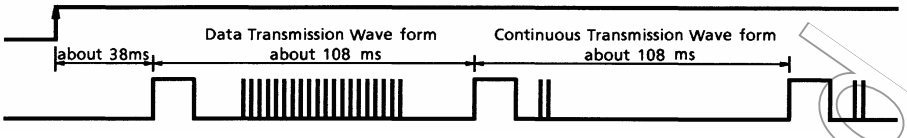
3. Key Data Code

Key No.	Tn	Kn	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
K_{01}	T_0	K_0	1	0	0	0	0	• Shift-key data • "000" except dual keying		
K_{02}		K_1	0	1	0	0	0			
K_{03}		K_2	1	1	0	0	0			
K_{04}		K_3	0	0	1	0	0			
K_{05}		K_4	1	0	1	0	0			
K_{06}		K_5	0	1	1	0	0			
K_{07}		K_6	1	1	1	0	0			
K_{08}		K_7	• Normal-key data • "00000" except dual keying.					1	0	0
K_{09}	T_1	K_0	1	0	0	1	0	• Shift-key data • "000" except dual keying		
K_{10}		K_1	0	1	0	1	0			
K_{11}		K_2	1	1	0	1	0			
K_{12}		K_3	0	0	1	1	0			
K_{13}		K_4	1	0	1	1	0			
K_{14}		K_5	0	1	1	1	0			
K_{15}		K_6	1	1	1	1	0			
K_{16}		K_7	• Normal-key data • "00000" except dual keying.					1	1	0
K_{17}	T_2	K_0	1	0	0	0	1	• Shift-key data • "000" except dual keying		
K_{18}		K_1	0	1	0	0	1			
K_{19}		K_2	1	1	0	0	1			
K_{20}		K_3	0	0	1	0	1			
K_{21}		K_4	1	0	1	0	1			
K_{22}		K_5	0	1	1	0	1			
K_{23}		K_6	1	1	1	0	1			
K_{24}		K_7	• Normal-key data • "00000" except dual keying.					1	0	1
K_{25}	T_3	K_0	1	0	0	1	1	• Shift-key data • "000" except dual keying		
K_{26}		K_1	0	1	0	1	1			
K_{27}		K_2	1	1	0	1	1			
K_{28}		K_3	0	0	1	1	1			
K_{29}		K_4	1	0	1	1	1			
K_{30}		K_5	0	1	1	1	1			
K_{31}		K_6	1	1	1	1	1			
K_{32}		K_7	• Normal-key data • "00000" except dual keying.					1	1	1

- Normal keys: K_{01}~K_{07}, K_{09}~K_{15}, K_{17}~K_{23}, K_{25}~K_{31}
- Shift keys: K_{08}, K_{16}, K_{24}, K_{32}

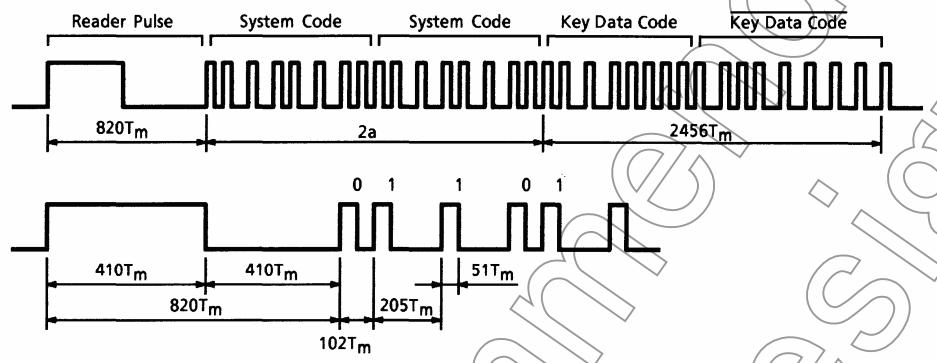
4. TX_{OUT} Output Waveform

Key ON

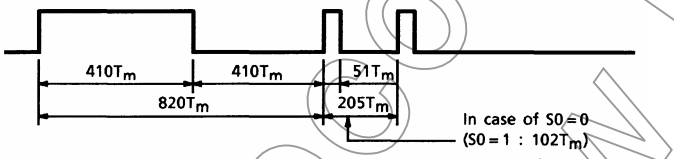


Note 2: In case of f_{OSC} = 455 kHz

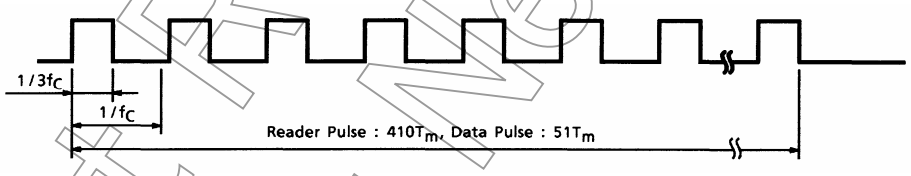
Data Transmission Waveform



Continuous Transmission Waveform



Carrier Waveform



$T_m = 5/f_{OSC}$: system clock

a: system code output time

$f_C = f_{OSC}/12$

When the oscillation frequency is 455 kHz, the signal is output after being pulse-modulated by 37.9 kHz at a duty ratio of 1/3, in 1/12 division, by the carrier generation circuit.

Caution

In preparing receiving software, strictly adhere to the following instructions:

- In the case of system codes, the same code is transmitted twice. Therefore always decode these two codes and determine whether they agree with each other.
- In the case of key data codes, always decode the key data code and its reversed code and determine whether they agree with each other.

Maximum Ratings (Ta = 25°C)

Characteristic	Symbol	Rating	Unit
Supply voltage	V_{DD}	−0.3~5.0	V
Input voltage	V_{IN}	VSS − 0.3~V_{DD} + 0.3	V
Output current	I_{OUT}	−20	mA
Power dissipation	P_D	350 (300) (Note 3)	mW
Operating temperature	T_{opr}	−20~75	°C
Storage temperature	T_{stg}	−40~125	°C

Note 3: The value shown in parentheses applies to the TC9243FG.

Electrical Characteristics

Recommended Operating Conditions

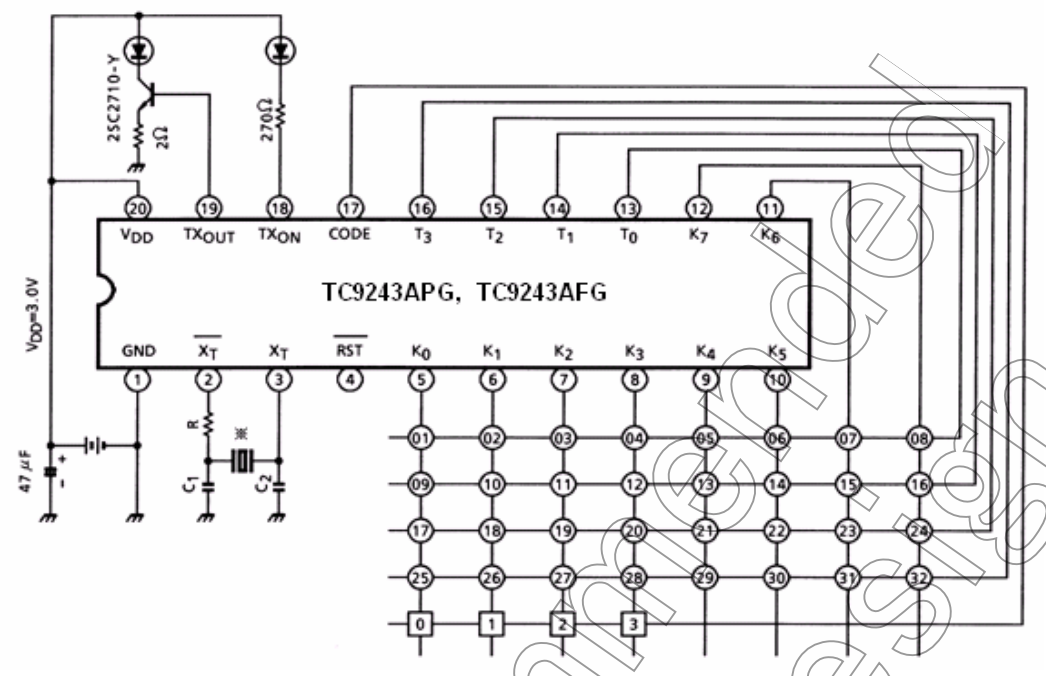
(unless otherwise specified, V_{DD} = 3.0 V, Ta = 25°C; for items with an asterisk (*), Ta = −25~75°C)

Characteristic		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Operating supply voltage *		V_{DD}	—	—	2.0	—	4.0	V
Oscillation frequency *		f_{OSC}	—	—	400	—	800	kHz
Input voltage	"H" level	V_{IH1}	—	(Except $\overline{RST}$)	V_{DD} × 0.7	—	V_{DD}	V
	"L" level	V_{IL1}	—	(Except $\overline{RST}$)	0	—	V_{DD} × 0.3	
Input voltage	"H" level	V_{IH2}	—	($\overline{RST}$)	V_{DD} × 0.8	—	V_{DD}	V
	"L" level	V_{IL2}	—	($\overline{RST}$)	0	—	V_{DD} × 0.2	

DC Characteristics (unless otherwise specified, V_{DD} = 3.0 V, Ta = 25°C)

Characteristic		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Operating supply current		I_{DD}	—	f_{OSC} = 455 kHz	—	—	1.0	MA
Static supply current		I_{QD}	—	During "Hold"	—	—	1.0	μA
Pull-down resistor		R_D	—	(K_0~K_7)	100	—	400	kΩ
Pull-up resistor		R_U	—	($\overline{RST}$)	25	—	100	kΩ
Output current	"H" level	I_{OH}	—	(TX_{OUT}) V_{OH} = 1.5 V	−10	—	—	mA
	"L" level	I_{OL}	—	(TX_{ON}) V_{OL} = 1.5 V	5	—	—	
Input leak current		I_{LI}	—	V_{IN} = V_{DD}, V_{SS}	−1.0	—	1.0	μA

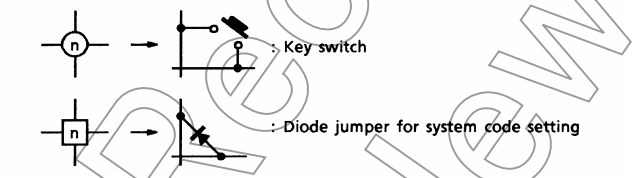
Application Circuit



Note 4: Ceramic oscillator CSB455E (Murata Seisakusho) $C_1 = C_2 = 100$ pF $R = 6.8$ kΩ

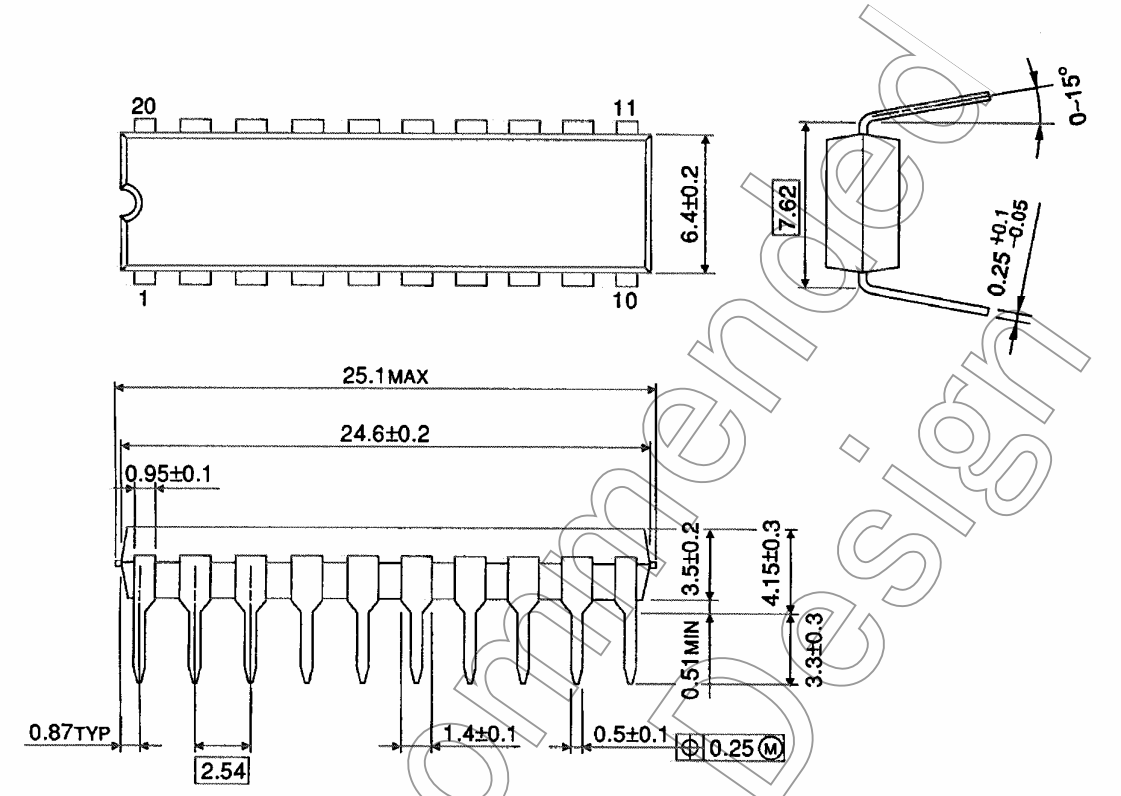
FCR455K3 (TDK) $C_1 = C_2 = 220$ pF $R = 2.2$ kΩ

or equivalent



Package Dimensions

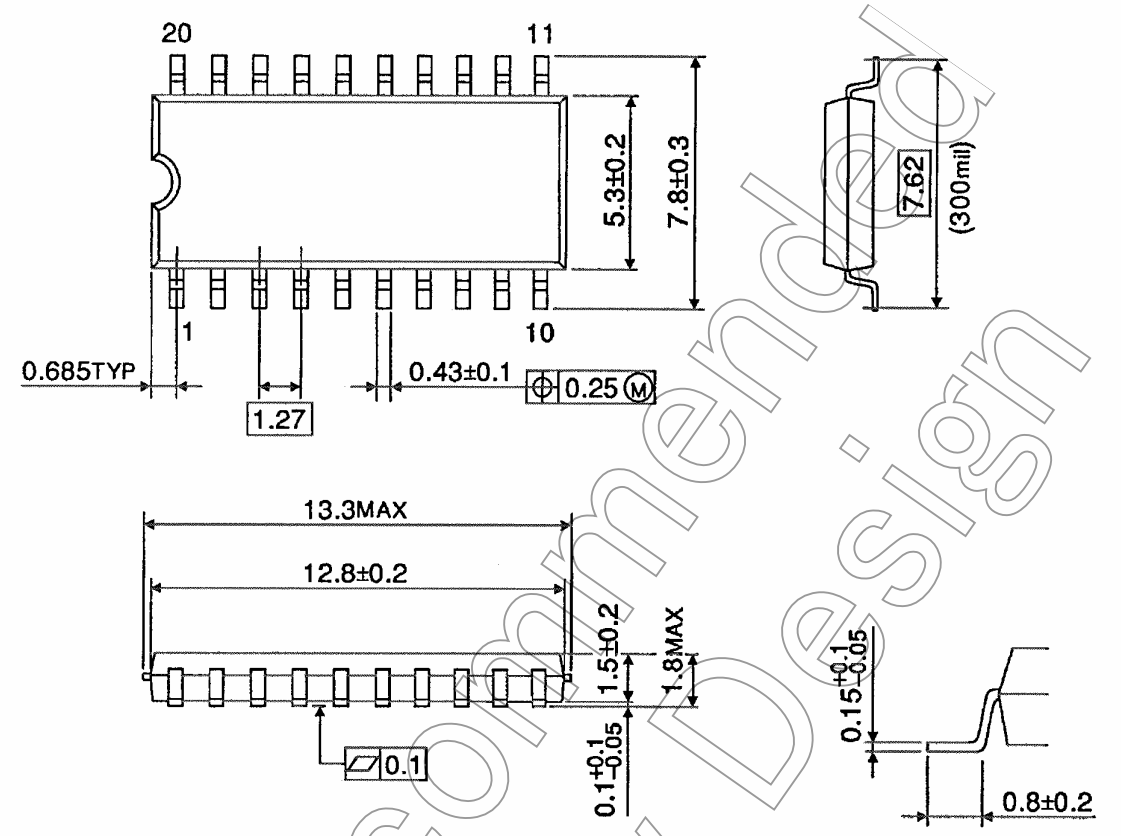
DIP20-P-300-2.54A Unit : mm



Weight: 1.4 g (typ.)

Package Dimensions

SOP20-P-300-1.27 Unit : mm



Weight: 0.48 g (typ.)

The following conditions apply to solderability:

- Solderability

  (1) Use of Sn-63Pb solder bath
  - solder bath temperature = 230°C
  - dipping time = 5 seconds
  - number of times = once
  - use of R-type flux

  (2) Use of Sn-3.0Ag-0.5Cu solder bath
  - solder bath temperature = 245°C
  - dipping time = 5 seconds
  - number of times = once
  - use of R-type flux

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