EM78F561/661N

8-Bit Microcontroller

Product Specification

DOC. VERSION 2.7

ELAN MICROELECTRONICS CORP.

September 2016

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APPENDIX

Specification Revision History

Doc. Version	Revision Description	Date
1.0	Initial released version	2009/06/17
2.0	1. Deleted ICE652N information. 2. Added CPU operation with Green/Idle mode, also added TBRD instructions. 3. Indicated the use of ICE660N to simulate EM78F661N.	2009/09/08
2.1	1. Redefined the CPU Operation Mode information. 2. Added IRC mode selection information on Bank 1 R8<7,6> and Word 1<12>.	2010/01/06
2.2	1. Revised the Pin Description format and Wake-up signal table. 2. Combined Specs of EM78F561N and EM78F661N.	2010/04/10
2.3	1. Added LVR parameter to *DC Electrical Characteristics.* 2. Modified the notes of the instruction set. 3. Added Ordering and Manufacturing Information. 4. Modified the product code description. 5. Changed the LVR of feature from CPU Configuration to Peripheral Configuration. 6. Deleted the machine code 7. Added EM78Fx61N 14-pin SOP Package Type	2013/09/18
2.4	1. Added power consumption for EEPROM 2. Added HLP in Bit 9 of Code Option Word 1	2014/08/28
2.5	Modified the CKR table and added Notes.	2015/06/05
2.6	1. Added User Application Note. 2. Removed the Material Type in Package Type in the Feature section. 3. Modified the ordering and Manufacturing information. 4. Removed the Material Type in Package Type in the Appendix	2016/03/25
2.7	1.Removed the parameter of LVR reset level (Ta is -40~85℃) in the DC Electrical Characteristics.	2016/09/14

User Application Note

(Before using this IC, take a look at the following description note, it includes important messages.)

1. If user changes the IRC frequency from A-frequency to B-frequency, the MCU needs to wait for some time for it to work. The waiting time corresponds to the B-frequency.
2. The operation mode setting is different between EM78F561N/F661N and UIT660N.
3. To obtain an accurate value, it is necessary to avoid any data transition on the I/O pins during AD conversion.
4. The noise rejection function is turned off under Low Crystal Oscillator (LXT2) and Sleep mode.

1 General Description

The EM78Fx61N are 8-bit microprocessors designed and developed with low-power, high-speed CMOS technology, and high noise immunity. They have on-chip 1K×13-bit Electrical Flash Memory and the EM78F661N has 128×8-bit in-system programmable EEPROM, and are provided with three protection bits to prevent intrusion of user's Flash memory code. Twelve Code option bits are also available to meet user's requirements.

With its enhanced Flash-ROM features, the EM78Fx61N provides a convenient way of developing and verifying user's programs. Moreover, this Flash-ROM device offers the advantages of easy and effective program updates, using development and programming tools. Users can avail of the ELAN Writer to easily program their development codes.

2 Features

- CPU configuration
  - 1K×13 bits on-chip Flash memory
  - 48×8 bits on-chip registers (SRAM)
  - 128 bytes in-system programmable EEPROM*
    (Only for EM78F661N)
    **Endurance: 1,000,000 write/erase cycles*
  - More than 10 years data retention
  - 8-level stacks for subroutine nesting
  - Less than 1.5 mA at 5V / 4 MHz
  - Typically 20 μA, at 3V / 32kHz
  - Typically 1.5 μA, during sleep mode
- I/O port configuration
  - 3 bidirectional I/O ports: P5, P6, and P8
  - 14 I/O pins
  - Wake-up port : P6
  - High sink port : P6
  - 6 programmable pull-high I/O pins
  - 5 programmable pull-down I/O pins
  - 6 programmable open-drain I/O pins
  - External interrupt with Wake-up: P60
- Operating voltage range
  - 2.4V~5.5V at -40°C~85°C (Industrial)
  - 2.2V~5.5V at 0°C~70°C (Commercial)
- Operating frequency range (base on two clocks)
  - Crystal mode: DC~16 MHz @ 4.5V~5.5V
    DC~8 MHz @ 3V~5.5V
    DC~4 MHz @ 2.2V~5.5V
  - ERC mode: DC~16 MHz @ 4.5V~5.5V;
    DC~8 MHz @ 3V~5.5V
    DC~4 MHz @ 2.2V~5.5V
  - IRC mode : DC~16 MHz @ 4.5V~5.5V;
    DC~4 MHz @ 2.2V~5.5V

Internal RC Frequency	Drift Rate			
	Temperature (-40°C~85°C)	Voltage (2.4V~5.5V)	Process	Total
4 MHz	± 3%	± 5%	± 2.5%	± 10.5%
16 MHz	± 3%	± 5%	± 2.5%	± 10.5%
8 MHz	± 3%	± 5%	± 2.5%	± 10.5%

- Six available interrupts
  - Internal interrupt: 3
  - External interrupt: 3
- 6 channels Analog-to-Digital Converter with 10-bit resolution
- One set comparator
  Offset voltage: smaller than 5 mV
- One 8-bit Timer/Counter
  - TC3: Timer/Counter/PDO (programmable divider output)/PWM (pulse width modulation)
- Peripheral configuration
  - 8-bit real time clock only (TCC) with overflow interrupt
  - External interrupt input pin
  - 2/4/8/16 clocks per instruction cycle selected by code option
  - Power down (Sleep) mode
  - High EFT immunity
  - 3 programmable Level Voltage Reset
    LVR: 4.0V, 3.5V, 2.7V
- Single instruction cycle commands
- Special Features
  - Programmable free running Watchdog Timer
  - Power-on voltage detector available (2.0V ~ 2.1V)
- Package Type:
  - 10-pin MSOP 118mil : EM78Fx61NMS10
  - 14-pin SOP 150mil : EM78Fx61NSO14
  - 16-pin DIP 300mil : EM78Fx61NAD16
  - 16-pin SOP 150mil : EM78Fx61NASO16A

NOTE: *These are Green Products which do not contain hazardous substances*

3 Pin Assignment

3.1 10-Pin MSOP

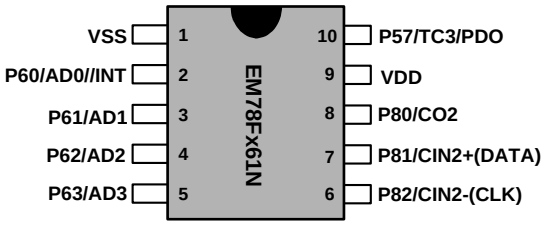


Figure 3-1a EM78Fx61NMS10

3.2 16-Pin DIP/SOP

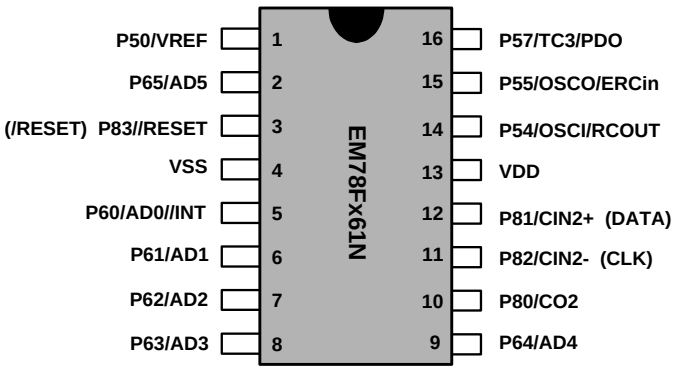


Figure 3-1b EM78Fx61NAD16 / EM78Fx61NASO16A

3.3 14-Pin SOP

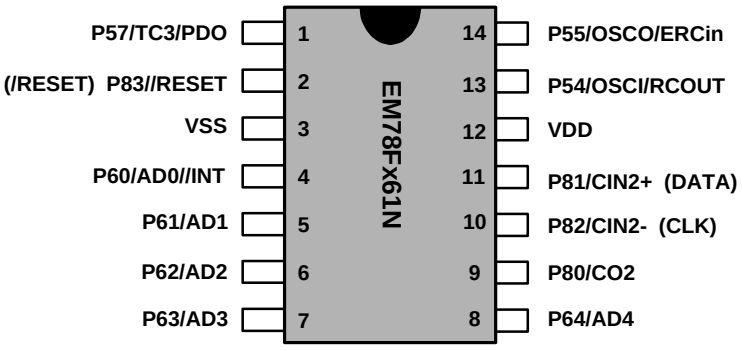


Figure 3-1c EM78Fx61NSO14

4 Pin Description

Legend: **ST:** *Schmitt Trigger input* **AN:** *Analog pin*
CMOS: *CMOS output* **XTAL:** *Oscillation pin for crystal/resonator*

Name	Function	Input Type	Output Type	Description
P50/VREF	P50	ST	CMOS	Bidirectional I/O pin with programmable pull-down
	VREF	AN	–	ADC external voltage reference
P54/OSCI/RCOUT	P54	ST	CMOS	Bidirectional I/O pin
	OSCI	XTAL	–	Clock input of crystal/resonator oscillator
	RCOUT	–	CMOS	Clock output of internal RC oscillator Clock output of external RC oscillator (open-drain)
P55/OSCO/ERCin	P55	ST	CMOS	Bidirectional I/O pin
	OSCO	–	XTAL	Clock output of crystal/resonator oscillator
	ERCin	AN	–	External RC input pin
P57/TC3/PDO	P57	ST	CMOS	Bidirectional I/O pin
	TC3	ST	–	Timer 3 clock input
	PDO	–	CMOS	Programmable divider output
P60/AD0//INT	P60	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	AD0	AN	–	ADC Input 0
	/INT	ST	–	External interrupt pin
P61/AD1	P61	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	AD1	AN	–	ADC Input 1
P62/AD2	P62	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	AD2	AN	–	ADC Input 2
P63/AD3	P63	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	AD3	AN	–	ADC Input 3
P64/AD4	P64	ST	CMOS	Bidirectional I/O pin with programmable pull-high, open-drain, and pin change wake-up
	AD4	AN	–	ADC Input 4
P65/AD5	P65	ST	CMOS	Bidirectional I/O pin with programmable pull-high, open-drain, and pin change wake-up
	AD5	AN	–	ADC Input 5

(Continuation)

Name	Function	Input Type	Output Type	Description
P80/CO2	P80	ST	CMOS	Bidirectional I/O pin
	CO2	–	CMOS	Output of Comparator 2
(DATA)	**(DATA)**	ST	CMOS	DATA pin for Writer programming
P81/CIN2+	P81	ST	CMOS	Bidirectional I/O pin
	CIN2+	AN	–	Non-inverting end of Comparator 2
(CLK)	**(CLK)**	ST	–	CLOCK pin for Writer programming
P82/CIN2-	P82	ST	CMOS	Bidirectional I/O pin
	CIN2-	AN	–	Inverting end of Comparator 2
P83//RESET **(/RESET)**	P83	ST	CMOS	Bidirectional I/O pin
	/RESET	ST	–	Internal pull-high reset pin
	(/RESET)	ST	–	/RESET pin for Writer programming
VDD	VDD	Power	–	Power
VSS	VSS	Power	–	Ground

5 Block Diagram

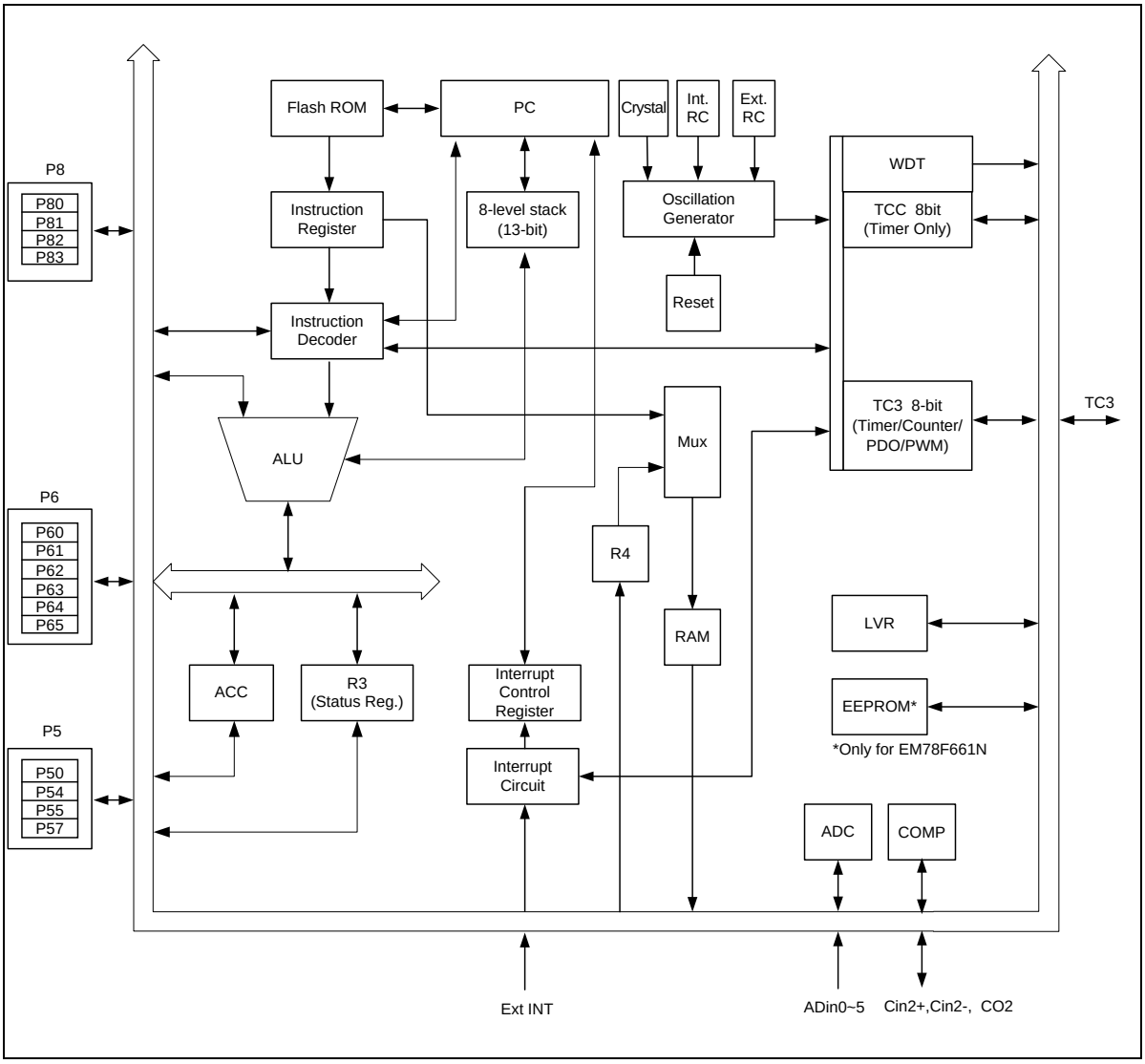


Figure 5-1 Functional Block Diagram

6 Functional Description

6.1 Operational Registers

6.1.1 R0 (Indirect Addressing Register)

R0 is not a physically implemented register. It is used as an indirect addressing pointer. Any instruction using R0 as a pointer actually accesses data pointed by the RAM Select Register (R4).

6.1.2 R1 (Timer Clock)

R1 is incremented by the instruction cycle clock. It is writable and readable as any other registers. It is defined by resetting PSTE (CONT-3).

The prescaler is assigned to TCC, if the PSTE bit (CONT-3) is reset. The content of the prescaler counter is cleared only when the TCC register is written with a value.

6.1.3 R2 (Program Counter and Stack)

Depending on the device type, R2 and hardware stack are 10-bit wide. The structure is depicted in Figure 6-1 below.

The configuration structure generates 1K×13 bits on-chip Flash ROM addresses to the relative programming instruction codes. One program page is 1024 words long.

R2 is set as all "**0**"s when under a reset condition.

"JMP" instruction allows direct loading of the lower 10 program counter bits. Thus, "JMP" allows the PC to go to any location within a page.

"CALL" instruction loads the lower 10 bits of the PC, and PC+1 are pushed onto the stack. Thus, the subroutine entry address can be located anywhere within a page.

"RET" ("RETL k", "RETI") instruction loads the program counter with the contents of the top-level stack.

"ADD R2, A" allows a relative address to be added to the current PC, and the ninth and above bits of the PC will increase progressively.

"MOV R2, A" allows loading an address from the "A" register to the lower 8 bits of the PC, and the ninth and tenth bits of the PC remain unchanged.

Any instruction except “ADD R2,A” that is written to R2 (e.g., "MOV R2, A", "BC R2, 6") will cause the ninth bit and the tenth bit (A8~A9) of the PC to remain unchanged.

All instructions are single instruction cycle (fclk/2, fclk/4, fclk/8, or fclk/16) except for the instruction that would change the contents of R2 and “TBRD” instruction. The “TBRD” instructions need two instruction cycles.

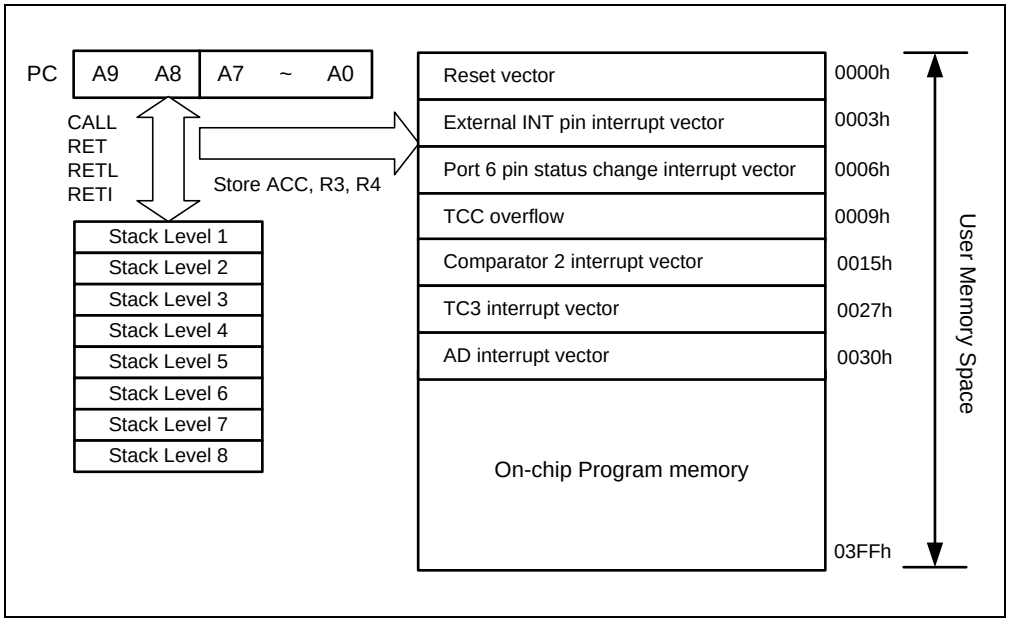


Figure 6-1 Program Counter Organization

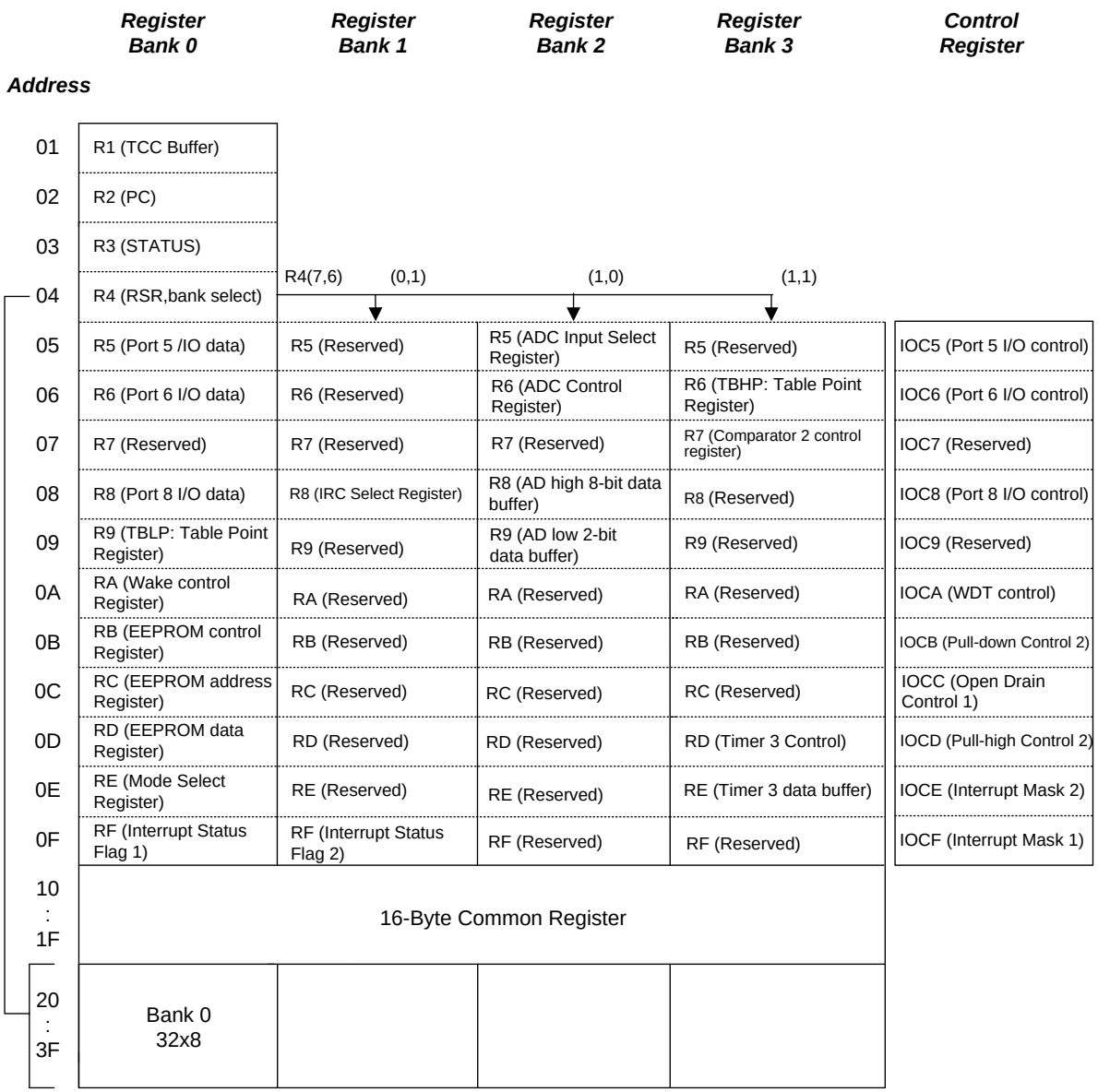


Figure 6-2 Data Memory Configuration

6.1.4 R3 (Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	T	P	Z	DC	C

Bits 7 ~ 5 Not used, set to "**0**" at all time

Bit 4 (T): Time-out bit

Set to "**1**" with the "SLEP" and "WDTC" commands, or during power up and reset to "**0**" by WDT time-out.

Bit 3 (P): Power down bit

Set to 1 during power-on or by a "WDTC" command and reset to "0" by a "SLEP" command.

Bit 2 (Z): Zero flag

Set to "**1**" if the result of an arithmetic or logic operation is zero.

Bit 1 (DC): Auxiliary carry flag

Bit 0 (C): Carry flag

6.1.5 R4 (RAM Select Register)

Bits 7 ~ 6: Used to select Bank 0 ~ Bank 3

Bits 5 ~ 0: Used to select registers (Address: 00~3F) in indirect addressing mode.

See the data memory configuration in Figure 6-2 above.

6.1.6 Bank 0 R5 ~ R6, R8 (Port 5 ~ Port 6, Port 8)

R5 ~ R6, and R8 are I/O registers.

6.1.7 Bank 0 R9 (TBLP: Table Point Register for Instruction TBRD)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RBit7	RBit6	RBit5	RBit4	RBit3	RBit2	RBit1	RBit0

Bits 7 ~ 0: These are the least 8 significant bits of address for program code.

NOTE

- *Bank 0 R9 overflow will carry to Bank 3 R6.*
- *Bank 0 R9 underflow will borrow from Bank 3 R6.*

6.1.8 Bank 0 RA (Wake-up Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMP2WE	ICWE	ADWE	EXWE	-	-	-	-

Bit 7 (CMP2WE): Comparator 2 wake-up enable bit.

0: Disable Comparator 2 wake-up

1: Enable Comparator 2 wake-up

When the Comparator 2 output status change is used to enter an interrupt vector or to wake-up the EM78Fx61N from Sleep mode, the CMP2WE bit must be set to “Enable”.

Bit 6 (ICWE): Port 6 input status change wake-up enable bit

0: Disable Port 6 input status change wake-up

1: Enable Port 6 input status change wake-up

Bit 5 (ADWE): ADC wake-up enable bit

0: Disable ADC wake-up

1: Enable ADC wake-up

When ADC Complete is used to enter an interrupt vector or to wake-up the EM78Fx61N from sleep with A/D conversion running, the ADWE bit must be set to “Enable“.

Bit 4 (EXWE): External /INT wake-up enable bit

0: Disable External /INT pin wake-up

1: Enable External /INT pin wake-up

Bits 3 ~ 0: Not used, set to “**0**” at all time

6.1.9 Bank 0 RB (EEPROM Control Register; for EM78F661N only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RD	WR	EEWE	EEDF	EEPC	-	-	-

Bit 7 (RD): Read control register

0: Does not execute EEPROM read

1: Read EEPROM contents (RD can be set by software, and cleared by hardware after Read instruction is completed).

Bit 6 (WR): Write control register

0: Write cycle to the EEPROM is completed.

1: Initiate a write cycle (WR can be set by software, and cleared by hardware after Write cycle is completed).

Bit 5 (EEWE): EEPROM Write Enable bit.

0: Prohibit write to the EEPROM

1: Allows EEPROM write cycles

Bit 4 (EEDF): EEPROM Detect Flag

0: Write cycle is completed.

1: Write cycle is unfinished.

Bit 3 (EEPC): EEPROM power-down control bit

0: Switch off the EEPROM

1: EEPROM is operating

Bits 2 ~ 0: Not used, set to "**0**" at all time

6.1.10 Bank 0 RC (128 Bytes EEPROM Address, for EM78F661N only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	EE_A6	EE_A5	EE_A4	EE_A3	EE_A2	EE_A1	EE_A0

Bits 6 ~ 0: 128 bytes EEPROM address

6.1.11 Bank 0 RD (128 Bytes EEPROM Data, only for EM78F661N)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EE_D7	EE_D6	EE_D5	EE_D4	EE_D3	EE_D2	EE_D1	EE_D0

Bits 7 ~ 0: 128 bytes EEPROM data

6.1.12 Bank 0 RE (Mode Select Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	TIMERSC	CPUS	IDLE	-	-	-	-

Bit 7: Not used, set to "**0**" at all time

Bit 6 (TIMERSC): TCC, TC3 clock source select

0: Fs is used as Fc

1: Fm is used as Fc

Bit 5 (CPUS): CPU Oscillator Source Select

0: Fs**:** Sub frequency for WDT internal RC time base

1: Fm**:** Main-oscillator clock

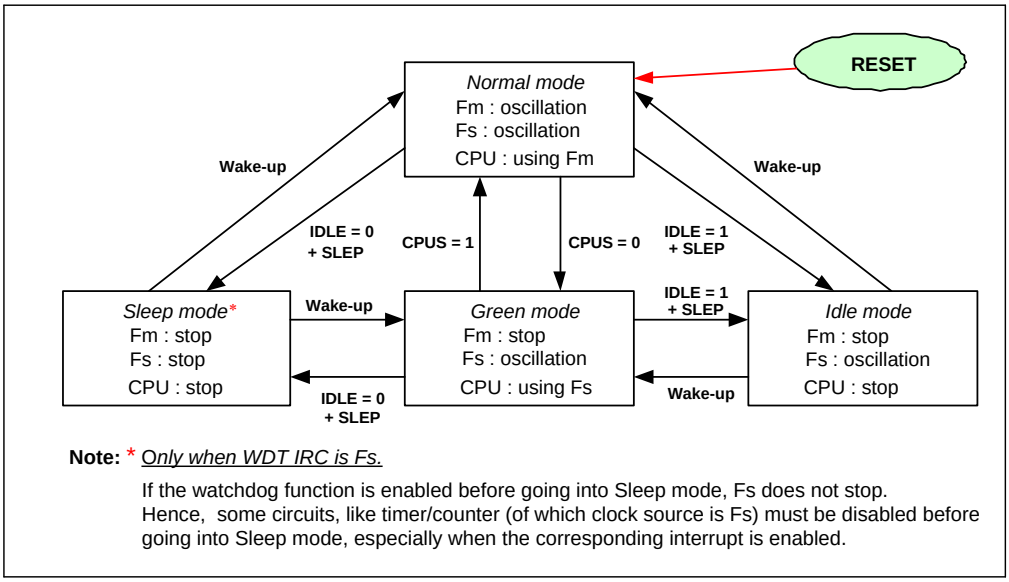
When CPUS=0, the CPU oscillator selects a sub-oscillator and the main oscillator is stopped.

Bit 4 (IDLE): Idle Mode Enable Bit

0: IDLE="**0**" + SLEP instruction → Sleep mode

1: IDLE="**1**" + SLEP instruction → Idle mode

■ CPU Operation Mode



Note: * *Only when WDT IRC is Fs.*

If the watchdog function is enabled before going into Sleep mode, Fs does not stop. Hence, some circuits, like timer/counter (of which clock source is Fs) must be disabled before going into Sleep mode, especially when the corresponding interrupt is enabled.

Figure 6-3 CPU Operation Mode

Oscillator (Normal Mode Source)	CPU Mode Status	Oscillator Stable Time (s)[1]	Count from Normal/Green (CLK)[2]
Crystal ; 1M ~ 16 MHz	Sleep/Idle → Normal	0.5 ms ~ 2 ms	254 CLK
	Green → Normal		254 CLK
	Sleep/Idle → Green	< 100 µs	32 CLK
ERC ; 3.5 MHz	Sleep/Idle → Normal	< 5 µs	32 CLK
	Green → Normal		
	Sleep/Idle → Green	< 100 µs	
IRC ; 4M, 8M, 16 MHz	Sleep/Idle → Normal	< 2 µs	32 CLK
	Green → Normal		
	Sleep/Idle → Green	< 100 µs	

[1] *Stabilization time for the oscillator depends on the oscillator characteristics.*

[2] *After the oscillator has stabilized, the CPU will count 254/32 CLK in Normal/Green mode and continue to work in Normal/Green mode.*

Ex 1: *When the 4 MHz IRC wakes-up from Sleep mode to Normal mode, its total wake-up time is 2 µs + 32 CLK @ 4 MHz*

Ex 2: *When the 4 MHz IRC wakes-up from Sleep mode to Green mode, its total wake-up time is 100 µs + 32 CLK @ 16kHz*

Bits 3 ~ 0: Not used, set to "**0**" at all time

6.1.13 Bank 0 RF (Interrupt Status Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	ADIF	-	-	-	EXIF	ICIF	TCIF

***NOTE:** "1" means with interrupt request "0" means no interrupt occurs*

Bit 7: Not used, set to "**0**" at all time

Bit 6 (ADIF): Interrupt flag for analog to digital conversion. Set when AD conversion is completed, reset by software.

Bits 5 ~ 3: Not used, set to "**0**" at all time

Bit 2 (EXIF): External interrupt flag. Set by a falling edge on the /INT pin, reset by software.

Bit 1 (ICIF): Port 6 input status change interrupt flag. Set when Port 6 input changes, reset by software.

Bit 0 (TCIF): TCC overflow interrupt flag. Set when TCC overflows, reset by software.

NOTE

- *RF can be cleared by instruction but cannot be set.*
- *IOCF is an interrupt mask register.*
- *The result of reading RF is the "Logic AND" of RF and IOCF.*

6.1.14 R10 ~ R3F

These are all 8-bit general-purpose registers.

6.1.15 Bank 1 R5~R7

These are reserved registers.

6.1.16 Bank 1 R8 (IRC Select Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RCM1	RCM0	-	-	-	-	-	-

Bits 7 ~ 6 (RCM1 ~ RCM0): IRC mode select bits. Bank 1 R8<7, 6> is enabled when Word 1<12> COBS0 = "1".

Writer Trim IRC	Bank 1 R8<7,6>		Frequency	Operating Voltage Range	Stable Time
	RCM1	RCM0			
4 MHz	**0**	**0**	**4 MHz ± 2.5%**	2.2V ~ 5.5V	< 5µs
	0	1	16 MHz ± 10%	4.5V ~ 5.5V	< 1.5µs
	1	0	8 MHz ± 10%	3.0V ~ 5.5V	< 3µs
	1	1	x	-	-
16 MHz	0	0	4 MHz ± 10%	2.2V ~ 5.5V	< 6µs
	0	**1**	**16 MHz ± 2.5%**	4.5V ~ 5.5V	< 1.25µs
	1	0	8 MHz ± 10%	3.0V ~ 5.5V	< 3µs
	1	1	x	-	-
8 MHz	0	0	4 MHz ± 10%	2.2V ~ 5.5V	< 6µs
	0	1	16 MHz ± 10%	4.5V ~ 5.5V	< 1.5µs
	1	**0**	**8 MHz ± 2.5%**	3.0V ~ 5.5V	< 2.5µs
	1	1	x	-	-

NOTE

- *The initial values of Bank1 R8<7, 6> will be kept the same as Word 1<3, 2>.*
- *If user changes the IRC frequency from A-frequency to B-frequency, the MCU needs to wait for some time for it to work. The waiting time corresponds to the B-frequency.*

■ **Examples:**

1st Step: When user selects the 4 MHz at the Writer, the initial values of Bank 1 R8<7,6> would be "00", the same as the value of Word 1<3,2> is "00". If the MCU is free-running, it will work at 4 MHz ± 2.5%. Refer to the table below.

Writer Trim IRC	Bank 1 R8<7,6>		Frequency	Operating Voltage Range	Stable Time
	RCM1	RCM0			
4 MHz	**0**	**0**	**4 MHz ± 2.5%**	2.2V ~ 5.5V	< 5µs
	0	1	16 MHz ± 10%	4.5V ~ 5.5V	< 1.5µs
	1	0	8 MHz ± 10%	3.0V ~ 5.5V	< 3µs
	1	1	x	-	-

2nd Step: If it is desired to set Bank 1 R8<7,6> = "01" while the MCU is working at 4 MHz ± 2.5%, the MCU needs to hold for 1.5µs, then it will continue to work at 16 MHz ± 10%.

Writer Trim IRC	Bank 1 R8<7,6>		Frequency	Operating Voltage Range	Stable Time
	RCM1	RCM0			
4 MHz	0	0	4 MHz ± 2.5%	2.2V ~ 5.5V	< 5 µs
	0	**1**	**16 MHz ± 10%**	4.5V ~ 5.5V	< 1.5µs
	1	0	8 MHz ± 10%	3.0V ~ 5.5V	< 3µs
	1	1	x	-	-

3rd Step: If it is desired to set Bank 1 R8<7,6> = "10" while the MCU is working at 16 MHz ± 10%, the MCU needs to hold for 3µs, then it will continue to work at 8 MHz ± 10%.

Writer Trim IRC	Bank 1 R8<7,6>		Frequency	Operating Voltage Range	Stable Time
	RCM1	RCM0			
4 MHz	0	0	4 MHz ± 2.5%	2.2V ~ 5.5V	< 5µs
	0	1	16 MHz ± 10%	4.5V ~ 5.5V	< 1.5µs
	1	**0**	**8 MHz ± 10%**	3.0V ~ 5.5V	< 3µs
	1	1	x	-	-

4th Step: If it is desired to set Bank 1 R8<7,6> = "00" while the MCU is working at 8 MHz ± 10%, the MCU needs to hold for 5µs, then it will continue to work at 4 MHz ± 2.5%.

Writer Trim IRC	Bank 1 R8<7,6>		Frequency	Operating Voltage Range	Stable Time
	RCM1	RCM0			
4 MHz	**0**	**0**	**4 MHz ± 2.5%**	2.2V ~ 5.5V	< 5µs
	0	1	16 MHz ± 10%	4.5V ~ 5.5V	< 1.5µs
	1	0	8 MHz ± 10%	3.0V ~ 5.5V	< 3µs
	1	1	x	-	-

6.1.17 Bank 1 R9~RE

These are reserved registers.

6.1.18 Bank 1 RF (Interrupt Status Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMP2IF	-	TC3IF	-	-	-	-	-

Bit 7 (CMP2IF): Comparator 2 Interrupt Flag. Set when a change occurs in the Comparator 2 output, reset by software.

Bit 6: Not used, set to "**0**" at all time

Bit 5 (TC3IF): 8-bit Timer/Counter 3 Interrupt Flag.

Bits 4 ~ 0: Not used, set to "**0**" at all time

NOTE

The Interrupt flag is automatically set by hardware. It must be cleared by software.

6.1.19 Bank 2 R5 AISR (ADC Input Select Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0

The AISR register individually defines the Port 6 pins as analog input or digital I/O.

Bits 7 ~ 6: Not used, set to "**0**" at all time

Bit 5 (ADE5): AD converter enable bit of P65 pin

0: Disable ADC5, P65 functions as I/O pin

1: Enable ADC5 to function as analog input pin

Bit 4 (ADE4): AD converter enable bit of P64 pin

0: Disable ADC4, P64 act as I/O pin

1: Enable ADC4 to act as analog input pin

Bit 3 (ADE3): AD converter enable bit of P63 pin

0: Disable ADC3, P63 act as I/O pin

1: Enable ADC3 to act as analog input pin.

Bit 2 (ADE2): AD converter enable bit of P62 pin

0: Disable ADC2, P62 act as I/O pin

1: Enable ADC2 to act as analog input pin

Bit 1 (ADE1): AD converter enable bit of P61 pin

0: Disable ADC1, P61 act as I/O pin

1: Enable ADC1 to act as analog input pin

Bit 0 (ADE0): AD converter enable bit of P60 pin

0: Disable ADC0, P60 act as I/O pin

1: Enable ADC0 to act as analog input pin

The following shows the priority of P60/ADC0//INT.

P60 / ADC0 / /INT Pin Priority		
High	Medium	Low
/INT	ADC0	P60

6.1.20 Bank 2 R6 ADCON (A/D Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VREFS	CKR1	CKR0	ADRUN	ADPD	ADIS2	ADIS1	ADIS0

Bit 7 (VREFS): Input source of the Vref of the ADC.

0: Vref of the ADC is connected to Vdd (default value), and the P50/VREF pin carries out the function of P50

1: Vref of the ADC is connected to P50/VREF

Bit 6 ~ Bit 5 (CKR1 ~ CKR0): Prescaler of ADC oscillator clock rate

00 = 1**:** 4 (default value)

01 = 1**:** 16

10 = 1**:** 1

11 = 1**:** 2

CKR1/CKR0	EM78F561N/F661N		UIT660N	
	Operation Mode	Max. Operation Frequency	Operation Mode	Max. Operation Frequency
00	$F_{OSC}/4$	4 MHz	$F_{OSC}/4$	4 MHz
01	$F_{OSC}/16$	16 MHz	F_{OSC}	1 MHz
10	F_{OSC}	1 MHz	$F_{OSC}/16$	16 MHz
11	$F_{OSC}/2$	2 MHz	$F_{OSC}/2$	2 MHz

Bit 4 (ADRUN): ADC starts to run

0: Reset on completion of AD conversion. This bit cannot be reset by software.

1: A/D conversion is started. This bit can be set by software.

Bit 3 (ADPD): ADC Power-down mode

0: Switch off the resistor reference to save power even while the CPU is operating.

1: ADC is operating.

Bits 2 ~ 0 (ADIS2~ADIS0): Analog Input Select

000 = AN0/P60

001 = AN1/P61

010 = AN2/P62

011 = AN3/P63

100 = AN4/P64

101 = AN5/P65

110 = x

111 = x

The following table shows the priority of P50/VREF pin. They can only be changed when the ADIF bit and the ADRUN bit are both low.

P50/VREF Pin Priority	
High	Low
VREF	P50

6.1.21 Bank 2 R7

These are reserved registers.

6.1.22 Bank 2 R8 ADDH (AD High 8-Bit Data Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2

When A/D conversion is completed, the result of high 8-bit is loaded into the ADDH. The ADRUN bit is cleared, and the ADIF is set. R8 is read only.

6.1.23 Bank 2 R9 ADDL (AD Low 2-Bit Data Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	-	AD1	AD0

Bits 7 ~ 2: Unimplemented, read as '**0**'

Bits 1 ~ 0 (AD1~AD0): AD low 2-bit data buffer. R9 is read only.

6.1.24 Bank 2 RA~RF

These are reserved registers.

6.1.25 Bank 3 R5

These are reserved registers.

6.1.26 Bank 3 R6 (TBHP: Table Point Register for Instruction TBRD)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MLB	-	-	-	-	-	RBit9	RBit8

Bit 7 (MLB): Choosing MSB or LSB machine code to be moved to the register. The machine code is pointed by TBLP and TBHP register.

Bits 6 ~ 2: Not used, set to "**0**" at all time

Bits 1 ~ 0: These are the most two significant bits of address for program code.

6.1.27 Bank 3 R7 (CMPCON: Comparator 2 Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	CPOUT2	COS21	COS20	-	-

Bit 7 ~ Bit 5: Not used, set to "**0**" at all time

Bit 4 (CPOUT2): The result of Comparator 2 output.

Bit 3 ~ Bit 2 (COS21: COS20): Comparator 2 Select bits.

COS21	COS20	Function Description
0	0	Comparator 2 is not used, P80 acts as normal I/O pin
0	1	Act as a Comparator 2 and P80 acts as normal I/O pin
1	0	Act as a Comparator 2 and P80 act as Comparator 2 output pin (CO)
1	1	Not used

Bit 1 ~ Bit 0: Not used, set to "**0**" at all time

6.1.28 Bank 3 R8 ~ RC

These are reserved registers.

6.1.29 Bank 3 RD TC3CR (Timer 3 Control)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC3FF1	TC3FF0	TC3S	TC3CK2	TC3CK1	TC3CK0	TC3M1	TC3M0

Bits 7 ~ 6 (TC3FF1 ~ TC3FF0): Timer/Counter 3 flip-flop control

TC3FF1	TC3FF0	Operating Mode
0	0	Clear
0	1	Toggle
1	0	Set
1	1	Reserved

Bit 5 (TC3S): Timer/Counter 3 start control

0: Stop and clear the counter

1: Start

Bits 4 ~ 2 (TC3CK2 ~ TC3CK0): Timer/Counter 3 clock source select

TC3CK2	TC3CK1	TC3CK0	Clock Source	Resolution	Max. Time	Resolution	Max. Time
			Normal, Idle	Fc=4M	Fc=4M	Fc=16K	Fc=16K
0	0	0	$Fc/2^{11}$	512 µs	131072 µs	128 ms	32768 ms
0	0	1	$Fc/2^{7}$	32 µs	8192 µs	8 ms	2048 ms
0	1	0	$Fc/2^{5}$	8 µs	2048 µs	2 ms	512 ms
0	1	1	$Fc/2^{3}$	2 µs	512 µs	500 µs	128 ms
1	0	0	$Fc/2^{2}$	1 µs	256 µs	250 µs	64 ms
1	0	1	$Fc/2^{1}$	500 ns	128 µs	125 µs	32 ms
1	1	0	Fc	250 ns	64 µs	62.5 µs	16 ms
1	1	1	External clock (TC3 pin)	-	-	-	-

Bits 1 ~ 0 (TC3M1 ~ TC3M0): Timer/Counter 3 operating mode select

TC3M1	TC3M0	Operating Mode
0	0	Timer/Counter
0	1	Reserved
1	0	Programmable Divider Output
1	1	Pulse Width Modulation Output

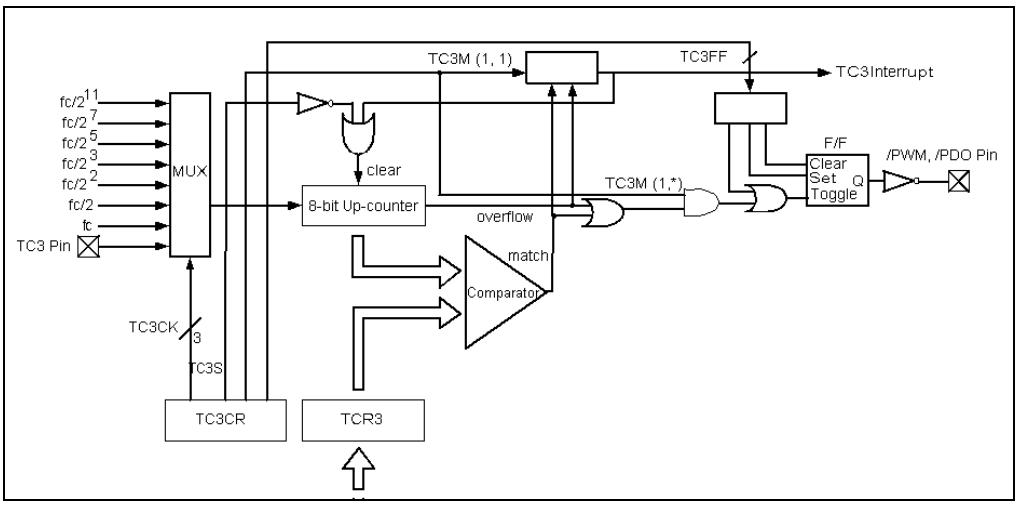


Figure 6-4 Timer / Counter 3 Configuration

In Timer mode, counting up is performed using the internal clock (rising edge trigger). When the contents of the up-counter match the TCR3, then interrupt is generated and the counter is cleared. Counting up resumes after the counter is cleared.

In Counter mode, counting up is performed using the external clock input pin (TC3 pin). When the contents of the up-counter match the TCR3, then interrupt is generated and the counter is cleared. Counting up resumes after the counter is cleared.

In Programmable Divider Output (PDO) mode, counting up is performed using the internal clock. The contents of TCR3 are compared with the contents of the up-counter. The F/F output is toggled and the counter is cleared each time a match is found. The F/F output is inverted and output to /PDO pin. This mode can generate 50% duty pulse output. **The F/F can be initialized by the program and it is initialized to "0" during reset**. A TC3 interrupt is generated each time a /PDO output is toggled.

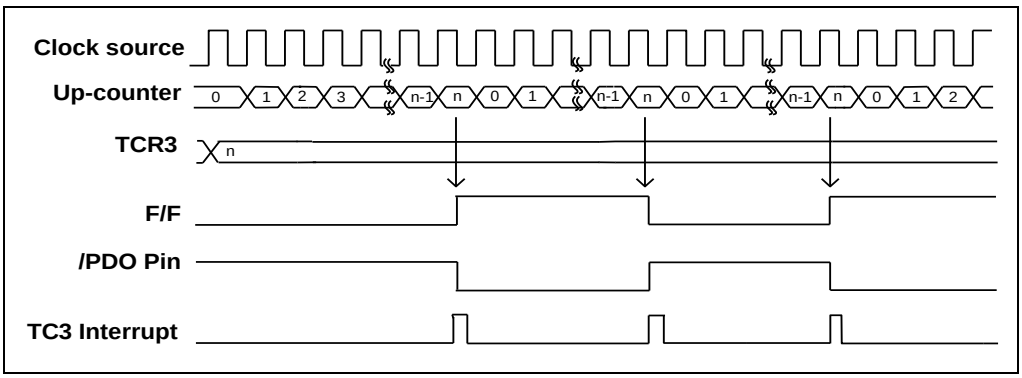


Figure 6-5 PDO Mode Timing Chart

In Pulse Width Modulation (PWM) Output Mode, counting up is performed using the internal clock. The contents of TCR3 are compared with the contents of the up-counter. The F/F is toggled when a match is found. The counter continues counting, the F/F is toggled again when the counter overflows, after which the counter is cleared. The F/F output is inverted and output to /PWM pin. A TC3 interrupt is generated each time an overflow occurs. **TCR3 is configured as a 2-stage shift register and, during output, will not switch until one output cycle is completed even if TCR3 is overwritten.** Therefore, the output can be changed continuously. Also, the first time, TCR3 is shifted by setting TC3S to "**1**" after data is loaded to TCR3.

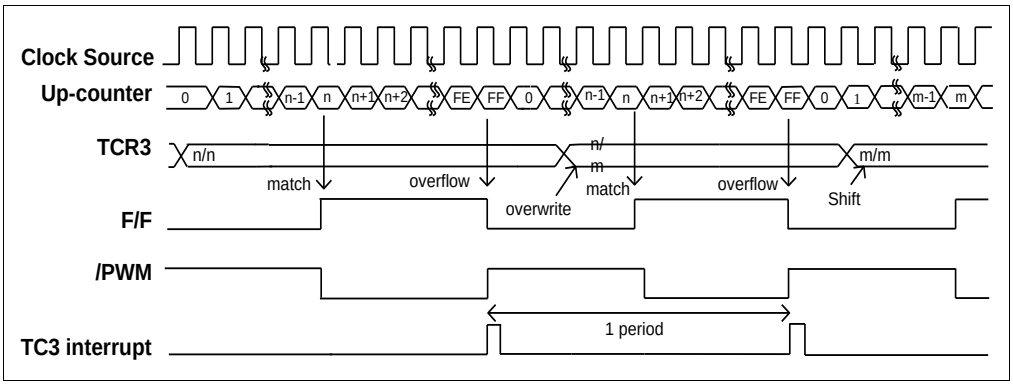


Figure 6-5 PWM Mode Timing Chart

6.1.30 Bank 3 RE TC3D (Timer 3 Data Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC3D7	TC3D6	TC3D5	TC3D4	TC3D3	TC3D2	TC3D1	TC3D0

Bits 7 ~ 0 (TC3D7 ~ TC3D0): Data Buffer of 8-bit Timer/Counter 3

6.1.31 Bank 3 RF

These are reserved registers.

6.2 Special Function Registers

6.2.1 A (Accumulator)

Internal data transfer operation, or instruction operand holding usually involves the temporary storage function of the Accumulator. The Accumulator is not an addressable register.

6.2.2 CONT (Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTE	/INT	-	-	PSTE	PST2	PST1	PST0

Bit 7 (INTE): INT signal edge

0: Interrupt occurs at a rising edge of the INT pin

1: Interrupt occurs at a falling edge of the INT pin

Bit 6 (/INT): Interrupt Enable flag

0: Masked by DISI or hardware interrupt

1: Enabled by ENI/RETI instructions

Bits 5 ~ 4: Not used, set to "**0**" at all time

Bit 3 (PSTE): Prescaler enable bit for TCC

0: Prescaler disable bit, TCC rate is 1:1

1: Prescaler enable bit, TCC rate is set at Bit 2 ~ Bit 0.

Bit 2 ~ Bit 0 (PST 2 ~ PST0): TCC prescaler bits

PST2	PST1	PST0	TCC Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

The CONT register is both readable and writable.

6.2.3 IOC5 ~ IOC6, IOC8 (I/O Port Control Register)

A value of "**1**" sets the relative I/O pin into high impedance, while "**0**" defines the relative I/O pin as output.

IOC5 ~ IOC6, IOC8 registers are both readable and writable.

6.2.4 IOC7, IOC9

Reserved registers

6.2.5 IOCA (WDT Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WDTE	EIS	-	-	PSWE	PSW2	PSW1	PSW0

Bit 7 (WDTE): Control bit used to enable the Watchdog timer

0: Disable WDT

1: Enable WDT

WDTE is both readable and writable.

Bit 6 (EIS): Control bit used to define the function of P60 (/INT) pin

0: P60, bidirectional I/O pin

1: /INT, external interrupt pin. In this case, the I/O control bit of P60 (Bit 0 of IOC6) must be set to "**1**".

When EIS is "**0**", the path of /INT is masked. When EIS is "**1**", the status of the /INT pin can also be read by way of reading Port 6 (R6).

The EIS is both readable and writable.

Bits 5 ~ 4: Not used, set to "**0**" at all time

Bit 3 (PSWE): Prescaler enable bit for WDT

0: prescaler disable bit, WDT rate is 1:1

1: prescaler enable bit, WDT rate is set at Bit 0~Bit 2

Bit 2 ~ Bit 0 (PSW2 ~ PSW0): WDT prescaler bits

PSW2	PSW1	PSW0	WDT Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

6.2.6 IOCB (Pull-down Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PD63	/PD62	/PD61	/PD60	-	-	-	/PD50

The IOCB Register is both readable and writable.

Bit 7 (/PD63): Control bit used to enable pull-down of the P63 pin.

0: Enable internal pull-down

1: Disable internal pull-down

Bit 6 (/PD62): Control bit used to enable pull-down of the P62 pin.

Bit 5 (/PD61): Control bit used to enable pull-down of the P61 pin.

Bit 4 (/PD60): Control bit used to enable pull-down of the P60 pin.

Bits 3 ~ 1: Not used, set to "**0**" at all time

Bit 0 (/PD50): Control bit used to enable pull-down of the P50 pin.

6.2.7 IOCC (Open-drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	OD65	OD64	OD63	OD62	OD61	OD60

The IOCC Register is both readable and writable.

Bits 7 ~ 6: Not used, set to "**0**" at all time

Bit 5 (OD65): Control bit used to enable open-drain output of the P65 pin

0: Disable open-drain output

1: Enable open-drain output

Bit 4 (OD64): Control bit used to enable open-drain output of the P64 pin

Bit 3 (OD63): Control bit used to enable open-drain output of the P63 pin

Bit 2 (OD62): Control bit used to enable open-drain output of the P62 pin

Bit 1 (OD61): Control bit used to enable open-drain output of the P61 pin

Bit 0 (OD60): Control bit used to enable open-drain output of the P60 pin

6.2.8 IOCD (Pull-high Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	/PH65	/PH64	/PH63	/PH62	/PH61	/PH60

The IOCD Register is both readable and writable.

Bits 7 ~ 6: Not used, set to "**0**" at all time

Bit 5 (/PH65): Control bit used to enable pull-high of the P65 pin.

0: Enable internal pull-high

1: Disable internal pull-high

Bit 4 (/PH64): Control bit used to enable pull-high of the P64 pin.

Bit 3 (/PH63): Control bit used to enable pull-high of the P63 pin.

Bit 2 (/PH62): Control bit used to enable pull-high of the P62 pin.

Bit 1 (/PH61): Control bit used to enable pull-high of the P61 pin.

Bit 0 (/PH60): Control bit used to enable pull-high of the P60 pin.

6.2.9 IOCE (Interrupt Mask Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMP2IE	-	TC3IE	-	-	-	-	-

Bit 7 (CMP2IE): CMP2IF interrupt enable bit.

0: Disable CMP2IF interrupt

1: Enable CMP2IF interrupt

When the Comparator 2 output status change is used to enter an interrupt vector or enter the next instruction. The CMP2IE bit must be set to "Enable".

Bit 6: Not used, set to "**0**" at all time

Bit 5 (TC3IE): Interrupt enable bit

0: Disable TC3IF interrupt

1: Enable TC3IF interrupt

Bits 4 ~ 0: Not used, set to "**0**" at all time

NOTE

- *User must set Bit 6 of the IOCE register to "**0**".*
- *The IOCE register is both readable and writable.*

6.2.10 IOCF (Interrupt Mask Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	ADIE	-	-	-	EXIE	ICIE	TCIE

Bit 7: Not used, set to "**0**" at all time

Bit 6 (ADIE): ADIF interrupt enable bit

0: Disable ADIF interrupt

1: Enable ADIF interrupt

When ADC complete status is used to enter an interrupt vector or enter the next instruction, the ADIE bit must be set to "Enable".

Bits 5 ~ 3: Not used, set to "0" at all time

Bit 2 (EXIE): EXIF interrupt enable bit

0: Disable EXIF interrupt

1: Enable EXIF interrupt

Bit 1 (ICIE): ICIF interrupt enable bit

0: Disable ICIF interrupt

1: Enable ICIF interrupt

Bit 0 (TCIE): TCIF interrupt enable bit

0: Disable TCIF interrupt

1: Enable TCIF interrupt

NOTE

- *User must set Bit 7 of the IOCF register to "**0**".*
- *Individual interrupt is enabled by setting its associated control bit in the IOCF to "**1**".*
- *Global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction.*
- *The IOCF register is both readable and writable.*

6.3 TCC/WDT and Prescaler

There are two 8-bit counters available as prescalers for the TCC and WDT respectively. The PST2~PST0 bits of the CONT register are used to determine the ratio of the prescaler of TCC. Likewise, the PSW2~PSW0 bits of the IOCA register are used to determine the WDT prescaler. The prescaler counter will be cleared by the instructions each time they are written into TCC. The WDT and prescaler will be cleared by the "WDTC" and "SLEP" instructions. Figure 6.7 below; depicts the EM78Fx61N circuit diagram of TCC/WDT.

R1 (TCC) is an 8-bit timer. The TCC clock source can be an internal clock only. The TCC signal source is from an internal clock, TCC will be incremented by 1 at Fc clock (without prescaler). **The TCC will stop running when sleep mode occurs**.

The watchdog timer is a free running on-chip RC oscillator. The WDT will keep on running even after the oscillator driver has been turned off (i.e. in sleep mode). During normal operation or sleep mode, a WDT time-out (if enabled) will cause the device to reset. The WDT can be enabled or disabled any time during normal mode by software programming. Refer to the WDTE bit of the IOCA register. With no prescaler, the WDT time-out period is approximately 18 ms[1] (one oscillator start-up timer period).

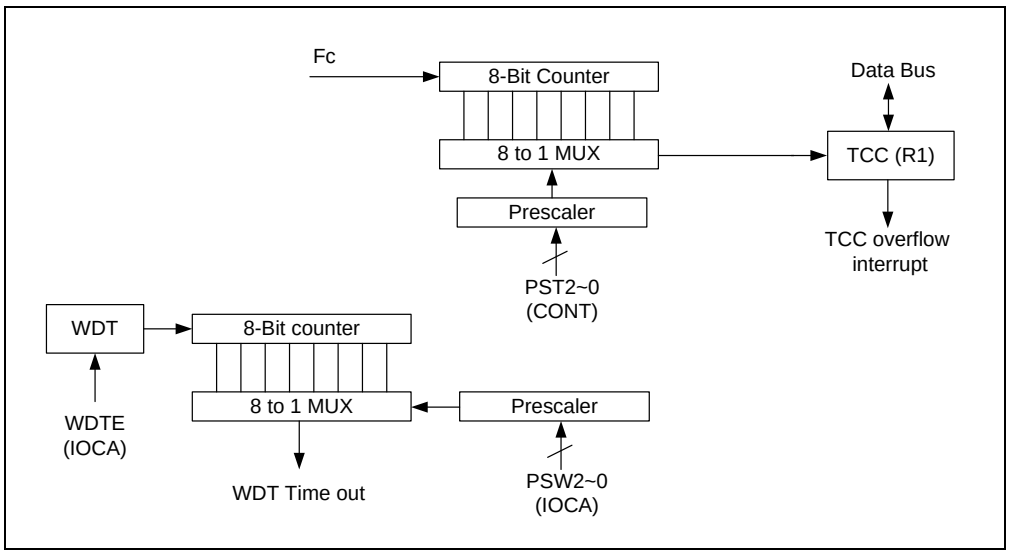


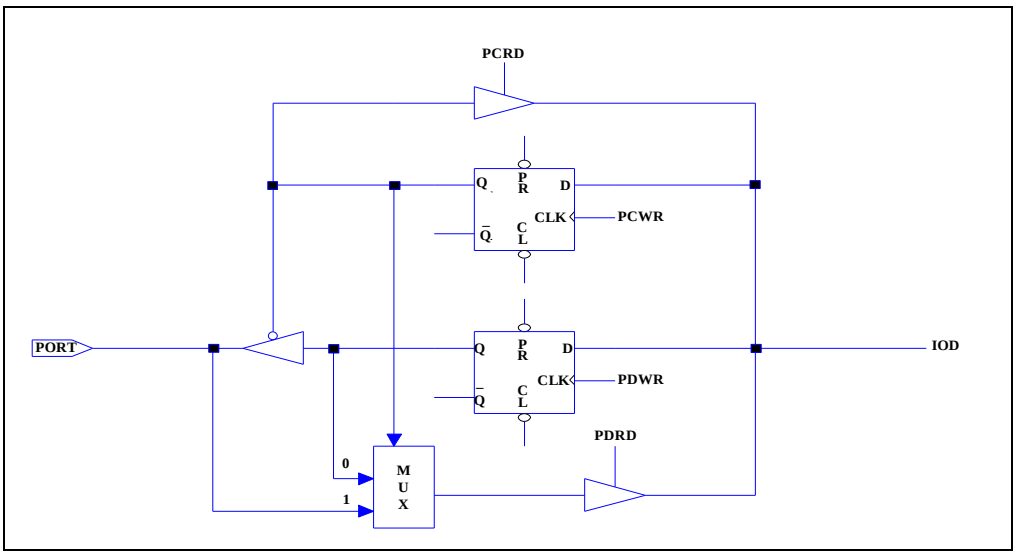
Figure 6.7 TCC and WDT Block Diagram

6.4 I/O Ports

The I/O registers, Ports 5, 6 and 8, are bidirectional tri-state I/O ports. Port 6 can be pulled-high internally by software. In addition, Port 6 can also have open-drain output by software. Input status change interrupt (or wake-up) function on Port 6, P50, P60 ~ P63 pins can be pulled down by software. Each I/O pin can be defined as "input" or "output" pin by the I/O control register (IOC5 ~ IOC6, IOC8).

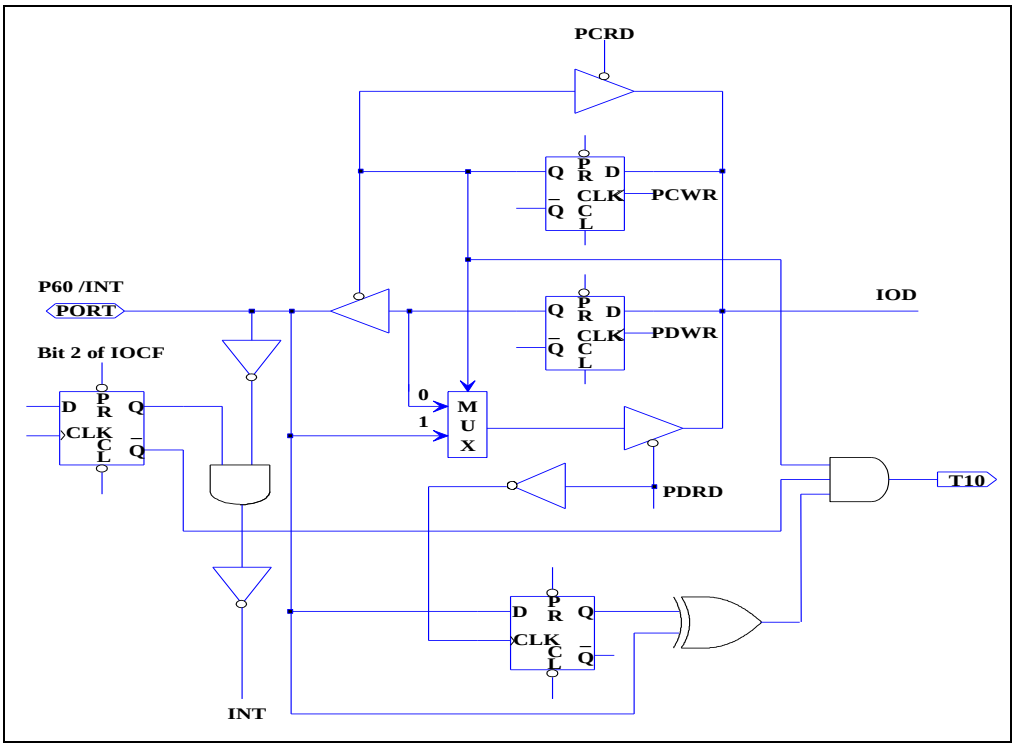
The I/O registers and I/O control registers are both readable and writable. The I/O interface circuits for Ports 5 ~ 6 and Port 8 are shown in the following Figures 6-8, 6-9(a), 6-9(b), and Figure 6-10.

[1] *VDD=5V, WDT time-out period = 16ms ± 7.5%*
VDD=3V, WDT time-out period = 18ms ± 7.5%



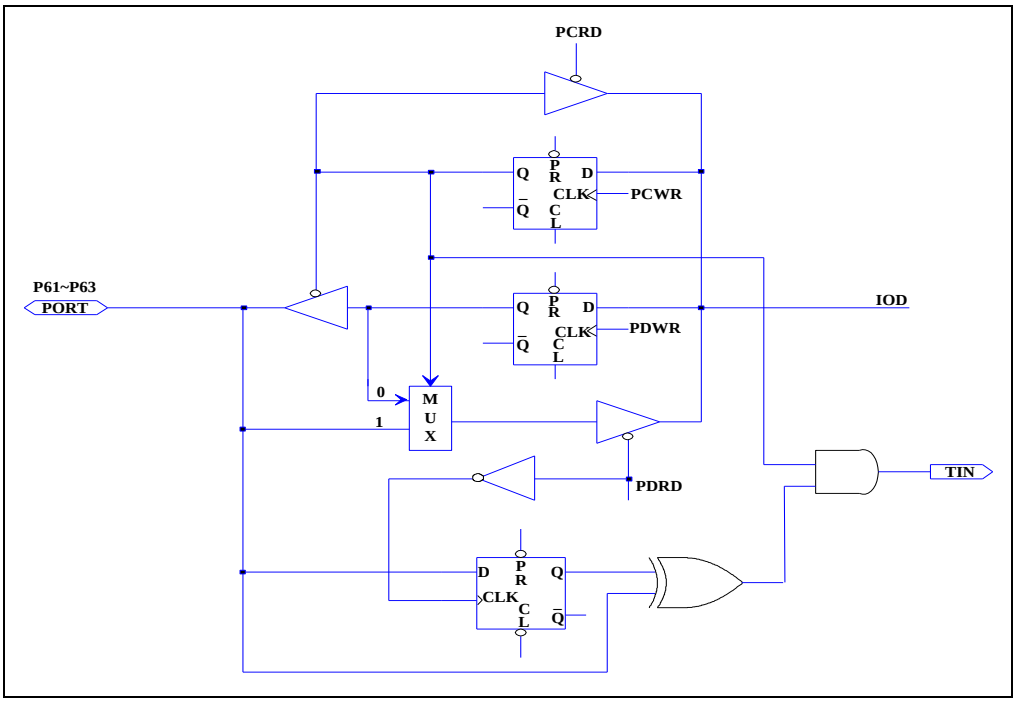
NOTE: *Pull-down is not shown in the figure.*

Figure 6-8 I/O Port and I/O Control Register Circuit for Ports 5 ~ 6, Port 8



NOTE: *Pull-high (down) and Open-drain are not shown in the figure.*

Figure 6-8(a) I/O Port and I/O Control Register Circuit for P60 (/INT)



Note: *Pull-high (down) and Open-drain are not shown in the figure.*

Figure 6-8(b) I/O Port and I/O Control Register Circuit for P61~P65

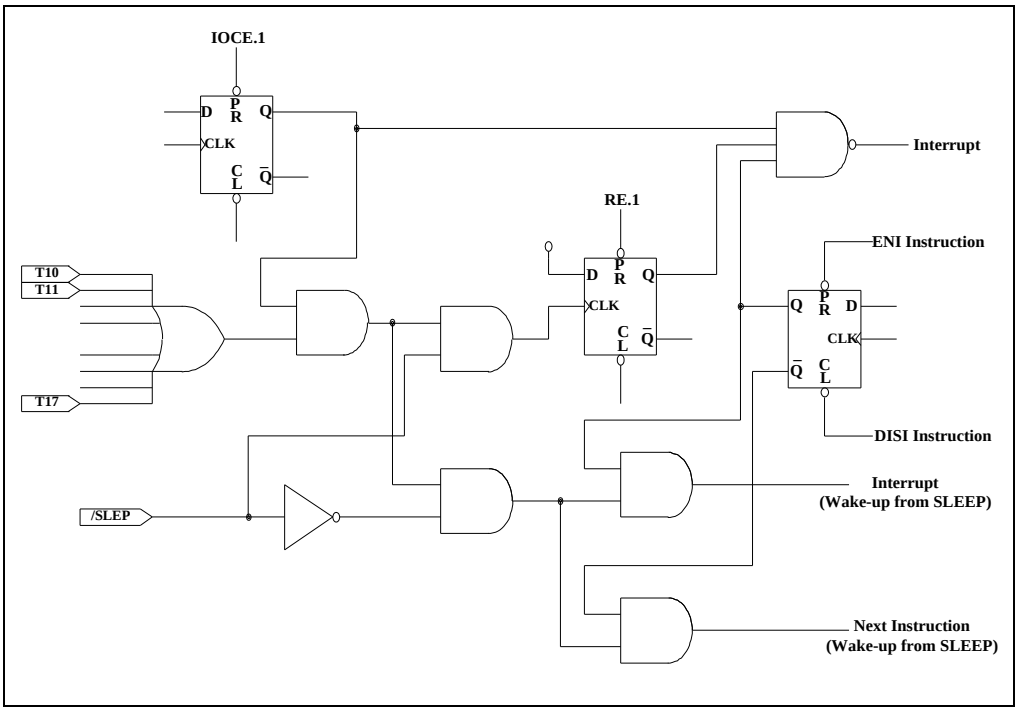


Figure 6-9 Block Diagram of I/O Port 6 with Input Change Interrupt/Wake-up

6.4.1 Usage of Port 6 Input Change Wake-up/Interrupt Function

Usage of Port 6 Input Status Changed Wake-up/Interrupt	
(I) Wake-up from Port 6 Input Status Change **a) Before Sleep** 1. Disable WDT[2] (use this very carefully) 2. Read I/O Port 6 (MOV R6,R6) 3a. Enable interrupt (Set IOCF.1), after wake-up if “ENI” switch to interrupt Vector (006H), if “DISI” excute next instruction 3b. Disable interrupt (Set IOCF.1), always execute next instruction 4. Enable wake-up enable bit (Set RA.6) 5. Execute "SLEP" instruction **b) After Wake-up** 1. IF "ENI" → Interrupt Vector (006H) 2. IF "DISI" → Next instruction	(II) Port 6 Input Status Change Interrupt 1. Read I/O Port 6 (MOV R6,R6) 2. Execute "ENI" 3. Enable interrupt (Set IOCF.1) 4. IF Port 6 change (interrupt) → Interrupt Vector (006H)

6.5 Reset and Wake-up

6.5.1 Reset

A reset is initiated by one of the following events**:**

1) Power-on reset
2) /RESET pin input "low"
3) WDT time-out (if enabled)

The device is kept in a reset condition for a period of approximately 18ms[3] (one oscillator start-up timer period) after a reset is detected.

- The oscillator is running, or will be started.
- The Program Counter (R2) is set to all "**0**".
- All I/O port pins are configured as input mode (high-impedance state).
- The Watchdog timer and prescaler are cleared.
- When power is switched on, the upper three bits of R3 are cleared.
- The bits of the RB, RC, RD registers are set to their previous status.

[2] *The Software disables the WDT (Watchdog Timer) but the hardware must be enabled before applying Port 6 Change wake-up function. (Code Option Register and Bit 6 (ENWDTB) are set to “**1**”).*

[3] *Vdd = 5V, set up time period = 16ms ± 7.5%*
Vdd = 3V, set up time period = 18ms ± 7.5%

- The bits of the CONT register are set to all "**0**".
- The bits of the IOCA register are set to all "**0**".
- The bits of the IOCB register are set to all "**1**".
- The bits of the IOCC register are set to all "**0**".
- The bits of the IOCD register are set to all "**1**".
- The bits of the IOCE register are set to all "**0**".
- The bits of the IOCF register are set to all "**0**".

Sleep (power down) mode is asserted by executing the “SLEP” instruction. While entering Sleep mode, the WDT (if enabled) is cleared but keeps on running. After a wake-up, the wake-up time is 10µs for RC mode and is 800 µs for High Crystal mode.

The controller can be awakened by**:**

1) External reset input on /RESET pin
2) WDT time-out (if enabled)
3) Port 6 input status changes (if enabled)
4) Comparator output status changed (if CMPWE is enabled).
5) A/D conversion completed (if ADWE is enabled).
6) External (P60, /INT) pin changes (if EXWE is enabled).

The first two cases (Case 1 and Case 2) will cause the EM78Fx61N to reset. The T and P flags of R3 can be used to determine the source of the reset (wake-up). Cases 3, 4, 5, 6 are considered the continuation of program execution and the global interrupt ("ENI" or "DISI" being executed) determines whether or not the controller branches to the interrupt vector following a wake-up. If ENI is executed before SLEP, the instruction will begin to execute from the Address 0×6, 0×15, 0×30, 0×3 after wake-up. If DISI is executed before SLEP, the execution will restart from the instruction right next to SLEP after wake-up. After a wake-up, the RC mode wake-up time is 10µs and the High Crystal mode wake-up time is 800µs.

One or more of Cases 2 to 6 can be enabled before entering into Sleep mode. That is-

a) If WDT is enabled before SLEP, all of the RE bit is disabled. Hence, the EM78Fx61N can be awakened only by Case 1 or 2. Refer to section on Interrupt (Section 6.6) for further details.

b) If Port 6 Input Status Change is used to wake-up EM78Fx61N and ICWE bit of RA register is enabled before SLEP, the WDT must be disabled. Hence, the EM78Fx61N can wake-up only by Case 3.

c) If Comparator 2 output status change is used to wake-up EM78Fx61N and CMPWE bit of RA register is enabled before SLEP, WDT must be disabled by software. Hence, the EM78Fx61N can wake-up only by Case 4.

d) If AD conversion completed is used to wake-up EM78Fx61N and ADWE bit of RA register is enabled before SLEP, the WDT must be disabled by software. Hence, the EM78Fx61N can wake-up only by Case 5.

e) If External (P60,/INT) pin change is used to wake-up EM78Fx61N and EXWE bit of RA register is enabled before SLEP, the WDT must be disabled. Hence, the EM78Fx61N can wake-up only by Case 6.

If Port 6 Input Status Change Interrupt is used to wake-up the EM78Fx61N, (as in Case [b] above), the following instructions must be executed before SLEP**:**

```
MOV             A, @0xxx1000b  ; Select WDT prescaler and
                               ; Disable the WDT
IOW             IOCA
WDTC                           ; Clear WDT and prescaler
MOV             R6, R6         ; Read Port 6
ENI (or DISI)                  ; Enable (or disable) global
                               ; interrupt
BC              R4, 7          ; Select Bank0
BC              R4, 6
MOV             A, @0100xxxxb  ; Enable Port 6 input change
                               ; wake-up bit
MOV             RA,A
MOV             A, @xxxxxx1xb  ; Enable Port 6 input change
                               ; interrupt
IOW             IOCF
SLEP                           ; Sleep
```

Similarly, if the Comparator 2 Interrupt is used to wake up the EM78Fx61N (as in Case [c] above), the following instructions must be executed before SLEP:

```
BS              R4, 7          ; Select Bank 3
BS              R4, 6
MOV             A, @xxxx10xxb  ; Select a comparator and P80 act
                               ; as CO pin
MOV             R7,A
MOV             A, @0xxx1000b  ; Select WDT prescaler and
                               ; Disable the WDT
IOW             IOCA
WDTC                           ; Clear WDT and prescaler
ENI (or DISI)                  ; Enable (or disable) global
                               ; interrupt
BC              R4, 7          ; Select Bank 0
BC              R4, 6
MOV             A, @1000xxxxb  ; Enable comparator output status
                               ; change wake-up bit
MOV             RA,A
MOV             A, @10000000b  ; Enable comparator output status
                               ; change interrupt
IOW             IOCE
SLEP                           ; Sleep
```

6.5.2 Summary of Wake-up and Interrupt Modes Operation

Wake-up Signal	Condition Signal	Sleep Mode		Idle Mode		Green Mode		Normal Mode	
		DISI	ENI	DISI	ENI	DISI	ENI	DISI	ENI
External INT	EXWE = 0, EXIE = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	EXWE = 0, EXIE = 1	Wake-up is invalid		Wake-up is invalid		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	EXWE = 1, EXIE = 0	Wake up + Next Instruction		Wake up + Next Instruction		Interrupt is invalid.		Interrupt is invalid	
	EXWE = 1, EXIE = 1	Wake up + Next Instruction	Wake up + Interrupt Vector	Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
Port 6 pin change	ICWE = 0, ICIE = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	ICWE = 0, ICIE = 1	Wake-up is invalid		Wake-up is invalid		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	ICWE = 1, ICIE = 0	Wake up + Next Instruction		Wake up + Next Instruction		Interrupt is invalid		Interrupt is invalid	
	ICWE = 1, ICIE = 1	Wake up + Next Instruction	Wake up + Interrupt Vector	Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
TCC overflow	TCIE = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	TCIE = 1	Wake-up is invalid		Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
Comparator 2 (Comparator Output Status Change)	CMP2WE = 0, CMP2IE = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	CMP2WE = 0, CMP2IE = 1	Wake-up is invalid		Wake-up is invalid		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	CMP2WE = 1, CMP2IE = 0	Wake up + Next Instruction		Wake up + Next Instruction		Interrupt is invalid		Interrupt is invalid	
	CMP2WE = 1, CMP2IE = 1	Wake up + Next Instruction	Wake up + Interrupt Vector	Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector

(Continuation)

Wake-up Signal	Condition Signal	Sleep Mode		Idle Mode		Green Mode		Normal Mode	
		DISI	ENI	DISI	ENI	DISI	ENI	DISI	ENI
TC3 interrupt	TC3IE = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	TC3IE = 1	Wake-up is invalid		Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
AD Conversion Complete Interrupt	ADWE = 0, ADIE = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	ADWE = 0, ADIE = 1	Wake-up is invalid		Wake-up is invalid		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	ADWE = 1, ADIE = 0	Wake up + Next Instruction		Wake up + Next Instruction		Interrupt is invalid		Interrupt is invalid	
	ADWE = 1, ADIE = 1	Wake up + Next Instruction	Wake up + Interrupt Vector	Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector

6.5.3 Summary of Registers Initialized Values

Legend: **x:** *Not used* **P:** *Previous value before reset*
u: *Unknown or don't care* **t:** *Refer to the tables under Section 6.5.4*

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N/A	IOC5	Bit Name	C57	-	C55	C54	-	-	-	C50
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC6	Bit Name	-	-	C65	C64	C63	C62	C61	C60
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC8	Bit Name	-	-	-	-	C83	C82	C81	C80
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	CONT	Bit Name	INTE	INT	-	-	PSTE	PST2	PST1	PST0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

(Continuation)

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0×00	R0 (IAR)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×01	R1 (TCC)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×02	R2 (PC)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	Jump to interrupt vector address or continue to execute next instruction							
0×03	R3 (SR)	Bit Name	-	-	-	T	P	Z	DC	C
		Power-on	0	0	0	1	1	U	U	U
		/RESET and WDT	0	0	0	t	t	P	P	P
		Wake-up from Pin Change	P	P	P	t	t	P	P	P
0×04	R4 (RSR)	Bit Name	Bank 1	Bank 0	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×05	P5 (Bank 0)	Bit Name	P57	-	P55	P54	-	-	-	P50
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×06	P6 (Bank 0)	Bit Name	-	-	P65	P64	P63	P62	P61	P60
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×08	P8 (Bank 0)	Bit Name	-	-	-	-	P83	P82	P81	P80
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

(Continuation)

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0×09	R9 (Bank 0)	Bit Name	RBit7	RBit6	RBit5	RBit4	RBit3	RBit2	RBit1	RBit0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0A	RA (Bank 0)	Bit Name	CMP2WE	ICWE	ADWE	EXWE	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0B	RB (ECR) (Bank 0)	Bit Name	RD	WR	EEWE	EEDF	EEPC	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0C	RC (Bank 0)	Bit Name	-	EE_A6	EE_A5	EE_A4	EE_A3	EE_A2	EE_A1	EE_A0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0D	RD (Bank 0)	Bit Name	EE_D7	EE_D6	EE_D5	EE_D4	EE_D3	EE_D2	EE_D1	EE_D0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0E	RE (Bank 0)	Bit Name	-	TIMERSC	CPUS	IDLE	-	-	-	-
		Power-on	0	1	1	1	0	0	0	0
		/RESET & WDT	0	1	1	1	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0F	RF (ISR) (Bank 0)	Bit Name	-	ADIF	-	-	-	EXIF	ICIF	TCIF
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×08	R8 (Bank 1)	Bit Name	RCM1	RCM0	-	-	-	-	-	-
		Power-on	Word 1<3,2>		0	0	0	0	0	0
		/RESET & WDT	Word 1<3,2>		0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

(Continuation)

Addr	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0×0F	RF (Bank 1)	Bit Name	CMP2IF	-	TC3IF	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×05	R5 (Bank 2)	Bit Name	-	-	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×06	R6 (Bank 2)	Bit Name	VREFS	CKR1	CKR0	ADRUN	ADPD	ADIS2	ADIS1	ADIS0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×08	R8 (Bank 2)	Bit Name	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×09	R9 (Bank 2)	Bit Name	-	-	-	-	-	-	AD1	AD0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×06	R6 (Bank 3)	Bit Name	MLB	-	-	-	-	-	RBit9	RBit8
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×07	R7 (Bank 3)	Bit Name	-	-	-	CPOUT2	COS21	COS20	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0D	RD (Bank 3)	Bit Name	TC3FF1	TC3FF0	TC3S	TC3CK2	TC3CK1	TC3CK0	TC3M1	TC3M0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

(Continuation)

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0×0E	RE (Bank 3)	Bit Name	TCR3 D7	TCR3D6	TCR3D5	TCR3D4	TCR3D3	TCR3D2	TCR3D1	TCR3D0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0A	IOCA	Bit Name	WDTE	EIS	-	-	PSWE	PSW2	PSW1	PSW0
		Power-un	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0B	IOCB	Bit Name	/PD63	/PD62	/PD61	/PD60	-	-	-	/PD50
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0C	IOCC	Bit Name	-	-	OD65	OD64	OD63	OD62	OD61	OD60
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0D	IOCD	Bit Name	-	-	/PH65	/PH64	/PH63	/PH62	/PH61	/PH60
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0E	IOCE	Bit Name	CMP2IE	-	TC3IE	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0F	IOCF	Bit Name	-	ADIE	-	-	-	EXIE	ICIE	TCIE
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×10 ~ 0×3F	R10~R 3F	Bit Name	-	-	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

6.5.4 Status of T and P of the Status Register

A reset condition is initiated by following events:

1) Power-on condition

2) High-low-high pulse on /RESET pin

3) Watchdog timer time-out

The values of **T** and **P** in the following tables are used to check how the processor wakes up and shows the events that may affect the status of **T** and **P** respectively.

■ **Values of T and P after Reset**

Reset Type	T	P
Power on	1	1
/RESET during operation mode	*P	*P
/RESET wake-up during Sleep mode	1	0
WDT during operation mode	0	*P
WDT wake-up during Sleep mode	0	0
Wake-up on pin change during Sleep mode	1	0

* ***P:*** *Previous status before reset*

■ **Status of T and P Being Affected by Events**

Event	T	P
Power on	1	1
WDTC instruction	1	1
WDT time-out	0	*P
SLEP instruction	1	0
Wake-up on pin change during Sleep mode	1	0

* ***P:*** *Previous status before reset*

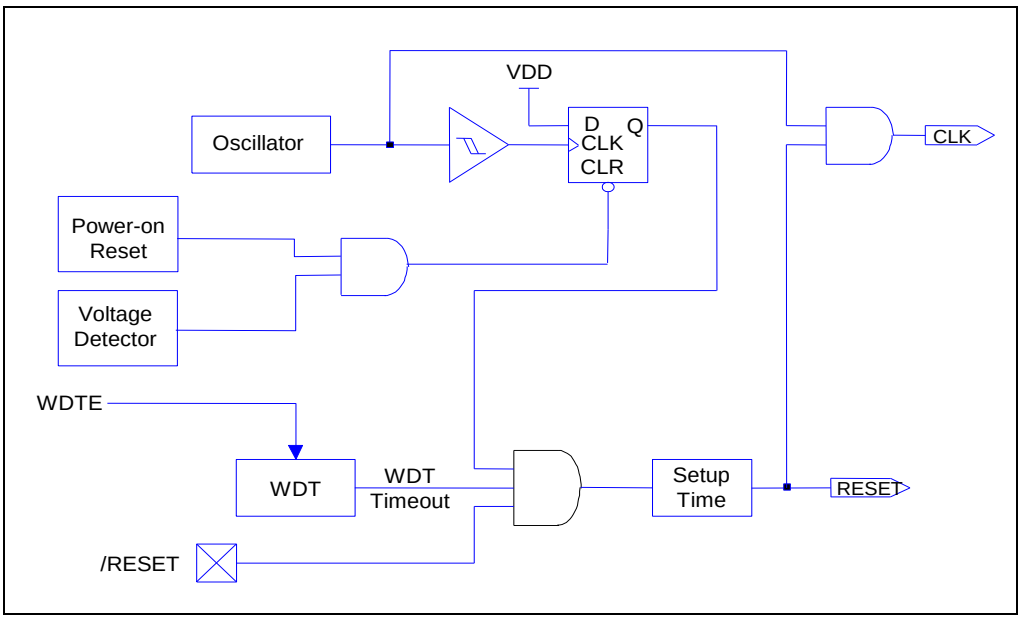


Figure 6-11 Block Controller Reset Diagram

6.6 Interrupt

The EM78Fx61N has 6 interrupts (3 external, 3 internal) as listed below**:**

Interrupt Source		Enable Condition	Int. Flag	Int. Vector	Priority
Internal / External	Reset	-	-	0000	High 0
External	INT	ENI + EXIE=1	EXIF	0003	1
External	Port 6 pin change	ENI +ICIE=1	ICIF	0006	2
Internal	TCC	ENI + TCIE=1	TCIF	0009	3
External	Comparator 2	ENI+CMP2IE=1	CMP2IF	0015	4
Internal	TC3	ENI + TC3IE=1	TC3IF	0027	5
Internal	AD	ENI+ADIE=1	ADIF	0030	6

RE and RF are the interrupt status registers that record the interrupt requests in the relative flags/bits. IOCE and IOCF are the interrupt mask registers. The global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. When one of the enabled interrupts occurs, the next instruction will be fetched from their individual address. The interrupt flag bit must be cleared by instructions before leaving the interrupt service routine and before interrupts are enabled to avoid recursive interrupts.

The flag (except ICIF bit) in the Interrupt Status Register (RF and RE) is set regardless of the status of its mask bit or the execution of ENI. The RETI instruction ends the interrupt routine and enables the global interrupt (the execution of ENI).

The external interrupt has an on-chip digital noise rejection circuit (input pulse less than **8 system clock time** is eliminated as noise), **but in Low Crystal oscillator (LXT) mode, the noise rejection circuit will be disabled**. When an interrupt (Falling edge) is generated by the External interrupt (when enabled), the next instruction will be fetched from Address 003H.

Before the interrupt subroutine is executed, the contents of ACC and the R3 and R4 register are saved by hardware. If another interrupt occurred, the ACC, R3 and R4 will be replaced by the new interrupt. After the interrupt service routine is completed, ACC,R3 and R4 are pushed back.

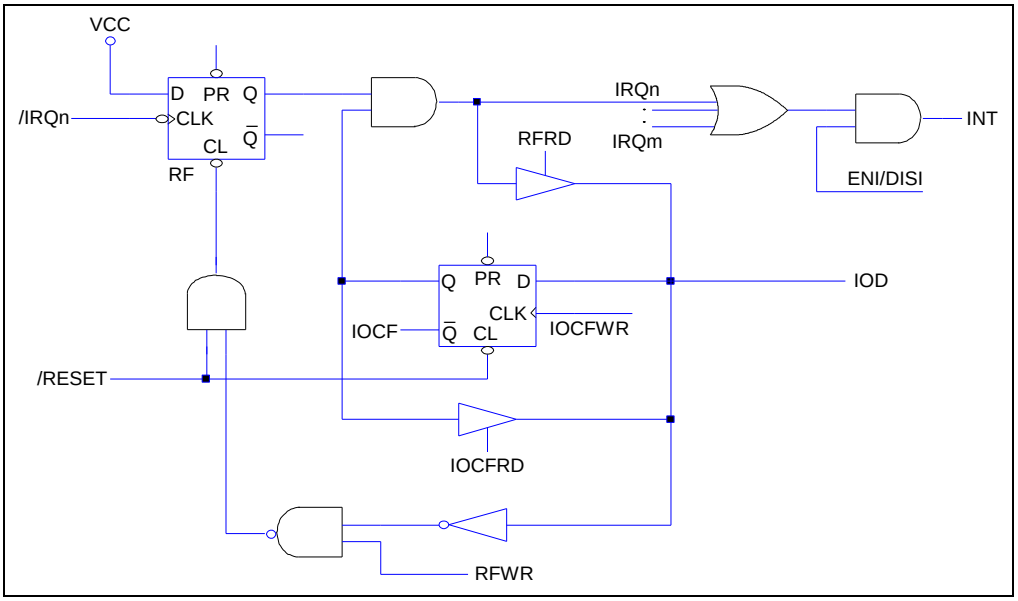


Figure 6-12 Interrupt Input Circuit

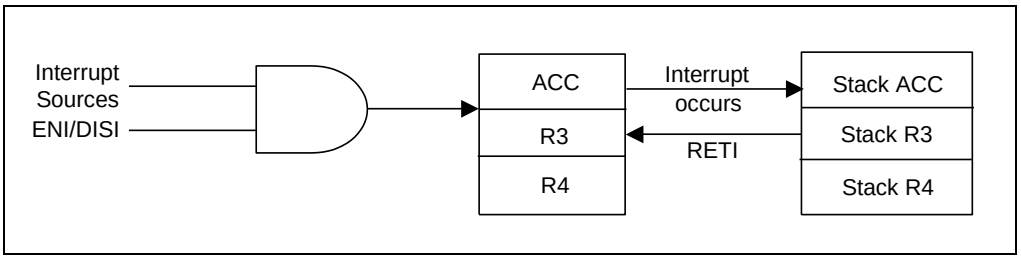


Figure 6-13 Interrupt Back-up Diagram

6.7 Data EEPROM (applicable to EM78F661N only)

The Data EEPROM is readable and writable during normal operation over the whole Vdd range. The operation for Data EEPROM is based on a single byte. A write operation makes an erase-then-write cycle to take place on the allocated byte.

The Data EEPROM memory provides high erase and write cycles. A byte write automatically erases the location and writes the new value.

6.7.1 Data EEPROM Control Register

6.7.1.1 RB (EEPROM Control Register)

The EECR (EEPROM Control Register) is the control register for configuring and initiating the control register status.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RD	WR	EEWE	EEDF	EEPC	-	-	-

Bit 7 (RD): Read control register

0: Does not execute EEPROM read

1: Read EEPROM content (RD can be set by software and is cleared by hardware after Read instruction is completed).

Bit 6 (WR): Write control register

0: Write cycle to the EEPROM is completed

1: Initiate a write cycle (WR can be set by software. WR is cleared by hardware after Write cycle is completed).

Bit 5 (EEPROM): Write Enable bit

0: Forbids write to the EEPROM

1: Allows EEPROM write cycles

Bit 4 (EEDF): EEPROM Detect Flag

0: Write cycle is completed.

1: Write cycle is unfinished.

Bit 3 (EEPC): EEPROM power-down control bit

0: Switch off the EEPROM

1: EEPROM is operating

Bits 2 ~ 0: Not used, set to "**0**" at all time

6.7.1.2 RC (128 Bytes EEPROM Address)

When accessing the EEPROM data memory, the RC (128 bytes EEPROM address register) holds the address to be accessed. In accordance with the operation, the RD (128 bytes EEPROM Data register) holds the data to be written, or the data read, at the address in RC.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	EE_A6	EE_A5	EE_A4	EE_A3	EE_A2	EE_A1	EE_A0

Bit 7: Not used, set to "**0**" at all time

Bits 6 ~ 0: 128 bytes EEPROM address

6.7.1.3 RD (128 Bytes EEPROM Data)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EE_D7	EE_D6	EE_D5	EE_D4	EE_D3	EE_D2	EE_D1	EE_D0

Bits 7 ~ 0: 128 bytes EEPROM data

6.7.2 Programming Steps / Example Demonstration

■ **Programming Steps**

Follow these steps to write or read data from the EEPROM:

1) Set the RB.EEPC bit to "**1**" to enable the EEPROM power.
2) Write the address to RC (128 bytes EEPROM address).
   a) Set the RB.EEWE bit to "**1**", if the write function is employed.
   b) Write the 8-bit data value to be programmed in the RD (128 bytes EEPROM data)
   c) Set the RB.WR bit to "**1**", then execute write function
   d) Set the RB.READ bit to "**1**", after which, execute read function
3) a) Wait for the RB.WR to be cleared
   b) Wait for the RB.EEDF to be cleared
4) For the next conversion, repeat from Step 2 as required.
5) If you want to save power, make sure the EEPROM data is switched off by clearing the RB.EEPC.

■ **Example Demonstration Programs**

```
;Define the control register
;Write data to EEPROM
RC == 0x0C
RB == 0x0B
RD == 0x0D
Read == 0x07
WR == 0x06
EEWE == 0x05
EEDF == 0x04
EEPC == 0x03

BS  RB, EEPC   ; Set the EEPROM power on
MOV A,@0x0A
MOV RC,A       ; Assign the address from EEPROM
BS  RB, EEWE   ; Enable the EEPROM write function
MOV A,@0x55
MOV RD,A       ; Set the data for EEPROM
BS  RB,WR      ; Write value to EEPROM
JBC RB,EEDF    ; Check whether the EEPROM bit is complete or not
JMP $-1
```

6.8 Analog-to-Digital Converter (ADC)

The analog-to-digital circuitry consists of a 10-bit analog multiplexer, two control registers [AISR/R5 (Bank 2), ADCON/R6 (Bank 2), two data registers (ADDH, ADDL/R8, R9), and an ADC with 10-bit resolution. The functional block diagram of the ADC is shown in Figure 6-14 below. The analog reference voltage (Vref) and analog ground are connected via separate input pins.

The ADC module utilizes successive approximation to convert the unknown analog signal into a digital value. The result is fed to the ADDH and ADDL. Input channels are selected by the analog input multiplexer via the ADCON register Bits ADIS2 ~ ADIS0.

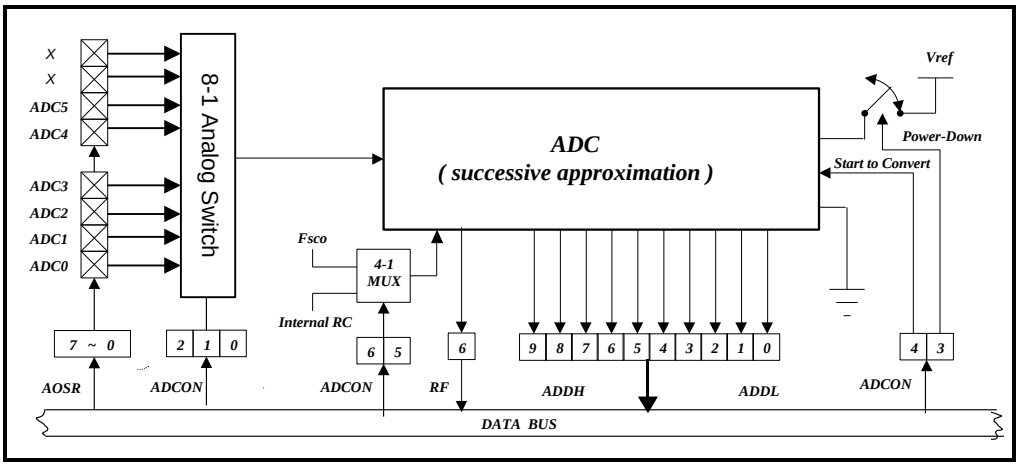


Figure 6-14 Functional Block Diagram of Analog-to-Digital Conversion

6.8.1 ADC Control Register (AISR/R5, ADCON/R6)

6.8.1.1 Bank 2 R5 AISR (ADC Input Select Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0
0	0	0	0	0	0	0	0

The AISR register individually defines the Port 6 pins as analog input or as digital I/O.

Bits 7 ~ 6: Not used, set to "**0**" at all time

Bit 5 (ADE5): AD converter enable bit of P65 pin

0: Disable ADC5, P65 functions as I/O pin

1: Enable ADC5 to function as analog input pin

Bit 4 (ADE4): AD converter enable bit of P64 pin

0: Disable ADC4, P64 functions as I/O pin

1: Enable ADC4 to function as analog input pin

Bit 3 (ADE3): AD converter enable bit of P63 pin

0: Disable ADC3, P63 functions as I/O pin

1: Enable ADC3 to function as analog input pin

Bit 2 (ADE2): AD converter enable bit of P62 pin

0: Disable ADC2, P62 functions as I/O pin

1: Enable ADC2 to function as analog input pin

Bit 1 (ADE1): AD converter enable bit of P61 pin

0: Disable ADC1, P61 functions as I/O pin

1: Enable ADC1 to function as analog input pin

Bit 0 (ADE0): AD converter enable bit of P60 pin

0: Disable ADC0, P60 functions as I/O pin

1: Enable ADC0 to function as analog input pin

6.8.1.2 Bank 2 R6 ADCON (A/D Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VREFS	CKR1	CKR0	ADRUN	ADPD	ADIS2	ADIS1	ADIS0

The ADCON register controls the operation of the A/D conversion and determines which pin should be currently active.

Bit 7 (VREFS): ADC's Vref input source

0: ADC's Vref is connected to Vdd (default value), and the P50/VREF pin carries out the function of P50

1: ADC's Vref is connected to P50/VREF

Bit 6 ~ Bit 5 (CKR1 ~ CKR0): The prescaler of oscillator clock rate of ADC

00 = 1**:** 4 (default value)

01 = 1**:** 16

10 = 1**:** 1

11 = 1**:** 2

CKR1/CKR0	EM78F561N/F661N		UIT660N	
	Operation Mode	Max. Operation Frequency	Operation Mode	Max. Operation Frequency
00	$F_{OSC}/4$	4 MHz	$F_{OSC}/4$	4 MHz
01	$F_{OSC}/16$	16 MHz	F_{OSC}	1 MHz
10	F_{OSC}	1 MHz	$F_{OSC}/16$	16 MHz
11	$F_{OSC}/2$	2 MHz	$F_{OSC}/2$	2 MHz

Bit 4 (ADRUN): ADC starts to run

0: Reset on completion of the conversion. This bit cannot be reset by software.

1: A/D conversion is started. This bit can be set by software.

Bit 3 (ADPD): ADC Power-down mode

0: Switch off the resistor reference to save power even while the CPU is operating

1: ADC is operating

Bit 2 ~ Bit 0 (ADIS2 ~ ADIS0): Analog Input Select

000 = AN0/P60

001 = AN1/P61

010 = AN2/P62

011 = AN3/P63

100 = AN4/P64

101 = AN5/P65

110 = X

111 = X

These can only be changed when the ADIF bit and the ADRUN bit are both Low.

6.8.2 ADC Data Buffer (ADDH, ADDL/R8, R9)

When the A/D conversion is completed, the result is loaded to the ADDH, ADDL. The ADRUN bit is cleared, and the ADIF is set.

6.8.3 A/D Sampling Time

The accuracy, linearity, and speed of the successive approximation A/D converter are dependent on the properties of the ADC and the comparator. The source impedance and the internal sampling impedance directly affect the time required to charge the sample holding capacitor. The application program controls the length of the sample time to meet the specified accuracy. Generally speaking, the program should wait for 2μs for each KΩ of the analog source impedance and at least 2μs for the low-impedance source. The maximum recommended impedance for analog source is 10KΩ at Vdd=5V. After the analog input channel is selected, this acquisition time must be done before the conversion can be started.

6.8.4 A/D Conversion Time

CKR1 and CKR0 select the conversion time (Tct), in terms of instruction cycles. This allows the MCU to run at a maximum frequency without sacrificing the AD conversion accuracy. For EM78Fx61N, the conversion time per bit is 1μs. The following table shows the relationship between Tct and the maximum operating frequencies.

EM78F561N/F661N				
CKR1: CKR0	**Operation Mode**	**Max. Operation Frequency**	**Max. Conversion Rate/Bit**	**Max. Conversion Rate**
00	Fosc/4	4 MHz	1 MHz (1 μs)	16×1 μs = 16 μs (62.5kHz)
01	Fosc/16	16 MHz	1 MHz (1 μs)	16×1 μs = 16 μs (62.5kHz)
10	Fosc	1 MHz	1 MHz (1 μs)	16×1 μs = 16 μs (62.5kHz)
11	Fosc/2	2 MHz	1 MHz (1 μs)	16×1 μs = 16 μs (62.5kHz)

UIT660				
CKR1: CKR0	**Operation Mode**	**Max. Operation Frequency**	**Max. Conversion Rate/Bit**	**Max. Conversion Rate**
00	Fosc/4	4 MHz	1 MHz (1 μs)	16×1 μs = 16 μs (62.5kHz)
01	Fosc	1 MHz	1 MHz (1 μs)	16×1 μs = 16 μs (62.5kHz)
10	Fosc/16	16 MHz	1 MHz (1 μs)	16×1 μs = 16 μs (62.5kHz)
11	Fosc/2	2 MHz	1 MHz (1 μs)	16×1 μs = 16 μs (62.5kHz)

NOTE

- *The pin that is not used as analog input can be used as regular input or output pin.*
- *During conversion, do not perform output instruction to maintain precision for all the pins.*
- The operation mode setting is different between EM78F561N/F661N and UIT660N.

6.8.5 A/D Operation during Sleep Mode

In order to obtain a more accurate ADC value and reduced power consumption, the A/D conversion remains operational during Sleep mode. **As the SLEP instruction is executed, all MCU operations will stop except for the Oscillator, TCC, TC3, and A/D conversion.**

The AD Conversion is considered completed when**:**

1 ADRUN bit of R6 register is cleared to "**0**".

2 Wake-up from A/D conversion remains in operation during Sleep Mode.

The result is fed to the ADDATA, ADOC when the conversion is completed. If the ADWE is enabled, the device will wake up. Otherwise, the A/D conversion will be shut off, no matter what the status of the ADPD bit is.

6.8.6 Programming Steps/Considerations

■ **Programming Steps**

Follow the following steps to obtain data from the ADC**:**

1. Write to the four bits (ADE5~ADE0) on the R5 (AISR) register to define the characteristics of R6 (digital I/O, analog channels, or voltage reference pin)
2. Write to the R6/ADCON register to configure the AD module:
   a) Select AD input channel (ADIS2 **:** ADIS0)
   b) Define the AD conversion clock rate (CKR1 ~ CKR0)
   c) Select the VREFS input source of the ADC
   d) Set the ADPD bit to "**1**" to begin sampling
3. Set the ADWE bit if the wake-up function is employed.
4. Set the ADIE bit if the interrupt function is employed.
5. Write "ENI" instruction if the interrupt function is employed.
6. Set the ADRUN bit to "**1**"
7. Wait for wake-up or for ADRUN bit to be cleared to "**0**"
8. Read the ADDATAH and ADDATAL conversion data registers
9. Clear the interrupt flag bit (ADIF) when A/D interrupt function has occurred.
10. For the next conversion, repeat from Step 1 or Step 2 as required. At least two TCT's are required before the next acquisition starts.

NOTE

To obtain an accurate value, it is necessary to avoid any data transition on the I/O pins during AD conversion.

■ Demonstration Programs

```
;Define the General Registers
R 0 == 0                ; Indirect addressing register
PSW == 3                ; Status register
PORT5 == 5
PORT6 == 6
RA== 0XA                ; Wake-up control register
RF== 0XF                ; Interrupt status register

;Define the Control Register
IOC50 == 0X5            ; Control Register of Port 5
IOC60 == 0X6            ; Control Register of Port 6
C_INT == 0XF            ; Interrupt Control Register

;ADC Control Registers
ADDATAH == 0x8          ; The contents are the results of ADC
ADDATAL == 0x9          ; The contents are the results of ADC
AISR == 0x05            ; ADC input select register
ADCON == 0x6            ; 7    6    5     4    3    2    1    0
                        VREFS CKR1 CKR:0 ADRUN ADPD ADIS2 ADIS1 ADIS0
ADOC == 0x07            ; ADC offset calibration register

;Define Bits in ADCON
ADRUN == 0x4            ; ADC is executed as the bit is set
ADPD == 0x3             ; Power Mode of ADC

;Program Starts
ORG 0                   ; Initial address
JMP INITIAL
ORG 0x30                ; Interrupt vector

(User's Program)        ; Determined by User
;
BANK 0
CLR RF                  ; To clear the ADIF bit
BANK 2
BS ADCON , ADRUN        ; To start to execute the next AD
                        ;  conversion if necessary
RETI
```

```
INITIAL:
BANK        2
MOV A       , @0B00000001   ;Define P60 as an analog input
MOV AISR    , A
MOV A       , @0B00001000   ; Select P60 as an analog input
                            ;  channel, and AD power on
MOV ADCON   , A             ; Define P60 as an input pin and
                            ;  set clock rate at fosc/4
MOV A       , @0B00000000
MOV ADOC    , A             ; Disable calibration

En_ADC:
MOV A       , @0BXXXXXXX1   ; Define P60 as an input pin, and
                            ;  the others are dependent
IOW PORT6                   ;  on applications
BANK        0
MOV A       , @0BXX1XXXXX   ; Enable the ADWE wake-up function
                            ;  of ADC, "X" by application
MOV RA      , A
MOV A       , @0BX1XXXXXX   ; Enable the ADIE interrupt function
                            ;  of ADC, "X" by application
IOW C_INT

ENI                         ; Enable the interrupt function
BANK        2
BS ADCON    , ADRUN         ; Start to run the ADC
                            ; If the interrupt function is
                            ;  employed, the following three
                            ;  lines may be ignored
SLEP                        ; Goto Sleep mode
POLLING:
JBC ADCON   , ADRUN         ; Check the ADRUN bit
                            ;  continuously
JMP POLLING                 ; ADRUN bit will be reset as the AD
                            ;  conversion is completed
(User's program)            ; Read AD converted data from ADDATAH/L
```

6.9 Timer/Counter 3

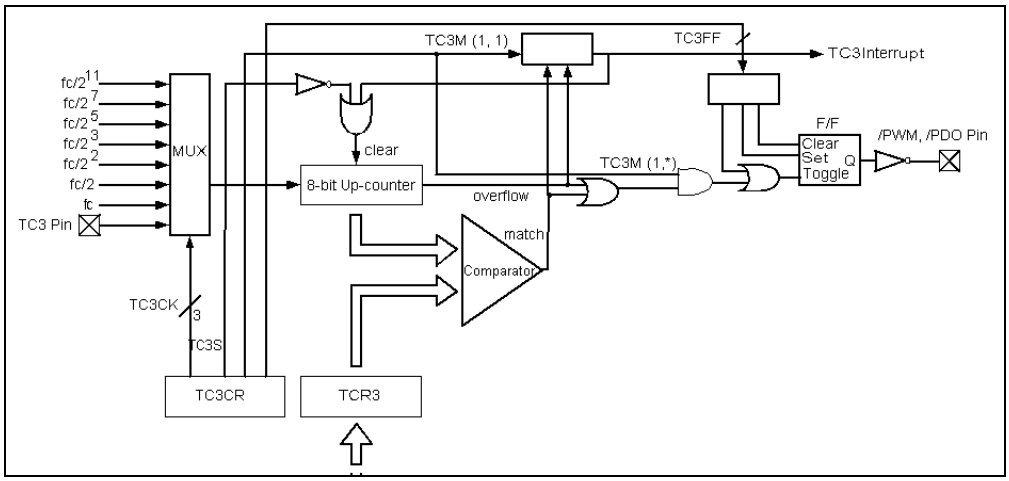


Figure 6-15 Timer/Counter 3 Configuration

In Timer mode, counting up is performed using the internal clock (rising edge trigger). When the contents of the up-counter matched with the contents of TCR3, interrupt is then generated and the counter is cleared. Counting up resumes after the counter is cleared.

In Counter mode, counting up is performed using the external clock input pin (TC3). When the contents of the up-counter matched with the contents of TCR3, interrupt is then generated and the counter is cleared. Counting up resumes after the counter is cleared.

In Programmable Divider Output (PDO) mode, counting up is performed using the internal clock. The contents of TCR3 are compared with the contents of the up-counter. The F/F output is toggled and the counter is cleared each time a match is found. The F/F output is inverted and output to /PDO pin. This mode can generate 50% duty pulse output. **The F/F can be initialized by program and it is initialized to "0" during reset.** A TC3 interrupt is generated each time the /PDO output is toggled.

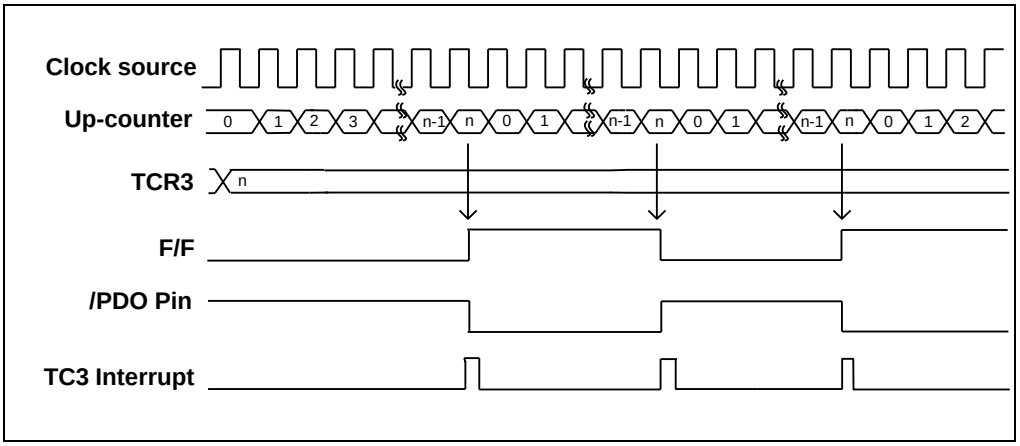


Figure 6-16 PDO Mode Timing Diagram

In Pulse Width Modulation (PWM) Output mode, counting up is performed using the internal clock. The contents of TCR3 are compared with the contents of the up-counter. The F/F is toggled when a match is found. While the counter is counting, the F/F is toggled again when the counter overflows, after which the counter is cleared. The F/F output is inverted and output to the /PWM pin. A TC3 interrupt is generated each time an overflow occurs. **TCR3 is configured as a 2-stage shift register and during output, will not switch until one output cycle is completed even if TCR3 is overwritten.** Hence, the output can be changed continuously. Also, after data is loaded to TCR3, the TCR3 is shifted for the first time by setting TC3S to "**1**".

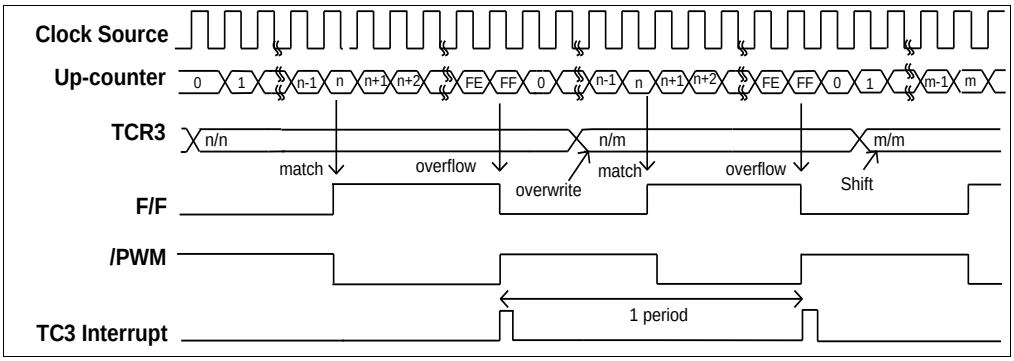


Figure 6-17 PWM Mode Timing Diagram

6.10 Comparator

EM78Fx61N has two comparators, which has two analog inputs and one output. The comparator can be utilized to wake up EM78Fx61N from Sleep mode. Figure below shows the comparator operating mode.

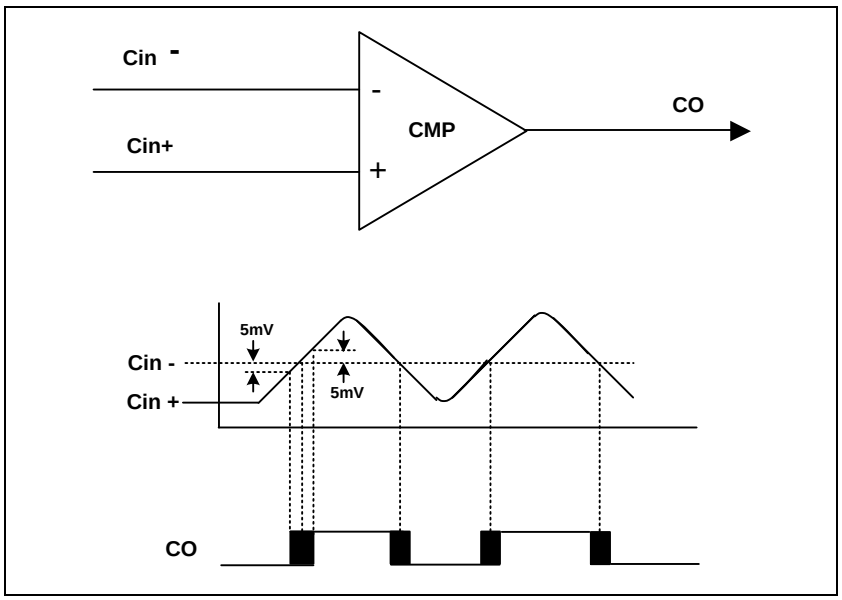


Figure 6-18 Comparator Operating Mode

6.10.1 External Reference Signal

The analog signal that is presented at Cin- is compared to the signal at Cin+, and the digital output (CO) of the comparator is adjusted in accordance with the following considerations:

- The reference signal must be between Vss and Vdd.
- The reference voltage can be applied to either pin of the comparator.
- Threshold detector applications may be of the same reference.
- The comparator can operate from the same or different reference source.

6.10.2 Comparator Outputs

- The compared result is stored in the CPOUT2 of R7 Bit 4 of Bank 3.
- The comparator is output to CO2 (P80) by programming Bit 3, Bit 2 <COS21, COS20> of Register R7 Bank 3.

The Figure below shows the comparator output block diagram.

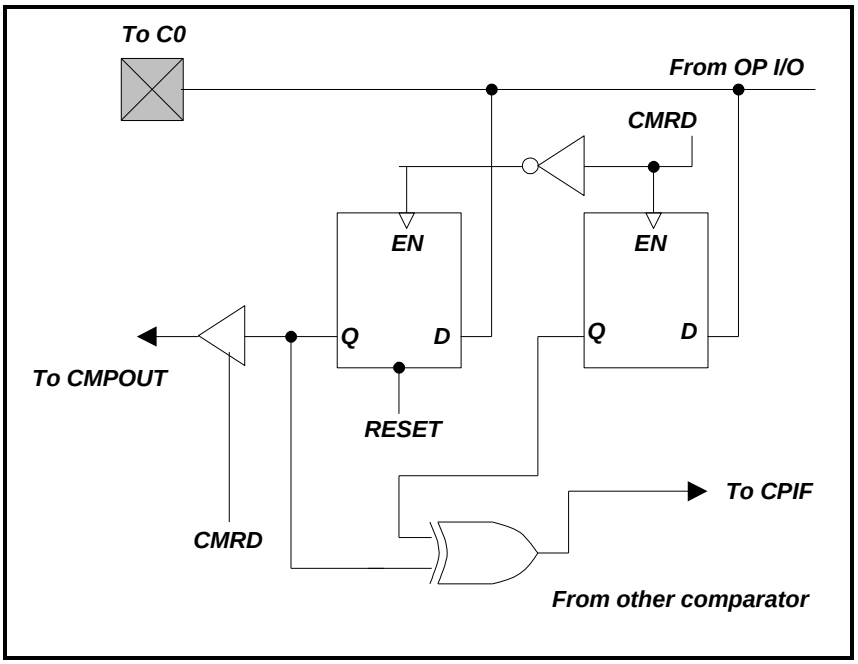


Figure 6-18 Comparator Output Configuration

6.10.3 Interrupt

- CMP2IE (IOCE.7) must be enabled for the “ENI” instruction to take effect.
- Interrupt triggers whenever a change occurs on the comparator output pin.
- The actual change on the pin can be determined by reading Bit CPOUT2, (R7.4, Bank 3).
- CMP2IF (RF.7, Bank 1), the comparator interrupt flag, can only be cleared by software.

6.10.4 Wake-up from Sleep Mode

- If enabled, the comparator remains active and the interrupt remains functional, even in Sleep mode.
- If a mismatch occurs, the interrupt will wake up the device from Sleep mode.
- The power consumption should be taken into consideration for the benefit of energy conservation.
- If the function is unemployed during Sleep mode, turn off the comparator before entering into sleep mode.

6.11 Oscillator

6.11.1 Oscillator Modes

The EM78Fx61N device can be operated in four different oscillator modes, such as Internal RC oscillator mode (IRC), External RC oscillator mode (ERC), High Crystal oscillator mode (HXT), and Low Crystal oscillator mode (LXT). User can select one of such modes by programming OSC2, OSC1, and OSC0 in the Code Option register. Table below depicts how these modes are defined.

■ **Oscillator Modes as Defined by OSC2 ~ OSC0**

Mode	OSC2	OSC1	OSC0
XT (Crystal oscillator mode)	**0**	**0**	**0**
HXT (High Crystal oscillator mode)	**0**	**0**	**1**
LXT1 (Low Crystal 1 oscillator mode)	**0**	**1**	**0**
LXT2 (Low Crystal 2 oscillator mode)	**0**	**1**	**1**
IRC (Internal RC oscillator mode); P55, P54 act as I/O pin	**1**	**0**	**0**
IRC (Internal RC oscillator mode); P55 act as I/O pin P54 act as RCOUT pin	**1**	**0**	**1**
ERC (External RC oscillator mode); P55 act as ERCin pin P54 act as I/O pin	**1**	**1**	**0**
ERC (External RC oscillator mode); P55 act as ERCin pin P54 act as RCOUT pin with Open-drain	**1**	**1**	**1**

Note: *1) Frequency range of HXT mode is 16 MHz ~ 6 MHz*
2) Frequency range of XT mode is 6 MHz ~ 1 MHz
3) Frequency range of LXT1 mode is 1 MHz ~ 100 kHz.
4) Frequency range of LXT2 mode is 32 kHz.

OSCI and OSCO are used in LXT2, LXT1, XT, HXT, and ERC modes. They cannot be used as normal I/O pins.

In IRC mode, P55 is used as normal I/O pin.

The up-limited operation frequency of the crystal/resonator on the different VDD is listed in the following table.

■ **Summary of Maximum Operating Speeds**

Conditions	VDD	Max. Fxt. (MHz)
Two cycles with two clocks	2.5	4.0
	3.0	8.0
	4.5	16.0

6.11.2 Crystal Oscillator/Ceramic Resonators (Crystal)

The EM78Fx61N can be driven by an external clock signal through the OSCI pin as illustrated below.

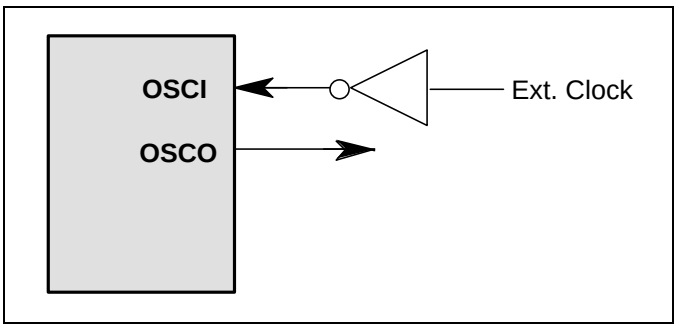


Figure 6-20 Circuit for External Clock Input

In most applications, Pin OSCI and Pin OSCO can be connected with a crystal or ceramic resonator to generate oscillation as depicted in the figure below. The same thing applies whether it is in the HXT mode or in the LXT mode.

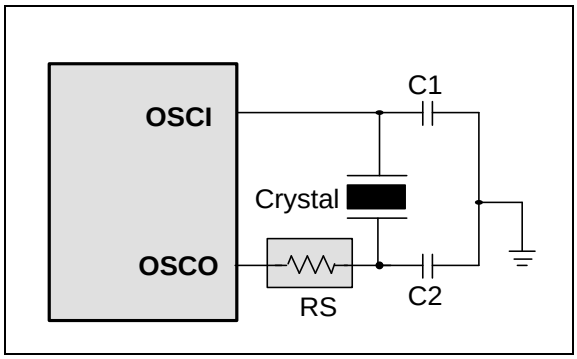


Figure 6-21 Circuit for Crystal/Resonator

The following table provides the recommended values of C1 and C2. Since each resonator has its own attribute, you should refer to its specification for appropriate values of C1 and C2. A serial resistor RS, may be necessary for AT strip cut crystal or low frequency mode.

■ **Capacitor Selection Guide for Crystal Oscillator or Ceramic Resonator**

Oscillator Type	Frequency Mode	Frequency	C1 (pF)	C2 (pF)
Ceramic Resonators	LXT1 (100K~1 MHz)	100 kHz	45pF	45pF
		200 kHz	20pF	20pF
		455 kHz	20pF	20pF
		1.0 MHz	20pF	20pF
	XT (1M~6 MHz)	1.0 MHz	25pF	25pF
		2.0 MHz	20pF	20pF
		4.0 MHz	20pF	20pF
Crystal Oscillator	LXT2 (32.768kHz)	32.768 kHz	40pF	40pF
	LXT1 (100K~1 MHz)	100 kHz	45pF	45pF
		200 kHz	20pF	20pF
		455 kHz	20pF	20pF
		1.0 MHz	20pF	20pF
	XT (1~6 MHz)	455 kHz	30pF	30pF
		1.0 MHz	20pF	20pF
		2.0 MHz	20pF	20pF
		4.0 MHz	20pF	20pF
		6.0 MHz	20pF	20pF
	HXT (6~16 MHz)	6.0 MHz	25pF	25pF
		8.0 MHz	20pF	20pF
		10.0 MHz	20pF	20pF
		12.0 MHz	20pF	20pF
		16.0 MHz	15pF	15pF

6.11.3 External RC Oscillator Mode

For some applications that do not require a very precise timing calculation, the RC oscillator (Figure 6-22 below) offers a cost-effective oscillator configuration. Nevertheless, it should be noted that the frequency of the RC oscillator is influenced by the supply voltage, the values of the resistor (Rext), the capacitor (Cext), and even by the operation temperature. Moreover, the frequency also changes slightly from one chip to another due to manufacturing process variation.

In order to maintain a stable system frequency, the values of the Cext should not be less than 20pF, and that of Rext should not be greater than 1MΩ. If they cannot be kept under this range, the frequency can be easily affected by noise, humidity, and leakage.

The smaller the Rext in the RC oscillator, the faster its frequency will be. However, when a very low Rext value is used, for instance, 1KΩ; the oscillator will become unstable since the NMOS cannot correctly discharge the capacitance current.

Based on the above conditions, it must be kept in mind that all of the supply voltage, the operation temperature, the components of the RC oscillator, the package types, and the PCB layout, could affect the system frequency.

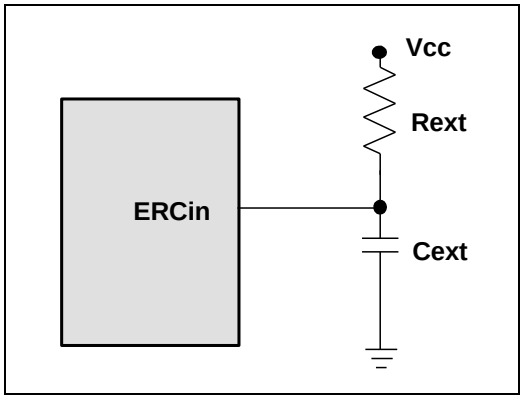


Figure 6-22 External RC Oscillator Mode Circuit

■ **RC Oscillator Frequencies**

Cext	Rext	Average Fosc 5V, 25°C	Average Fosc 3V, 25°C
20 pF	3.3k	3.5 MHz	3.2 MHz
	5.1k	2.5 MHz	2.3 MHz
	10k	1.30 MHz	1.25 MHz
	100k	140 kHz	140 kHz
100 pF	3.3k	1.27 MHz	1.21 MHz
	5.1k	850 kHz	820 kHz
	10k	450 kHz	450 kHz
	100k	48 kHz	50 kHz
300 pF	3.3k	560 kHz	540 kHz
	5.1k	370 kHz	360 kHz
	10k	196 kHz	192 kHz
	100k	20 kHz	20 kHz

Note: *Measured based on DIP packages. These are theoretical values intended for design reference only.*

6.11.4 Internal RC Oscillator Mode

The EM78Fx61N offers a versatile internal RC mode with a default frequency value of 4MHz. Internal RC oscillator mode has other frequencies (16 MHz and 8 MHz) that can be set by Code Option Word1<3,2> or switch by Bank1 R8<7,6>, RCM1 and RCM0. All these three main frequencies can be calibrated by programming the Code Option Word1<8~4>, C4~C0 (auto calibration).

■ **Internal RC Drift Rate (Ta=25°C, VDD=5 V± 5%, VSS=0V)**

Internal RC	Drift Rate			
	Temperature (-40°C~85°C)	Voltage (2.4V~5.5V)	Process	Total
4 MHz	± 3%	± 5%	± 2.5%	± 10.5%
16 MHz	± 3%	± 5%	± 2.5%	± 10.5%
8 MHz	± 3%	± 5%	± 2.5%	± 10.5%

6.12 Code Option Register

The EM78Fx61N has a Code Option Word that is not part of the normal program memory. The option bits cannot be accessed during normal program execution.

Code Option Register and Customer ID Register arrangement distribution**:**

Word 0	Word 1	Word 2
Bit 12~Bit 0	Bit 12~Bit 0	Bit 12~Bit 0

6.12.1 Code Option Register (Word 0)

Word 0											
Bit	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2 ~ Bit 0**
Mnemonic	**–**	**NRHL**	**NRE**	**RESETENB**	**CLKS1**	**CLKS0**	**ENWDTB**	**OSC2**	**OSC1**	**OSC0**	**Protect**
1	–	8/fc	Disable	/RESET	High	High	Enable	High	High	High	Enable
0	–	32/fc	Enable	P83	Low	Low	Disable	Low	Low	Low	Disable

Bit 12: Not used, set to "**0**" at all time

Bit 11 (NRHL): Noise rejection high/low pulse define bit. INT pin is a falling edge trigger.

0: Pulses equal to 32/fc [s] are regarded as signal (default).

1: Pulses equal to 8/fc [s] are regarded as signal.

> **NOTE**
> *The noise rejection function is turned off under Low Crystal Oscillator (LXT2) and Sleep mode.*

Bit 10 (NRE): Noise rejection enable. The INT pin is falling edge triggered.

0: Enable noise rejection (default) but in Low Crystal oscillator (LXT2) mode. The noise rejection circuit is always disabled.

1: Disable noise rejection

Bit 9 (RESETENB): Reset pin enable bit

0: P83 set to I/O pin (default)

1: P83 set to /RESET pin

Bit 8 ~ Bit 7 (CLKS1 ~ CLKS0): Instruction period option bit

Instruction Period	CLKS1	CLKS0
4 clocks (default)	**0**	**0**
2 clocks	**0**	**1**
8 clocks	**1**	**0**
16 clocks	**1**	**1**

Refer to Section 6.16, *Instruction Set*.

Bit 6 (ENWDTB): Watchdog timer enable bit

0: Disable (default)

1: Enable

Bit 5 ~ Bit 3 (OSC2 ~ OSC0): Oscillator Mode Selection bits

Mode	OSC2	OSC1	OSC0
XT (Crystal oscillator mode) (default)	**0**	**0**	**0**
HXT (High Crystal oscillator mode)	**0**	**0**	**1**
LXT1 (Low Crystal 1 oscillator mode)	**0**	**1**	**0**
LXT2 (Low Crystal 2 oscillator mode)	**0**	**1**	**1**
IRC (Internal RC oscillator mode); P55, P54 act as I/O pin	**1**	**0**	**0**
IRC (Internal RC oscillator mode); P55 act as I/O pin P54 act as RCOUT pin	**1**	**0**	**1**
ERC (External RC oscillator mode); P55 act as ERCin pin P54 act as I/O pin	**1**	**1**	**0**
ERC (External RC oscillator mode); P55 act as ERCin pin P54 act as RCOUT pin with Open-Drain	**1**	**1**	**1**

Note: *1. Frequency range of HXT mode is 16 MHz ~ 6 MHz*
2. Frequency range of XT mode is 6 MHz ~ 1 MHz
3. Frequency range of LXT1 mode is 1 MHz ~ 100kHz
4. Frequency range of LXT2 mode is 32kHz

Bit 2 ~ Bit 0 (Protect): Protect bit. Protect type is as follows**:**

Protect	Protect
1	Enable
0	Disable

6.12.2 Code Option Register (Word 1)

Word 1													
Bit	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	COBS0	–	–	HLP	C4	C3	C2	C1	C0	RCM1	RCM0	LVR1	LVR0
1	Register	–	–	High	High	High	High	High	High	High	High	High	High
0	Option	–	–	Low	Low	Low	Low	Low	Low	Low	Low	Low	Low

Bit 12 (COBS0): IRC mode select bit

0: IRC frequency select from code option (default)

1: IRC frequency select from register.

Bit 11: Not used, set to "**0**" at all time

Bit 10: Not used, set to "**1**" at all time

Bit 9 (HLP): Power consumption selection

0: Normal power consumption

1: Low power consumption

Bit 8 ~ Bit 4 (C4 ~ C0): Internal RC mode calibration bits. C4 ~ C0 must be set to "**0**" only (auto-calibration).

Bit 3 ~ Bit 2 (RCM1 ~ RCM0): RC mode select bits

RCM 1	RCM 0	*Frequency (MHz)
0	0	4 (default)
0	1	16
1	0	8
1	1	x

Bit 1 ~ Bit 0 (LVR1 ~ LVR0): Low Voltage Reset Enable bits

LVR1	LVR0	Reset Level	Release Level
0	0	NA	NA
0	1	2.7V	2.9V
1	0	3.5V	3.7V
1	1	4.0V	4.2V

Note: *LVR1, LVR0="0, 0" : LVR disable, power-on reset point of EM78Fx61N is 2.0~2.1V (default).*

LVR1, LVR0="0, 1" : If Vdd <2.7V, the EM78Fx61N will reset.

LVR1, LVR0="1, 0" : If Vdd <3.5V, the EM78Fx61N will reset.

LVR1, LVR0="1, 1" : If Vdd <4.0V, the EM78Fx61N will reset.

6.12.3 Customer ID Register (Word 2)

Word 1													
Bit	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	SC3	SC2	SC1	SC0	–	–	–	–	ID4	ID3	ID2	ID1	ID0
1	High	High	High	High	–	–	–	–	High	High	High	High	High
0	Low	Low	Low	Low	–	–	–	–	Low	Low	Low	Low	Low

Bits 12 ~ 9 (SC3 ~ SC0): Calibrator of sub frequency (WDT frequency, auto calibration)

Bit 8: Not used, set to "**0**" at all time

Bit 7: Not used, set to "**1**" at all time

Bits 6 ~ 5: Not used, set to "**0**" at all time

Bits 4 ~ 0: Customer's ID code

6.13 Power-On Considerations

Any microcontroller is not guaranteed to start to operate properly before the power supply has stabilized. The EM78Fx61N has an on-chip Power-on Voltage Detector (POVD) with a detecting level of 2.0V~2.1V. It will work well if Vdd can rise quickly enough (50ms or less). In many critical applications, however, extra devices are still required to assist in solving power-up problems.

6.14 External Power-on Reset Circuit

The circuit shown below uses an external RC to produce a reset pulse. The pulse width (time constant) should be kept long enough for Vdd to reach minimum operation voltage. This circuit is used when the power supply has a slow rise time. Since the current leakage from the /RESET pin is ± 5 μA, it is recommended that R should not be greater than 40 KΩ in for the /RESET pin voltage to remain at below 0.2V. The diode (D) functions as a short circuit at the moment of power down. The capacitor C will discharge rapidly and fully. The current-limited resistor (Rin) will prevent high current or ESD (electrostatic discharge) from flowing to /RESET pin.

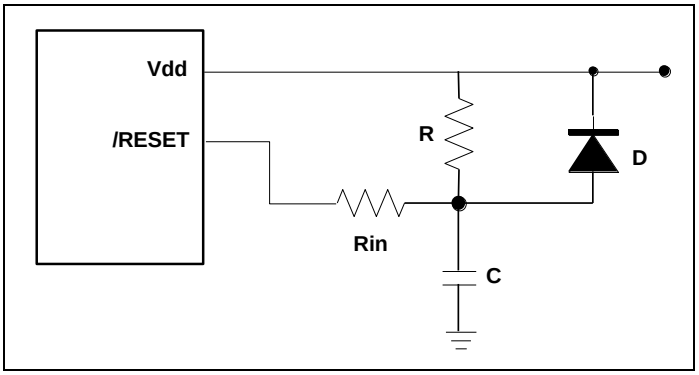


Figure 6-23 External Power-up Reset Circuit

6.15 Residue-Voltage Protection

When the battery is replaced, the device power (Vdd) is taken off but residue-voltage remains. The residue-voltage may trip below Vdd minimum, but not to zero. This condition may cause a poor power-on reset. Figure 6-23 and Figure 6-24 show how to create a proper residue-voltage protection circuit.

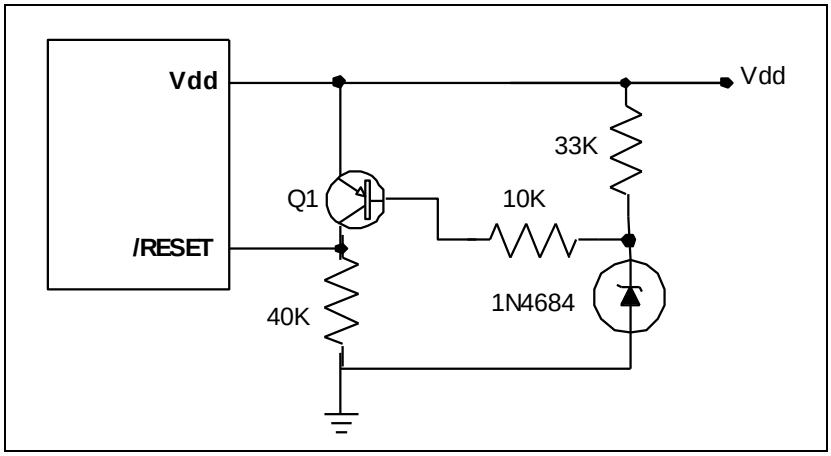


Figure 6-24 Residue Voltage Protection Circuit 1

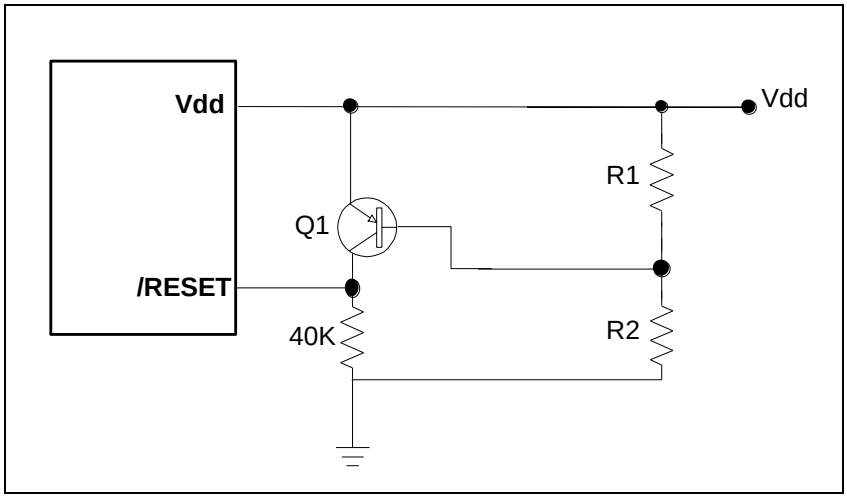


Figure 6-25 Residue Voltage Protection Circuit 2

6.16 Instruction Set

Each instruction in the Instruction Set is a 13-bit word divided into an OP code and one or more operands. Normally, all instructions are executed within one single instruction cycle (one instruction consists of two oscillator periods), unless the program counter is changed by instructions "MOV R2, A", "ADD R2, A", or by instructions of arithmetic or logic operation on R2 (e.g., "SUB R2, A", "BS(C) R2,6", "CLR R2", etc.). In this case, the execution takes two instruction cycles.

If for some reasons, the specification of the instruction cycle is not suitable for certain applications, try to modify the instruction as follows**:**

A) Change one instruction cycle to consist of four oscillator periods.

B) "TBRD", "RET", "RETL", "RETI", or the conditional skip ("JBS", "JBC", "JZ", "JZA", "DJZ", "DJZA") commands which were tested to be true, are executed within two instruction cycles. The instructions that are written to the program counter also take two instruction cycles.

Case A is selected by the Code Option bit called CLKS. One instruction cycle consists of two oscillator clocks if CLKS1&0 is “**01**”, and four oscillator clocks if CLKS1&0 is “**00**” (see Section 6.12.1 *(Code Option Register (Word 0)*).

Note that once the four oscillator periods within one instruction cycle is selected as in Case A, the internal clock source for TCC should be CLK = Fc as indicated in Figure 6-7 *(TCC and WDT Block Diagram)* in Section 6.3.

In addition, the Instruction Set has the following features**:**

1) Every bit of any register can be set, cleared, or tested directly.

2) The I/O register can be regarded as general register. That is, the same instruction can operate on the I/O register.

■ Instruction Set Table

The following symbols are used in the following table:

R = *Register designator that specifies which one of the registers (including operation and general purpose registers) is to be utilized by the instruction.*

b = *Bit field designator that selects the value for the bit located in the Register R and which affects the operation.*

k = *8 or 10-bit constant or literal value*

Mnemonic	Operation	Status Affected
NOP	No Operation	None
DAA	Decimal Adjust A	C
CONTW	A → CONT	None
SLEP	0 → WDT, Stop oscillator	T, P
WDTC	0 → WDT	T, P
IOW R	A → IOCR	None[1]
ENI	Enable Interrupt	None
DISI	Disable Interrupt	None
RET	[Top of Stack] → PC	None
RETI	[Top of Stack] → PC, Enable Interrupt	None
CONTR	CONT → A	None
IOR R	IOCR → A	None[1]
MOV R,A	A → R	None
CLRA	0 → A	Z
CLR R	0 → R	Z
SUB A,R	R-A → A	Z, C, DC
SUB R,A	R-A → R	Z, C, DC
DECA R	R-1 → A	Z
DEC R	R-1 → R	Z
OR A,R	A ∨ R → A	Z
OR R,A	A ∨ R → R	Z
AND A,R	A & R → A	Z
AND R,A	A & R → R	Z
XOR A,R	A ⊕ R → A	Z
XOR R,A	A ⊕ R → R	Z
ADD A,R	A + R → A	Z, C, DC
ADD R,A	A + R → R	Z, C, DC
MOV A,R	R → A	Z
MOV R,R	R → R	Z
COMA R	/R → A	Z
COM R	/R → R	Z

[1] *This instruction is applicable to IOC5~IOC7, IOCA ~ IOCF only.*

(Continuation)

Mnemonic	Operation	Status Affected
INCA R	R+1 → A	Z
INC R	R+1 → R	Z
DJZA R	R-1 → A, skip if zero	None
DJZ R	R-1 → R, skip if zero	None
RRCA R	R(n) → A(n-1), R(0) → C, C → A(7)	C
RRC R	R(n) → R(n-1), R(0) → C, C → R(7)	C
RLCA R	R(n) → A(n+1), R(7) → C, C → A(0)	C
RLC R	R(n) → R(n+1), R(7) → C, C → R(0)	C
SWAPA R	R(0-3) → A(4-7), R(4-7) → A(0-3)	None
SWAP R	R(0-3) ↔ R(4-7)	None
JZA R	R+1 → A, skip if zero	None
JZ R	R+1 → R, skip if zero	None
BC R,b	0 → R(b)	None[2]
BS R,b	1 → R(b)	None [3]
JBC R,b	if R(b)=0, skip	None
JBS R,b	if R(b)=1, skip	None
CALL k	PC+1 → [SP], (Page, k) → PC	None
JMP k	(Page, k) → PC	None
MOV A,k	k → A	None
OR A,k	A ∨ k → A	Z
AND A,k	A & k → A	Z
XOR A,k	A ⊕ k → A	Z
RETL k	k → A, [Top of Stack] → PC	None
SUB A,k	k-A → A	Z, C, DC
ADD A,k	k+A → A	Z, C, DC
BANK k	K → R4(7:6)	None
TBRD R	If Bank 3 R6.7=0, machine code (7:0) → R Else Bank 3 R6.7=1, machine code (12:8) → R(4:0), R(7:5)=(0,0,0)	None

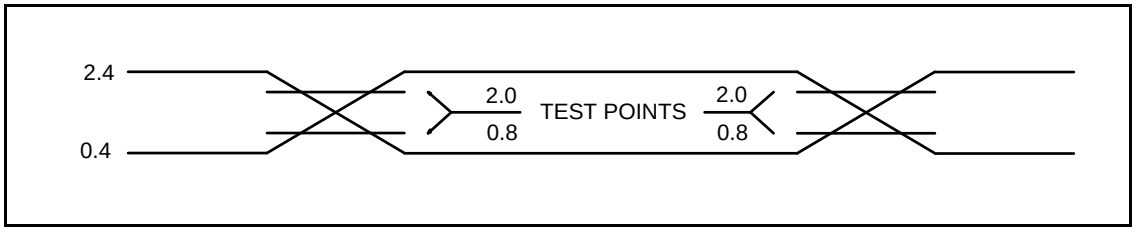
[2] *This instruction is not recommended for interrupt status register operation.*
If you want to clear Bit0 for interrupt status register (ex: 0xF), use the method below:

```
MOV     A,@0B11111110
AND     0xF,A
```

[3] *This instruction cannot operate under interrupt status register.*

7 Timing Diagram

■ AC Test Input / Output Waveform



Note: *AC Testing**:** Input are driven at 2.4V for Logic "**1**" and 0.4V for Logic "**0**"*
*Timing measurements are made at 2.0V for Logic "**1**" and 0.8V for Logic "**0**"*

Figure 7-1 AC Test Input / Output Waveform Timing Diagram

■ Reset Timing (CLK1:0 = "01")

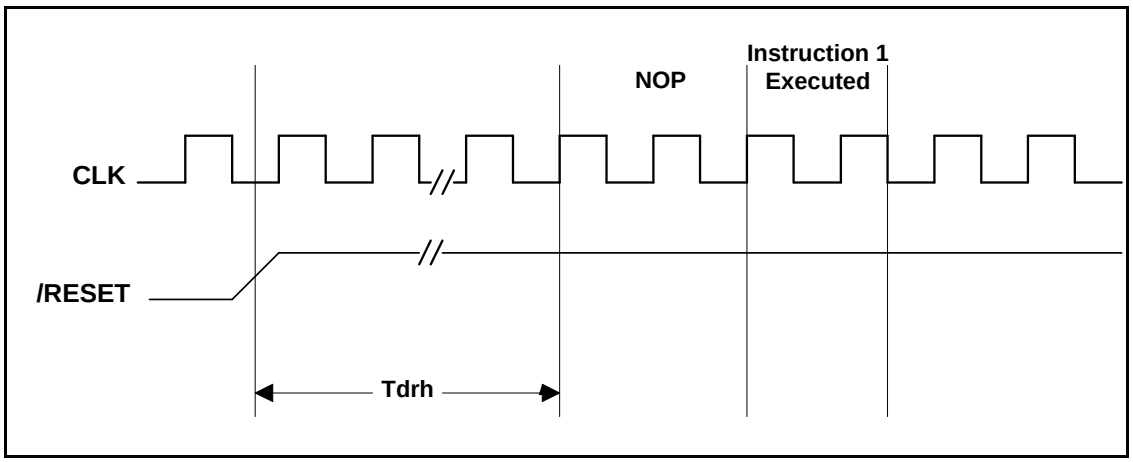


Figure 7-2 Reset Timing Diagram

8 Absolute Maximum Ratings

Items	Rating		
Temperature under bias	-40°C	to	85°C
Storage temperature	-65°C	to	150°C
Working voltage	2.2V	to	5.5V
Working frequency	DC	to	16 MHz
Input voltage	Vss-0.3V	to	Vdd+0.5V
Output voltage	Vss-0.3V	to	Vdd+0.5V

NOTE: *These parameters are theoretical values only and have not been verified.*

9 DC Electrical Characteristics

■ **Ta=25°C, VDD=5.0V ± 5%, VSS=0V**

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Fxt	Crystal: VDD to 3V	Two cycles with two clocks	DC	–	8	MHz
	Crystal: VDD to 5V		DC	–	16	MHz
	ERC: VDD to 5V	R: 5.1KΩ, C: 300 pF	F-30%	370	F+30%	kHz
	IRC: VDD to 5 V	4 MHz, 16 MHz, 8 MHz	F-2.5%	F	F+2.5%	Hz
IIL	Input Leakage Current for input pins	VIN = VDD, VSS	–	–	±1	μA
VIHRC	Input High Threshold Voltage (Schmitt Trigger)	OSCI in RC mode	–	3.5	–	V
IERC1	Sink current	VI from low to high, VI=5V	21	22	23	mA
VILRC	Input Low Threshold Voltage (Schmitt Trigger)	OSCI in RC mode	–	1.5	–	V
IERC2	Sink current	VI from high to low, VI=2V	16	17	18	mA
VIH1	Input High Voltage (Schmitt Trigger)	Ports 5, 6, 8	0.7VDD	–	VDD + 0.3V	V
VIL1	Input Low Voltage (Schmitt Trigger)	Ports 5, 6, 8	-0.3V	–	0.3VDD	V
VIHT1	Input High Threshold Voltage (Schmitt Trigger)	/RESET	0.7VDD	–	VDD + 0.3V	V
VILT1	Input Low Threshold Voltage (Schmitt Trigger)	/RESET	-0.3V	–	0.3VDD	V
VIHT2	Input High Threshold Voltage (Schmitt Trigger)	INT	0.7VDD	–	VDD+0.3V	V
VILT2	Input Low Threshold Voltage (Schmitt Trigger)	INT	-0.3V	–	0.3VDD	V

(Continuation)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VIHX1	Clock Input High Voltage	OSCI in crystal mode	–	3.0	–	V
VILX1	Clock Input Low Voltage	OSCI in crystal mode	–	1.8	–	V
IOH1	Output High Voltage (Ports 5, 6, 8)	VOH = VDD-0.5V (IOH =3.7mA)	-3.0	-4.2	–	mA
IOL1	Output Low Voltage (Ports 5, 8)	VOL = GND + 0.5V	9	11	–	mA
IOL2	Output Low Voltage (Port 6)	VOL = GND + 0.5V	15	18	–	mA
LVR1	Low voltage reset level	Ta= 25°C	2.4	2.7	3.02	V
LVR2	Low voltage reset level	Ta= 25°C	3.09	3.5	3.98	V
LVR3	Low voltage reset level	Ta= 25°C	3.51	4.0	4.51	V
IPH	Pull-high current	Pull-high active, Input pin at VSS	–	-70	-80	μA
IPL	Pull-low current	Pull-low active, Input pin at Vdd	–	20	30	μA
ISB1	Power down current	All input and I/O pins at VDD, Output pin floating, WDT disabled	–	1.0	1.5	μA
ISB2	Power down current	All input and I/O pins at VDD, Output pin floating, WDT enabled	–	8	10	μA
ICC1	Operating supply current at two clocks	/RESET= 'High', Fosc=32kHz (Crystal type, CLKS1:0="01"), Output pin floating, WDT disabled.	–	37	40	μA
ICC2	Operating supply current at two clocks	/RESET= 'High', Fosc=32kHz (Crystal type, CLKS1:0="01"), Output pin floating, WDT enabled.	–	39	43	μA
ICC3	Operating supply current at two clocks	/RESET= 'High', Fosc=455kHz (Crystal type, CLKS1:0="01"), Output pin floating, WDT enabled. (*VDD = 3V)	–	110	120	μA

(Continuation)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
ICC4	Operating supply current at two clocks	/RESET = 'High', Fosc = 4 MHz (Crystal type, CLKS1:0 = "01"), Output pin floating, WDT enabled	–	1.1	1.5	mA
ICC5	Operating supply current at two clocks	/RESET = 'High', Fosc = 10 MHz (Crystal type, CLKS1:0 = "01"), Output pin floating, WDT enabled	–	2.7	3	mA

NOTE

- *The above parameters are theoretical values only and have not been tested or verified. They are provided for design reference only.*
- *Data under the "**Min.**", "**Typ.**", and "**Max.**" (Minimum, Typical, and Maximum) columns are based on hypothetical results at 25°C.*

■ Data EEPROM Electrical Characteristics (Only for EM78F661N)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Tprog	Erase/Write cycle time	Vdd = 2.5~ 5.5V Temperature = -40°C ~ 85°C	–	4.0	4.2	ms
Treten	Data Retention		–	10	–	years
Tendu	Endurance time		–	1000K	–	cycles
Iprg	Programming	Vdd<=3.3V	-	0.6	-	mA
		Vdd<=5.5V	-	1.0	-	mA
Iread	Read	Vdd<=3.3V	-	1.0	-	mA
		Vdd<=5.5V	-	2.5	-	mA

■ Program Flash Memory Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Tprog	Erase/Write cycle time	Vdd = 5.0V Temperature = -40°C ~ 85°C	–	–	–	ms
Treten	Data Retention		–	10	–	years
Tendu	Endurance time		–	100K	–	cycles

■ **A/D Converter Characteristics** (Vdd=2.5V to 5.5V, Vss=0V, Ta=25°C)

Symbol		Parameter	Condition	Min.	Typ.	Max.	Unit
V_{AREF}		Analog reference voltage	V_{AREF} - V_{ASS} ≥ 2.5V	2.5	–	Vdd	V
V_{ASS}				Vss	–	Vss	V
VAI		Analog input voltage	–	V_{ASS}	–	V_{AREF}	V
IAI1	Ivdd	Analog supply current	Vdd=VAREF=5.0V, VASS =0V (V reference from Vdd)	1150	1300	1450	μA
	Ivref			-10	0	10	μA
IAI2	Ivdd	Analog supply current	Vdd=VAREF=5.0V, VASS =0V (V reference from VREF)	700	800	900	μA
	IVref			450	500	550	μA
RN		Resolution	Vdd=V_{AREF}=5.0V, V_{ASS} =0V	8	9	–	Bits
LN		Linearity error	Vdd = 2.5 to 5.5V Ta=25°C	–	±2	±4	LSB
DNL		Differential nonlinear error	Vdd = 2.5 to 5.5V Ta=25°C	–	±0.5	±0.9	LSB
FSE		Full scale error	Vdd=V_{AREF}=5.0V, V_{ASS} =0V	–	±1	±2	LSB
OE		Offset error	Vdd=V_{AREF}=5.0V, V_{ASS} =0V	–	±1	±2	LSB
ZAI		Recommended impedance of analog voltage source	–	–	8	10	KΩ
TAD1		A/D clock period	Vdd=V_{AREF}=2.5~5.5V, V_{ASS} =0V	4	–	–	μs
TAD2		A/D clock period	Vdd=V_{AREF}=3.0~5.5V, V_{ASS} =0V	1	–	–	μs
TCN		A/D conversion time	Vdd=V_{AREF}=5.0V, V_{ASS} =0V	14	–	14	TAD
ADIV		A/D OP input voltage range	Vdd=V_{AREF}=5.0V, V_{ASS} =0V	0	–	V_{AREF}	V
PSR		Power Supply Rejection	Vdd=5.0V±0.5V	–	–	±2	LSB

NOTE

- *These parameters are theoretical values and have not been tested. are provided for design reference only.*
- *When A/D is off, no current is consumed other than minor leakage current.*
- *The A/D conversion result does not decrease with an increase in the input voltage, and no missing code will result.*
- *The parameters are subject to change without prior notice.*

■ **Comparator Electrical Characteristics**

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VOS	Input offset voltage	RL = 5.1K[1]	–	–	5	mV
Vcm	Input common-mode voltages range[2]	–	GND	–	VDD	V
ICO	Supply current of Comparator	–	–	200	–	μA
TRS	Response time	Vin(-)=2.5V, Vdd=5V, CL=15p (comparator output load), overdrive=30mV[3]	–	0.7	–	μs
TLRS	Large signal response time	Vin(-)=2.5V, Vdd=5V, CL=15p (comparator output load),	–	300	–	ns
VS	Operating range	–	2.5	–	5.5	V

[1] *The output voltage is in the unit gain circuitry and over the full input common-mode range.*

[2] *The input common-mode voltage or any of the input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is VDD.*

[3] *The response time specified is a 100mV input step with 30mV overdrive.*

10 AC Electrical Characteristics

■ **0 ≤ Ta ≤ 70°C, VDD=5V, VSS=0V**

■ **–40 ≤ Ta ≤ 85°C, VDD=5V, VSS=0V**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Dclk	Input CLK duty cycle	–	45	50	55	%
Tins	Instruction cycle time (CLKS1:0="01")	Crystal type	100	–	DC	ns
		RC type	500	–	DC	ns
Ttcc	TCC input period	–	(Tins+20)/N*	–	–	ns
Tdrh	Device reset hold time	–	14	16	18	ms
Trst	/RESET pulse width	Ta = 25°C	2000	–	–	ns
Twdt	Watchdog timer period	Ta = 25°C	14	16	18	ms
Tset	Input pin setup time	–	–	0	–	ns
Thold	Input pin hold time	–	–	20	–	ns
Tdelay	Output pin delay time	Cload = 20 pF	–	50	–	ns

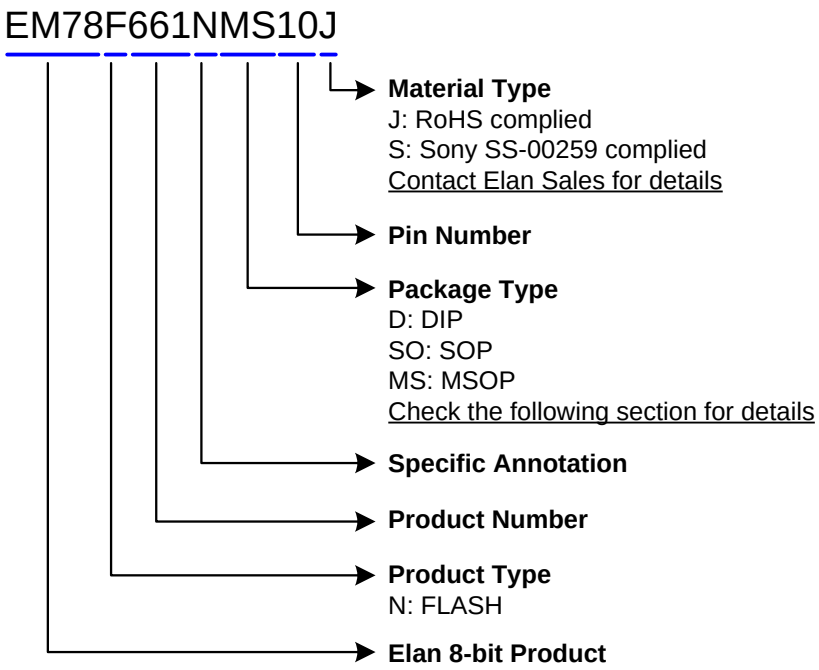
*__N__ = *Selected prescaler ratio*

NOTE

- *The above parameters are theoretical values only and have not been tested or verified. They are provided for design reference only.*
- *Data under the "**Min.**", "**Typ.**" and "**Max.**" (Minimum, Typical, and Maximum) columns are based on hypothetical results at 25°C.*

APPENDIX

A Ordering and Manufacturing Information

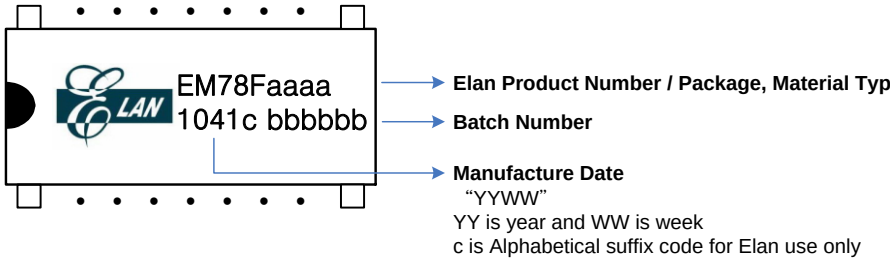


For example:

EM78F661NMS10J

is EM78F661N with FLASH program memory, product,
in 10-pin DIP 118mil package with RoHS complied

IC Mark



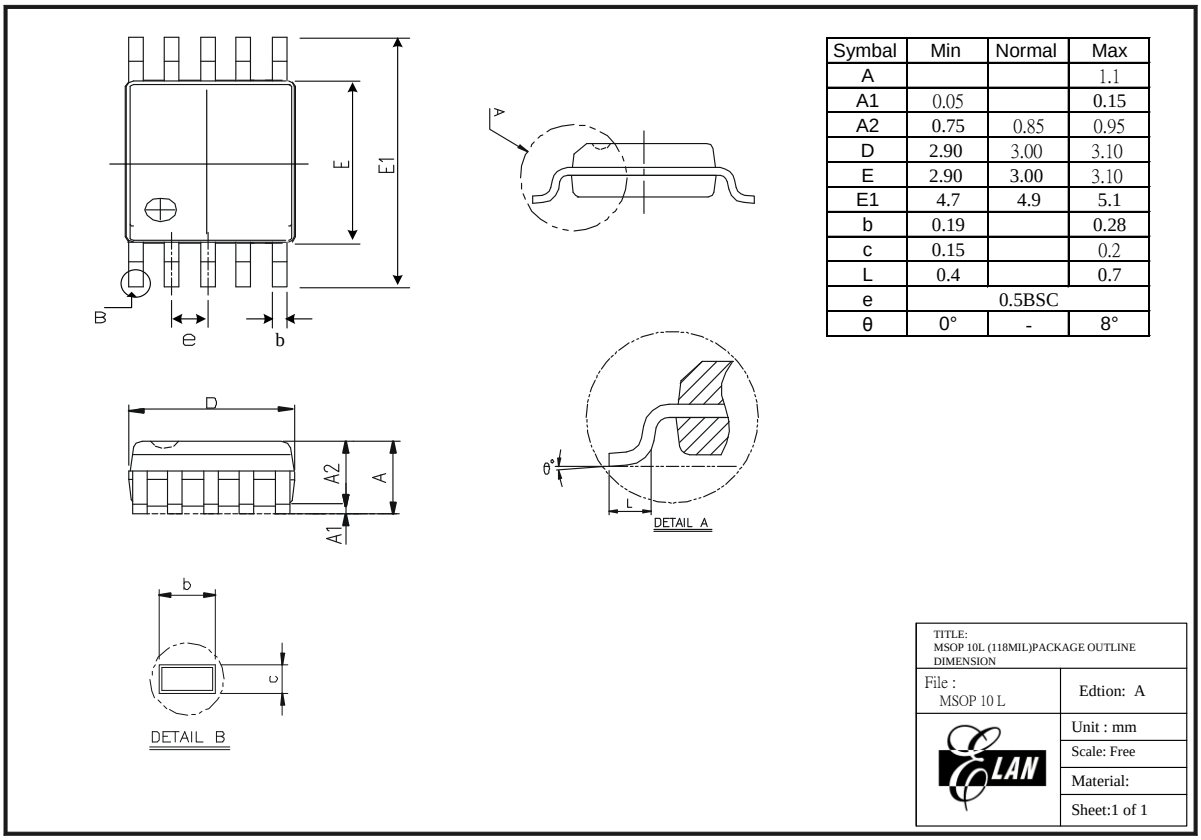
B Package Type

Flash MCU	Package Type	Pin Count	Package Size
EM78Fx61NMS10	MSOP	10	118 mil
EM78Fx61NSO14	SOP	14	150 mil
EM78Fx61NAD16	DIP	16	300 mil
EM78Fx61NASO16A	SOP	16	150 mil

Part No.	EM78Fx61NxJ/xS
Electroplate type	Pure Tin
Ingredient (%)	Sn: 100%
Melting point (°C)	232˚C
Electrical resistivity (μΩ cm)	11.4
Hardness (hv)	8~10
Elongation (%)	>50%

C Packaging Configuration

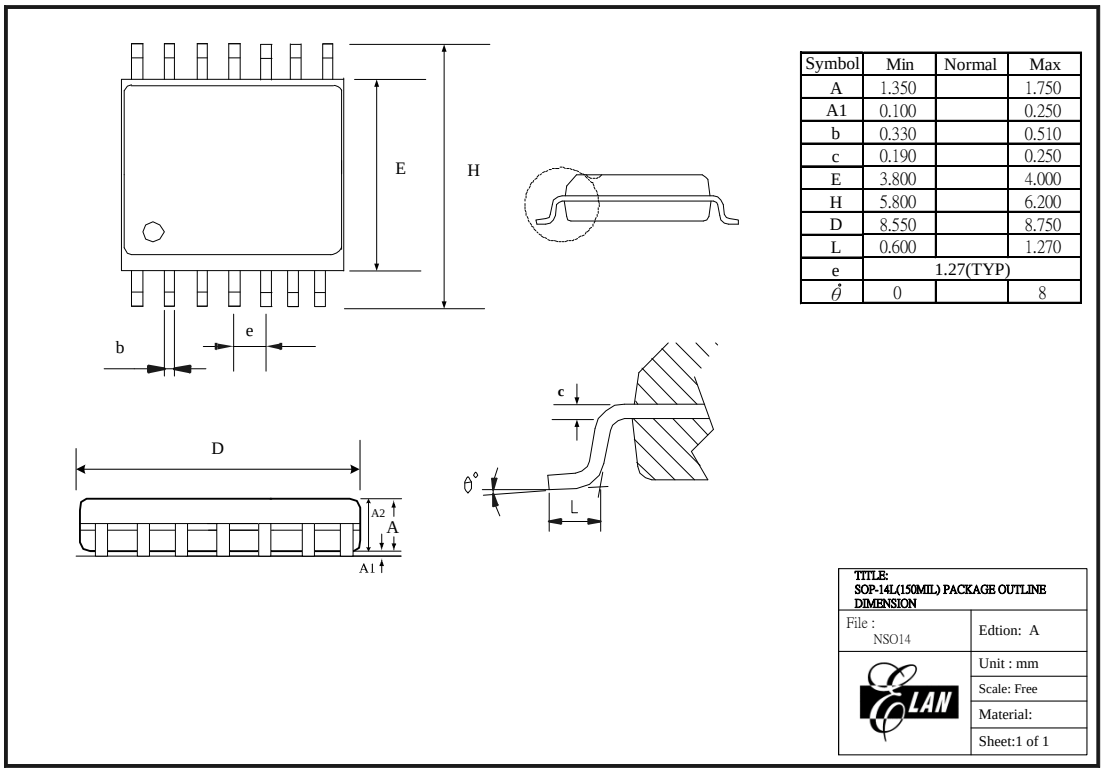
C.1 EM78Fx61NMS10



Symbal	Min	Normal	Max
A			1.1
A1	0.05		0.15
A2	0.75	0.85	0.95
D	2.90	3.00	3.10
E	2.90	3.00	3.10
E1	4.7	4.9	5.1
b	0.19		0.28
c	0.15		0.2
L	0.4		0.7
e		0.5BSC	
θ	0°	-	8°

Figure C-1 EM78Fx61N 10-pin MSOP Package Type

C.2 EM78Fx61NSO14



Symbol	Min	Normal	Max
A	1.350		1.750
A1	0.100		0.250
b	0.330		0.510
c	0.190		0.250
E	3.800		4.000
H	5.800		6.200
D	8.550		8.750
L	0.600		1.270
e	1.27(TYP)		
θ	0		8

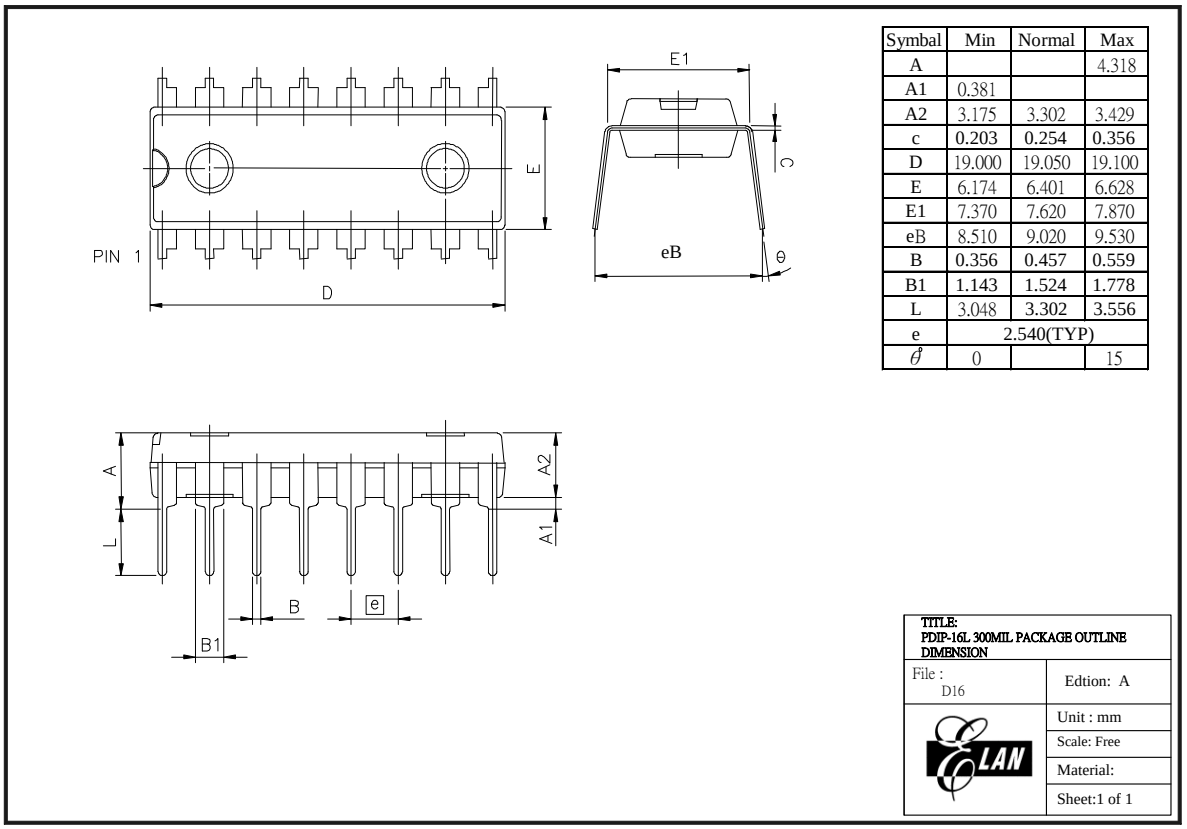
TITLE:
SOP-14L(150MIL) PACKAGE OUTLINE DIMENSION

File : NSO14 | Edtion: A

Unit : mm
Scale: Free
Material:
Sheet:1 of 1

Figure C-2 EM78Fx61N 14-pin SOP Package Type

C.3 EM78Fx61NAD16



Symbal	Min	Normal	Max
A			4.318
A1	0.381		
A2	3.175	3.302	3.429
c	0.203	0.254	0.356
D	19.000	19.050	19.100
E	6.174	6.401	6.628
E1	7.370	7.620	7.870
eB	8.510	9.020	9.530
B	0.356	0.457	0.559
B1	1.143	1.524	1.778
L	3.048	3.302	3.556
e	2.540(TYP)		
θ°	0		15

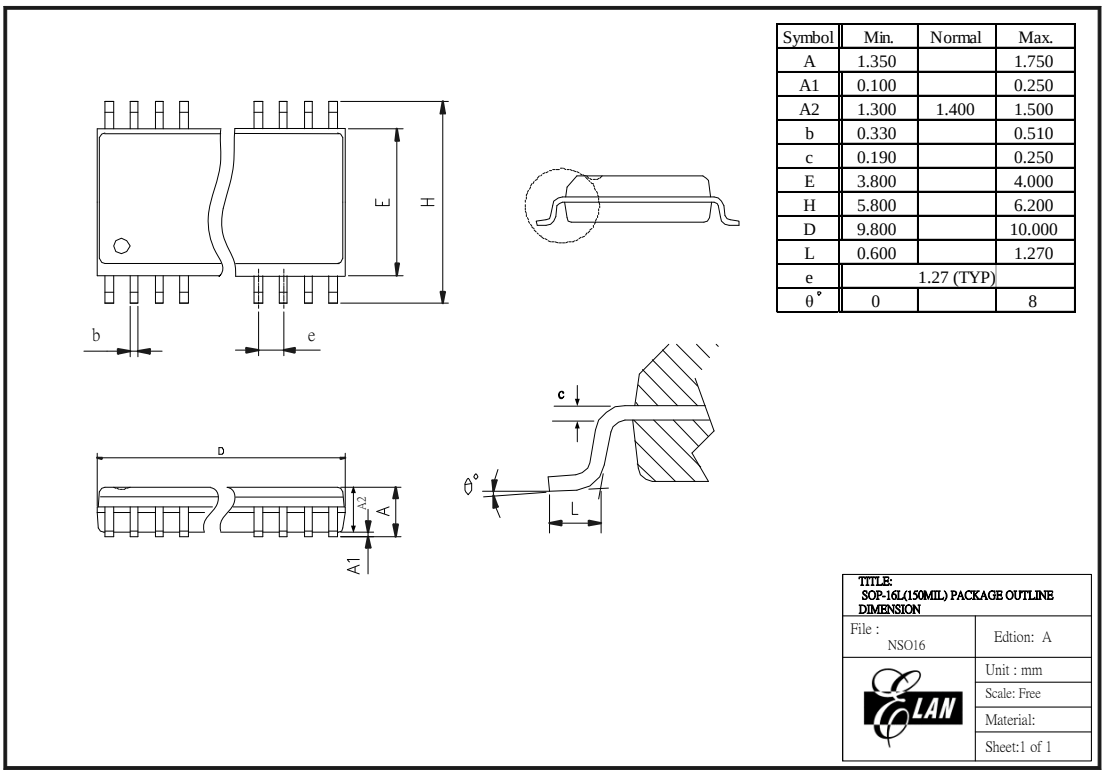
TITLE:
PDIP-16L 300MIL PACKAGE OUTLINE DIMENSION

File : D16 | Edtion: A

Unit : mm
Scale: Free
Material:
Sheet:1 of 1

Figure C-3 EM78Fx61N 16-pin DIP Package Type

C.4 EM78Fx61NASO16A



Symbol	Min.	Normal	Max.
A	1.350		1.750
A1	0.100		0.250
A2	1.300	1.400	1.500
b	0.330		0.510
c	0.190		0.250
E	3.800		4.000
H	5.800		6.200
D	9.800		10.000
L	0.600		1.270
e	1.27 (TYP)		
θ°	0		8

Figure C-4 EM78Fx61N 16-pin SOP Package Type

D Quality Assurance and Reliability

Test Category	Test Conditions	Remarks
Solderability	Solder temperature=245±5°C, for 5 seconds up to the stopper using a rosin-type flux	–
Pre-condition	Step 1: TCT, 65°C (15 min)~150°C (15 min), 10 cycles	For SMD IC (such as SOP, QFP, SOJ, etc)
	Step 2: Bake at 125°C, TD (endurance)=24 hrs	
	Step 3: Soak at 30°C/60%，TD (endurance)=192 hrs	
	Step 4: IR flow 3 cycles (Pkg thickness ≥ 2.5 mm or Pkg volume ≥ 350 mm^3 ----225±5°C) (Pkg thickness ≤ 2.5 mm or Pkg volume ≤ 350 mm^3 ----240 ± 5°C)	
Temperature cycle test	-65°C (15 min)~150°C (15 min), 200 cycles	–
Pressure cooker test	TA =121°C, RH=100%, pressure=2 atm, TD (endurance)= 96 hrs	–
High temperature / High humidity test	TA=85°C , RH=85%，TD (endurance) = 168 , 500 hrs	–
High-temperature storage life	TA=150°C, TD (endurance) = 500, 1000 hrs	–
High-temperature operating life	TA=125°C, VCC = Max. operating voltage, TD (endurance) = 168, 500, 1000 hrs	–
Latch-up	TA=25°C, VCC = Max. operating voltage, 150mA/20V	–
ESD (HBM)	TA=25°C, ≥｜± 3KV｜	IP_ND,OP_ND,IO_ND IP_NS,OP_NS,IO_NS IP_PD,OP_PD,IO_PD, IP_PS,OP_PS,IO_PS, VDD-VSS(+),VDD_VSS(-) mode
ESD (MM)	TA=25°C, ≥ ｜± 300V｜	

D.1 Address Trap Detect

Address Trap Detect is one of the MCU embedded fail-safe functions that detects MCU malfunction caused by noise or the like. Whenever the MCU attempts to fetch an instruction from a certain section of ROM, an internal recovery circuit is auto started. If a noise-caused address error is detected, the MCU will repeat execution of the program until the noise is eliminated. The MCU will then continue to execute the next program.