DALLAS
SEMICONDUCTOR

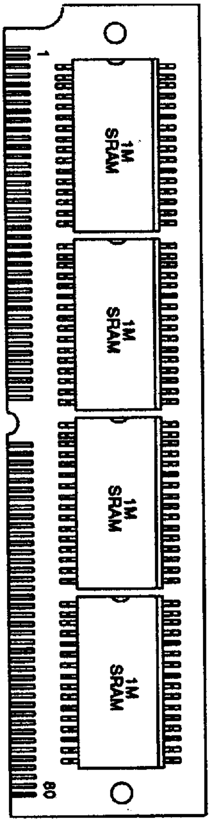
DS2229
Word-Wide 8 Meg SRAM Stik

T-46-23-14

FEATURES

- Organized as a high density 512K x 16 bit Stik™
- Fast access times – 85ns, 100ns, 120ns
- Unlimited write cycles
- Employs popular JEDEC standard 80-position SIMM connector
- Full ± 10% operating range
- Read cycle time equals write cycle time
- Ultra-low standby current < 20 µA
- Suitable for battery-backed applications

PIN ASSIGNMENT



80-pin SIP Stik

DESCRIPTION

The DS2229 is a 8,388,608-bit low-power fully static Random Access Memory organized as a 524,888 word by 16 bits using CMOS technology. The device employs the popular JEDEC standard 80-pin SIMM connection scheme with no additional circuitry required. The device operates from a single power supply with a voltage input of 4.5 to 5.5 volts. The Chip Enable inputs ($\overline{CE0}$, $\overline{CE1}$, $\overline{CE2}$, $\overline{CE3}$) are used for device selection and can be used in order to achieve the minimum standby current mode which facilitates battery backup. The device provides a fast access time of 85nS. The DS2229 maintains TTL levels over input voltage range 4.5V to 5.5V. The DS2229 is JEDEC pin compatible (see Figure 1) with flash EEPROM memory SIMM boards of similar density.

PIN DESCRIPTION Figure 1

PIN #	PIN NAME	PIN #	PIN NAME	PIN #	PIN NAME
1	GND	32	NC	63	DQ_7
2	V_{CC}	33	NC	64	DQ_6
3	NC	34	NC	65	DQ_5
4	$\overline{OE}$	35	CS	66	DQ_4
5	$\overline{WEH}$	36	A_{16}	67	DQ_3
6	$\overline{WEL}$	37	A_{15}	68	DQ_2
7	NC	38	A_{14}	69	DQ_1
8	NC	39	A_{13}	70	DQ_0
9	NC	40	A_{12}	71	NC
10	NC	41	A_{11}	72	V_{CC}
11	NC	42	A_{10}	73	NC
12	NC	43	A_9	74	GND
13	NC	44	A_8	75	NC
14	NC	45	A_7	76	GND
15	NC	46	A_6	77	GND
16	NC	47	A_5	78	
17	NC	48	A_4	79	
18	NC	49	A_3	80	GND
19	NC	50	A_2		
20	NC	51	A_1		
21	$\overline{CE3}$	52	A_0		
22	$\overline{CE2}$	53	GND		
23	$\overline{CE1}$	54	GND		
24	$\overline{CE0}$	55	DQ_{15}		
25	GND	56	DQ_{14}		
26	NC	57	DQ_{13}		
27	NC	58	DQ_{12}		
28	NC	59	DQ_{11}		
29	NC	60	DQ_{10}		
30	NC	61	DQ_9		
31	NC	62	DQ_8		

PIN NAME	DESCRIPTION
$A_0 - A_{16}$	Address Input
$\overline{WEL}$	Write Enable Input Low
$\overline{WEH}$	Write Enable Input High
$\overline{OE}$	Output Enable Input
NC	No Connect
$\overline{CE0} - \overline{CE3}$	Chip Enable Input
CS	Chip Select
$DQ_0 - DQ_{15}$	Data Input/Output
V_{CC}	+5 Volts
GND	Ground

DS2229 STATIC RAM MODULE FUNCTION DIAGRAM Figure 2

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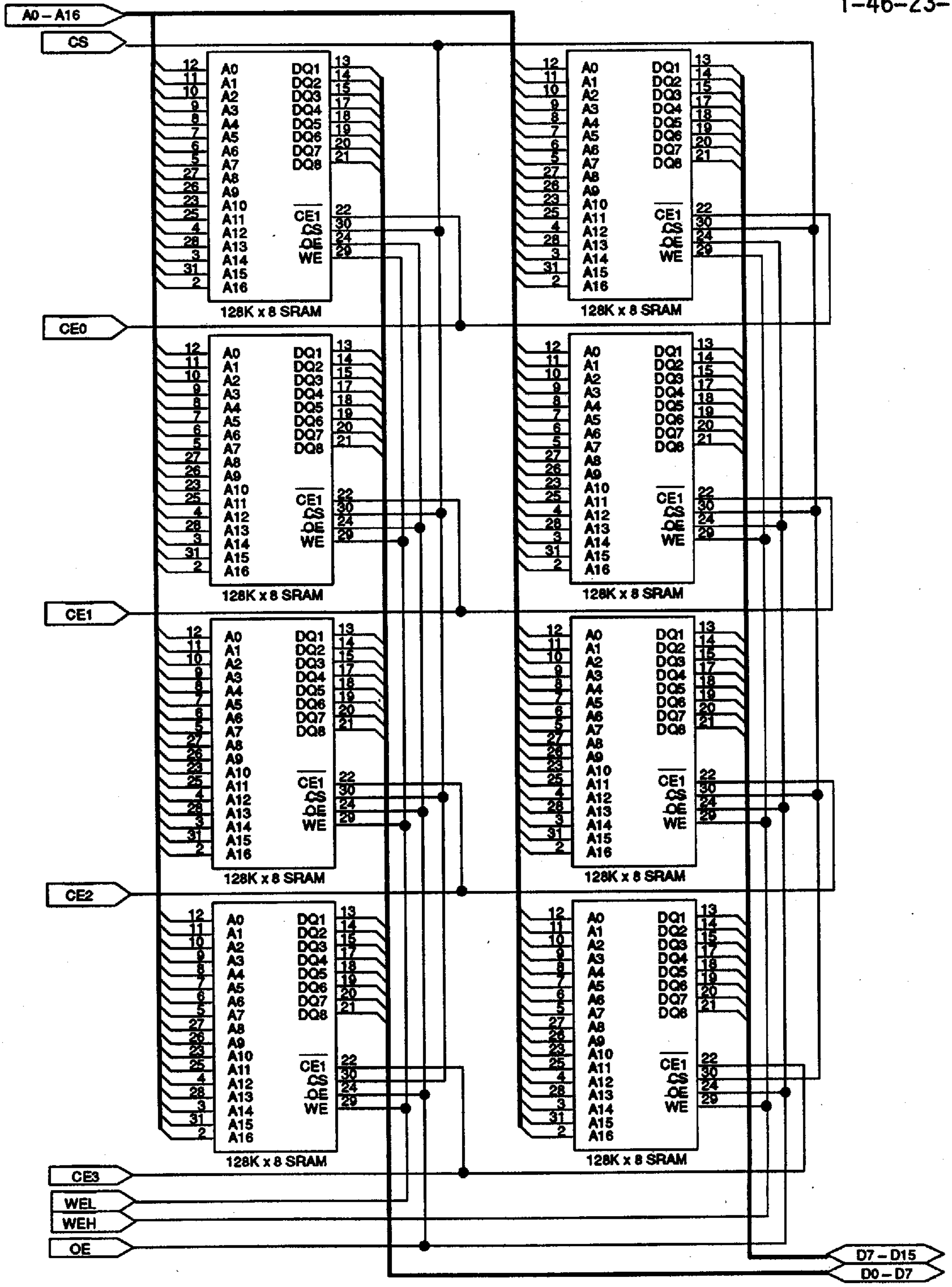

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ABSOLUTE MAXIMUM RATINGS*

Power Supply Voltage	-0.3V to +7.0V
Input, Input/Output Voltage	-0.3 to V_{CC} +0.3V
Operating Temperature	0°C to +70°C
Storage Temperature	-55°C to 125°C

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

OPERATION MODE

MODE	$\overline{CE0}$ - $\overline{CE3}$	CS	$\overline{OE}$	$\overline{WE}$	A0 – A16	DQ – DQ15	POWER
READ	L	H	L	H	STABLE	DATA OUT	I_{CC0}
WRITE	L	H	X	L	STABLE	DATA IN	I_{CC0}
DESELECT	L	H	H	H	X	HIGH-Z	I_{CC0}
STANDBY	H	X	X	X	X	HIGH-Z	I_{CCS}
STANDBY	X	L	X	X	X	HIGH-Z	I_{CCS}

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	
Input/Output Capacitance	$C_{I/O}$		5	12	pF	

RECOMMENDED DC OPERATING CONDITIONS

(t_A = 0°C to +70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
Input High Voltage	V_{IH}	2.0		V_{CC} + 0.3	V	
Input Low Voltage	V_{IL}	-0.3		0.8	V	
Data Retention Voltage	V_{DR}	2.0		5.5	V	

DC CHARACTERISTICS

(t_A = 0°C to +70°C, V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	$0V \le V_{IN} \le V_{CC}$		8	µA	
I/O Leakage Current	I_{LO}	$\overline{CE0} - \overline{CE3} = V_{IH}$, $0V \le V_{I/O} \le V_{CC}$		8	µA	
Output High Current	I_{OH}	V_{OH} = 2.4V	-1.0		mA	
Output Low Current	I_{OL}	V_{OL} = 0.4V	4.0		mA	
Standby Current	I_{CCS1}	$\overline{CE0}$ - $\overline{CE3}$ = 2.0V t_A = 25°C		8	µA	10
Standby Current	I_{CCS}	$\overline{CE0} - \overline{CE3} \ge V_{CC}$ -0.3V t_A=25°C		10	µA	10
Operating Current	I_{CC1}	$\overline{CE0} - \overline{CE3}$ = 0.8V; Cycle=200nS t_A= 25°C		60	mA	10

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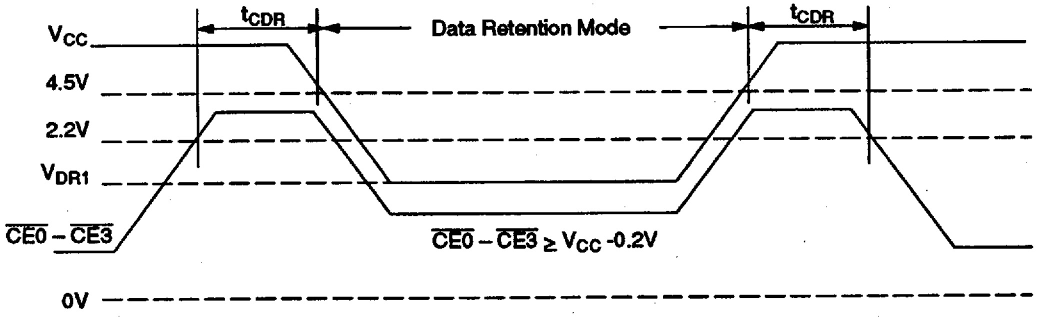
LOW VCC DATA RETENTION CHARACTERISTICS

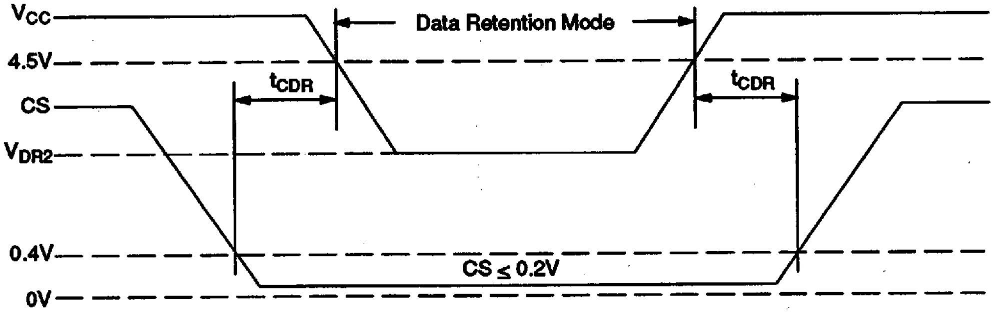
(t_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	TEST CONDITION
V_{CC} for Data Retention	V_{DR}	2.0	–	–	V	$\overline{CE0} - \overline{CE3} \geq V_{CC}$ -0.2V, CS $\geq V_{CC}$ -0.2V or 0V $\leq$ CS $\leq$ 0.2V $V_{IN} \geq$ 0V
Data Retention Current	I_{CCDR}	–	1	8	µA	V_{CC} = 3.0V, $V_{IN} \geq$ 0V $\overline{CE0} - \overline{CE3} \geq V_{CC}$ -0.2V, CS $\geq V_{CC}$ –0.2V or 0V $\leq$ CS $\leq$ 0.2V t_A=25°C
Chip Deselect to Data Retention Time	t_{CDR}	0	–	–	ns	See Retention Waveform
Operation Recovery Time	t_R	5	–	–	ms	

LOW VCC DATA RETENTION TIMING WAVEFORM (1) ($\overline{CE0} - \overline{CE3}$ Controlled) Figure 3



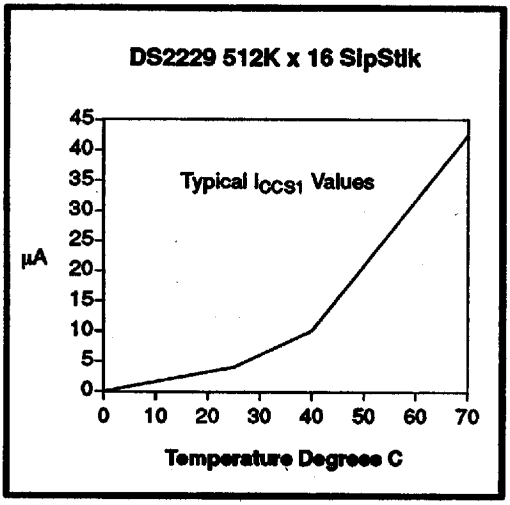
LOW VCC DATA RETENTION TIMING WAVEFORM (2) (CS Controlled) Figure 4

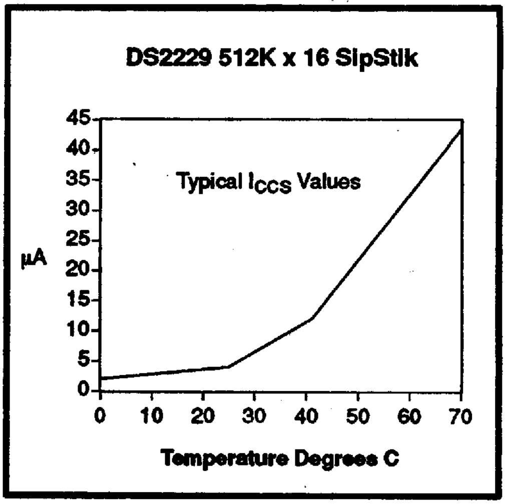


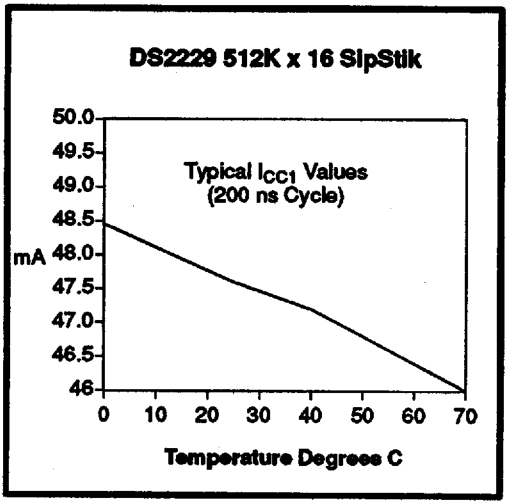
NOTES:

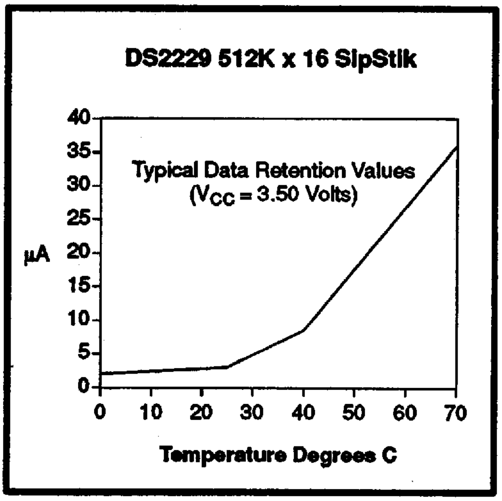
1. CS controls address buffer, $\overline{WE}$ buffer, $\overline{CE0}$ – $\overline{CE3}$ buffer and $\overline{OE}$ buffer and D_{IN} buffer. If CS controls data retention mode, V_{IN} levels (address, $\overline{WE}$, $\overline{OE}$, $\overline{CE0}$ – $\overline{CE3}$, I/O) can be in the high impedance state. If $\overline{CE0}$ – $\overline{CE3}$ controls data retention mode, CS must be CS $\geq V_{CC}$ -0.2V or 0V $\leq$ CS $\leq$ 0.2V. The other input levels (address, $\overline{WE}$, $\overline{OE}$, I/O) can be in the high impedance state.

PRODUCT CHARACTERISTICS









AC ELECTRICAL CHARACTERISTICS READ CYCLE

(0°C to 70°C; V_{CC} = 5V ± 10%)

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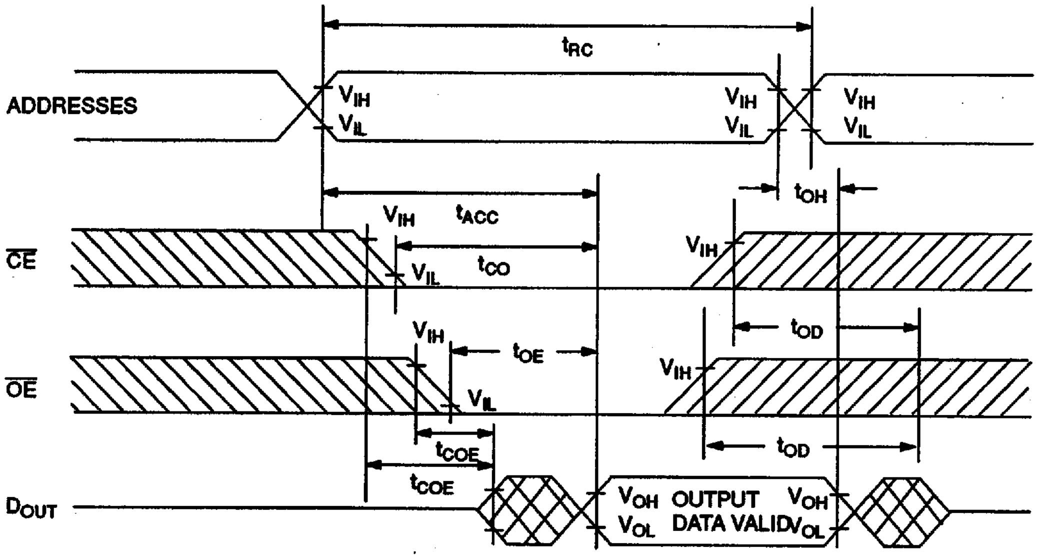
		DS2229-85		DS2229-100		DS2229-120			
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Read Cycle Time	t_{RC}	85		100		120		ns	
Access Time	t_{ACC}		85		100		120	ns	
$\overline{\text{OE}}$ to Output Valid	t_{OE}		45		50		60	ns	
$\overline{\text{CE0}}$ – $\overline{\text{CE3}}$ to Output Valid	t_{CO}		85		100		120	ns	
$\overline{\text{OE}}$ or $\overline{\text{CE0}}$ – $\overline{\text{CE3}}$ to Output In Low-Z	t_{COE}	10		10		10		ns	
Output High-Z from Deselection	t_{OD}	0	30	0	35	0	45	ns	
Output Hold from Address Change	t_{OH}	10		10		10		ns	

AC ELECTRICAL CHARACTERISTICS WRITE CYCLE

(0°C to 70°C; V_{CC} = 5V ± 10%)

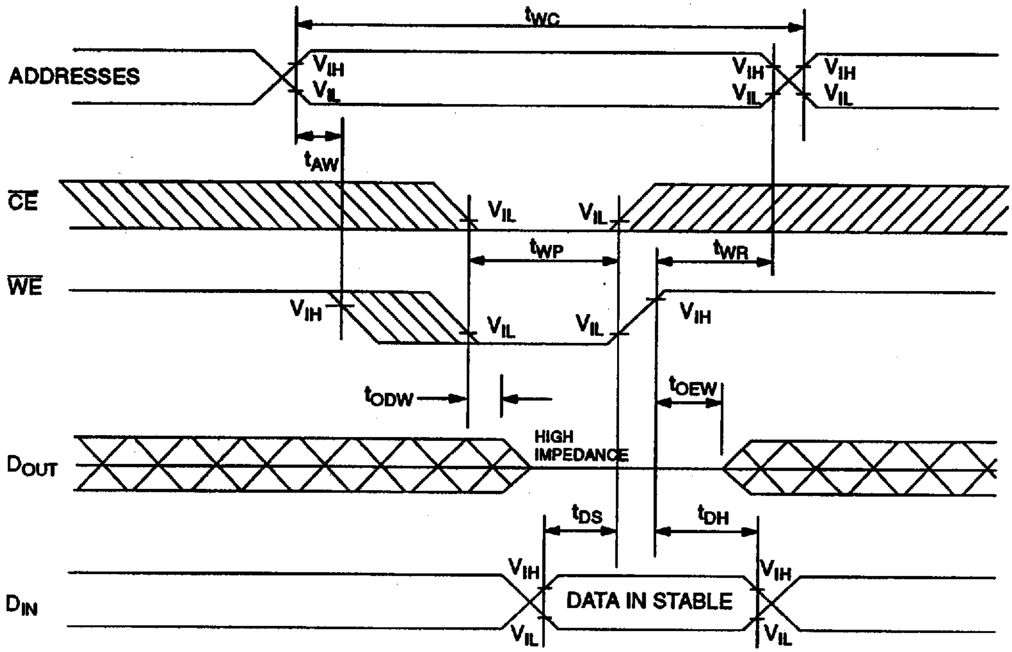
		DS2229-85		DS2229-100		DS2229-120			
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write Cycle Time	t_{WC}	85		100		120		ns	
Write Pulse Width	t_{WP}	65		75		85		ns	
Address Setup Time	t_{AW}	0		0		0		ns	
Write Recovery Time	t_{WR}	10		10		15		ns	
Output High-Z from $\overline{\text{WE}}$	t_{ODW}	0	30	0	35	0	40	ns	
Output Active from $\overline{\text{WE}}$	t_{OEW}	5		5		5		ns	
Data Setup Time	t_{DS}	35		40		45		ns	
Data Hold Time from $\overline{\text{WE}}$	t_{DH}	0		0		0		ns	

READ CYCLE Figure 5



SEE NOTE 1

WRITE CYCLE1 Figure 6



SEE NOTES 2, 6, AND 7

WRITE CYCLE 2 Figure 7

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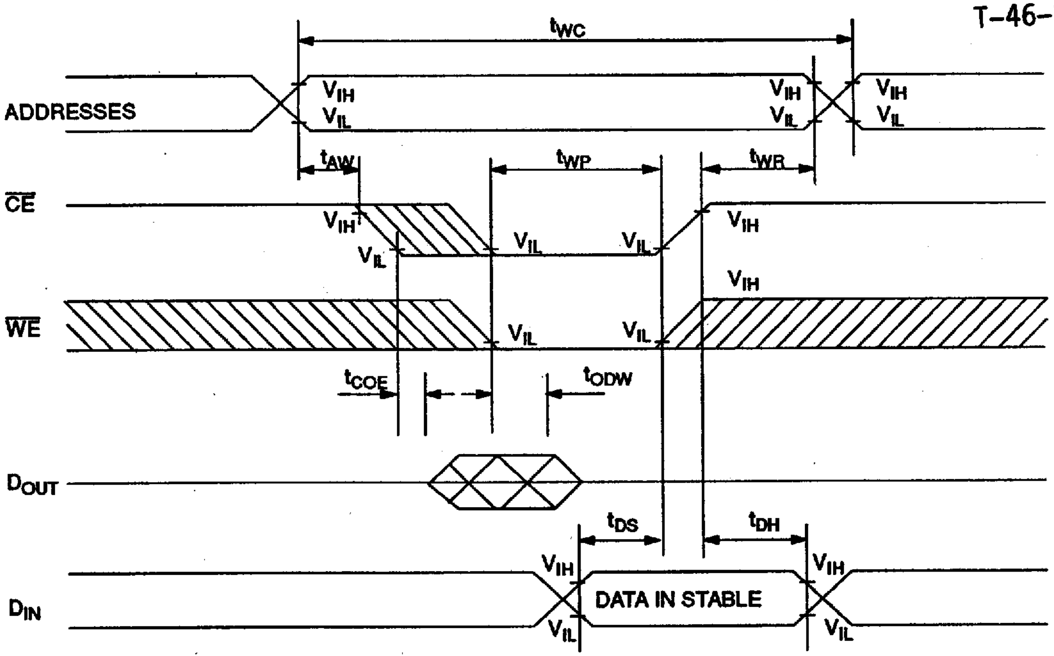


SEE NOTES 2 AND 8

NOTES

*1. A write occurs during the overlap of a low $\overline{\text{CE0}}$ – $\overline{\text{CE3}}$, a high CS, and a low $\overline{\text{WE}}$. A write begins at the latest transition among $\overline{\text{CE0}}$ – $\overline{\text{CE3}}$ going low, CS going high, and $\overline{\text{WE}}$ going low. A write ends at the earliest transition among $\overline{\text{CE0}}$ – $\overline{\text{CE3}}$ going high, CS going low and $\overline{\text{WE}}$ going high. t_{WP} is measured from the beginning of write to the end of write.

*2. t_{CW} is measured from the later of $\overline{\text{CE0}}$ – $\overline{\text{CE3}}$ going low or CS going high to the end of write.

*3. t_{AS} is measured from the address valid to the beginning of write.

*4. t_{WR} is measured from the earliest of $\overline{\text{CE0}}$ – $\overline{\text{CE3}}$ or $\overline{\text{WE}}$ going high or CS going low to the end of write cycle.

*5. During this period, I/O pins are in the output state; therefore, the input signals of the opposite phase to the outputs must not be applied.

*6. If $\overline{\text{CE0}}$ – $\overline{\text{CE3}}$ goes low simultaneously with $\overline{\text{WE}}$ going low or after $\overline{\text{WE}}$ going low, the outputs remain in a high impedance state.

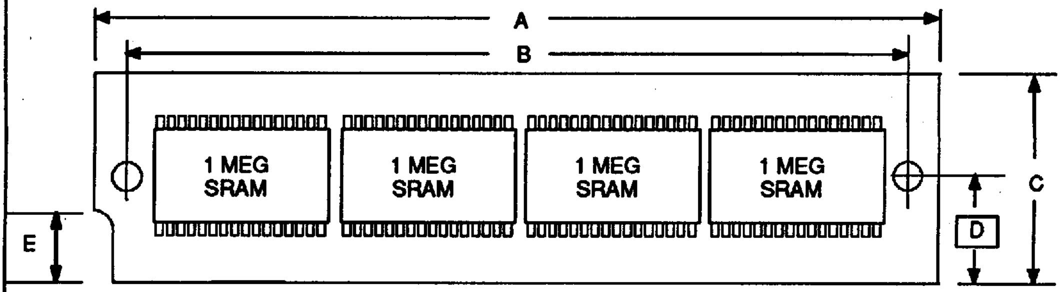
*7. If $\overline{\text{CE0}}$ – $\overline{\text{CE3}}$ is low and CS is high during this period, I/O pins are in the output state. Therefore, the input signals of the opposite phase to the outputs must not be applied to them.

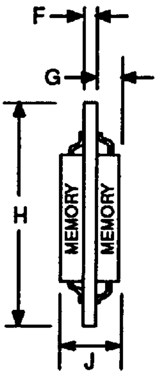
*8. This parameter is sampled and not 100% tested.

*9. This value is measured from CS going low to the end of write cycle.

*10. Only one $\overline{\text{CE}}$ active during any read or write cycle.

DS2229 80-PIN SIP STIK





DIM	MIN
A IN. MM	4.650 118.11
B IN. MM	4.384 111.35
C IN. MM	0.714 18.14
D IN. MM	0.400 10.16
E IN. MM	0.25 6.35
F IN. MM	0.540 13.72
G IN. MM	0.130 3.30
H IN. MM	0.714 18.14
J IN. MM	0.314 7.98