DATA SHEET (Preliminary)

NEC
ELECTRON DEVICE

BIPOLAR ANALOG INTEGRATED CIRCUIT
μPC660

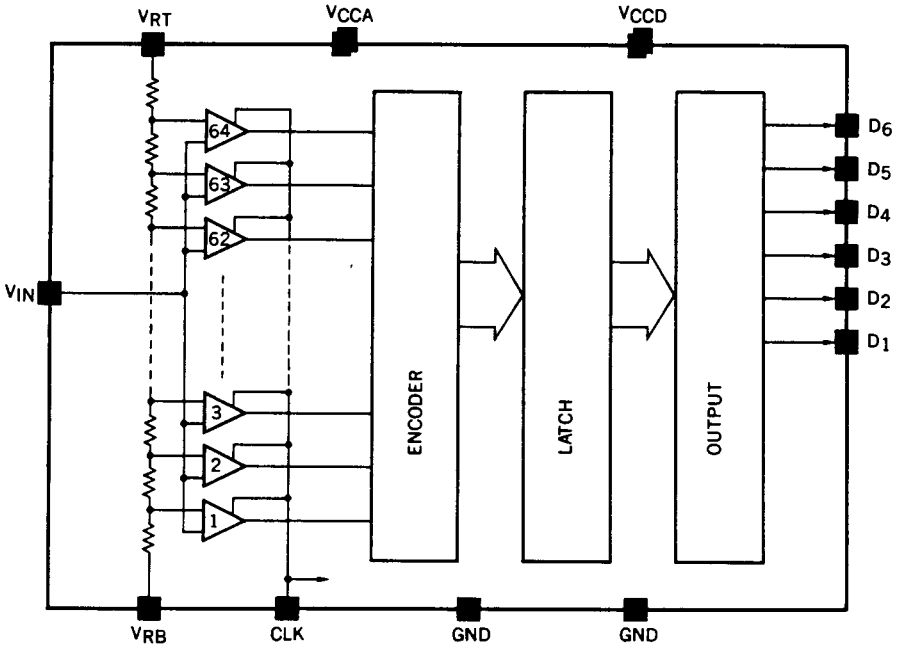
VIDEO SIGNAL PROCESSING
6-BIT A/D CONVERTER

The μPC660 is a 6-bit A/D converter for video systems. The high-speed/high-precision bipolar processing technology embodied in this IC realizes 20 Msps and ±0.5 LSB (MAX.). The low power consumption design provide wide applicability of this IC to digital systems in various fields, such as digital TV systems, or high speed facsimile system.

CHARACTERISTICS

- Resolution: 6 bits
- Conversion Rate: 20 Msps
- Non-Linearity Error: ±0.5 LSB
- +5 V Single Power Supply
- Input Voltage Range: 1.0 V_{p-p}
- Power Consumption: 165 mW (TYP.)
- Package: 16-pin DIP (300 mil), 16-pin SOP (375 mil)

BLOCK DIAGRAM

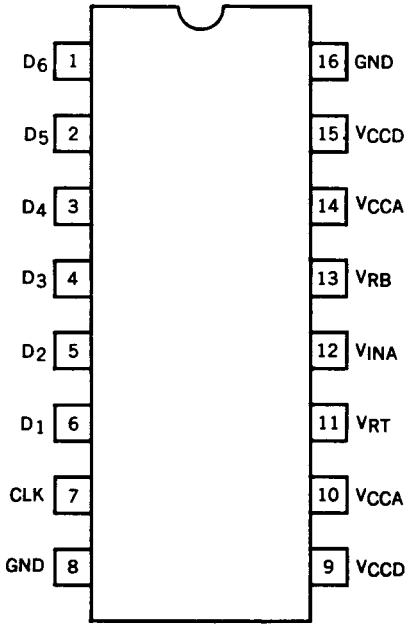


ORDER INFORMATION

Order Name	Package
μPC660C	16-pin DIP (300 mil)
μPC660G	16-pin SOP (375 mil)

The specifications of this product are subject to change without prior notice.

TERMINAL CONNECTION DIAGRAM (Top View)



PIN NUMBER	SYMBOL	PIN NAME	PIN NUMBER	SYMBOL	PIN NAME
1	D_6	Digital Output (LSB)	9	V_{CCD}	Digital Power Supply
2	D_5	Digital Output	10	V_{CCA}	Analog Power Supply
3	D_4	Digital Output	11	V_{RT}	Reference Voltage (High-level Voltage)
4	D_3	Digital Output	12	V_{INA}	Analog Input
5	D_2	Digital Output	13	V_{RB}	Reference Voltage (Low-level Voltage)
6	D_1	Digital Output (MSB)	14	V_{CCA}	Analog Power Supply
7	CLK	Clock Input	15	V_{CCD}	Digital Power Supply
8	GND	GND	16	GND	GND

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Supply Voltage	AV_{CC}, DV_{CC}	−0.3 to +5.7	V
Input Voltage on Each Pin	V_I	−0.3 to V_{CC} +0.3	V
Operating Temperature Range	T_{opt}	−20 to +75	°C
Storage Temperature Range	T_{stg}	−40 to +150	°C

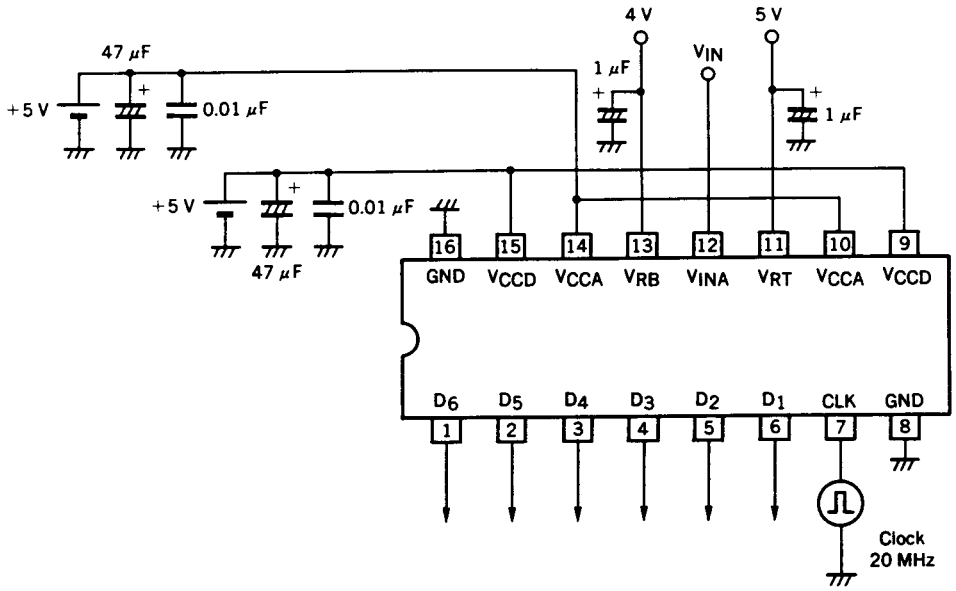
RECOMMENDED OPERATING CONDITIONS (T_a = −20 to +75 °C)

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Supply Voltage	AV_{CC},DV_{CC}	4.5	5.0	5.5	V	AGND = DGND = 0 V
Analog Input Voltage	V_{INA}	V_{RB}−0.4		V_{RT}+0.4	V	
Sampling Clock	F_{samp}	1		20	MHz	
Sampling Clock Low-level Pulse Width	t_{PWL}	20			ns	
Sampling Clock High-level Pulse Width	t_{PWH}	20			ns	
Digital Input High-level Voltage	V_{INDH}	2.7			V	
Digital Input Low-level Voltage	V_{INDL}			0.4	V	
Reference Input Voltage (Higher Voltage)	V_{RT}	4		5	V	
Reference Input Voltage (Lower Voltage)	V_{RB}	3		4	V	
Reference Voltage Differential	V_{REF}	1		2	V	

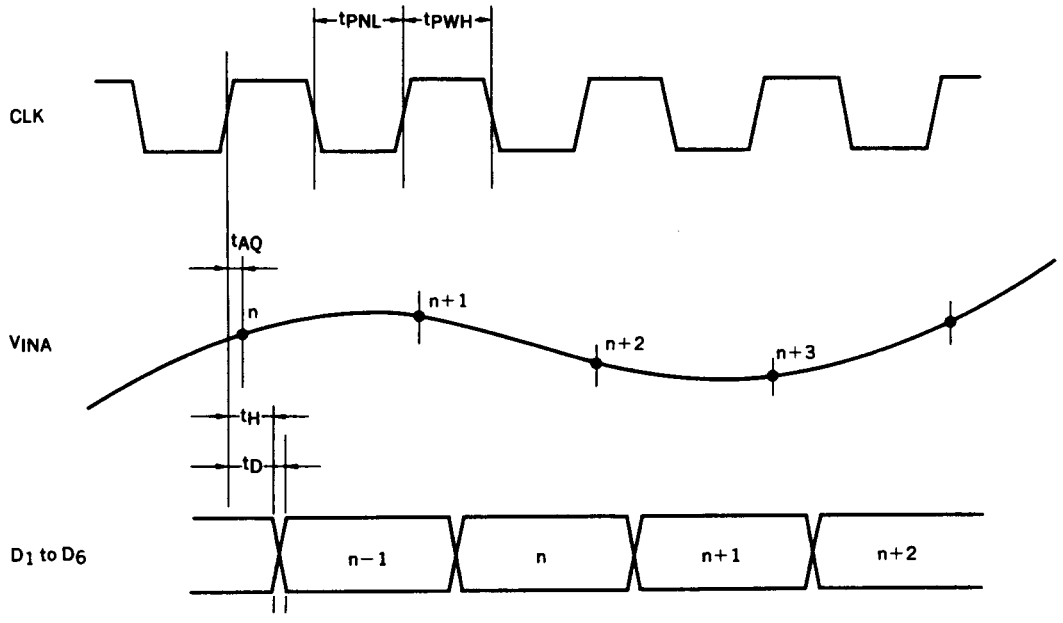
ELECTRICAL RATINGS (T_a = −20 to +75 °C, AV_{CC} = DV_{CC} = 5.0 ±0.5 V)

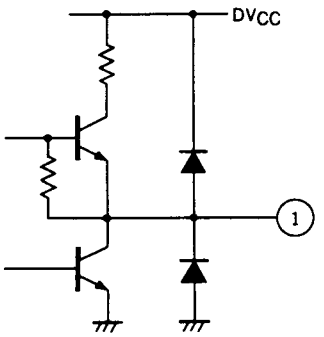
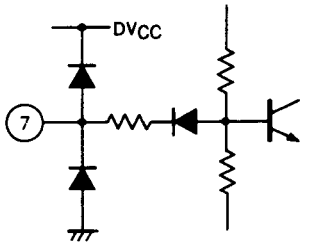
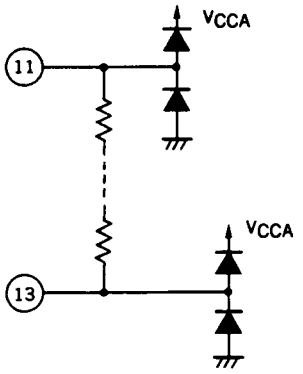
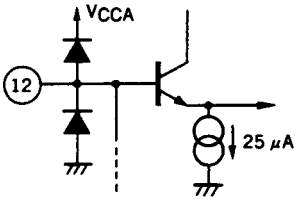
ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Power Consumption	I_{CC}	20	33	45	mA	AV_{CC} = DV_{CC} = 5.0 V, T_a = 25 °C
Nonlinearity Error	NL			±0.5	LSB	V_{CC} = 5.0 V, T_a = 0 to 60 °C, V_{INA} = 1 V_{p-p} f_{samp} = 20 MHz
Differential Linearity Error	DNL			±0.5	LSB	V_{CC} = 5.0 V, T_a = 0 to 60 °C, V_{INA} = 1 V_{p-p} f_{samp} = 20 MHz
Data Output Delay Time	t_D		12		ns	Delay time from the rise of the clock signal, D_1 to D_6
Digital Low-level Output Voltage	V_{OL}			0.4	V	I_{OL} = 1.6 mA
Digital High-level Output Voltage	V_{OH}	2.7			V	I_{OH} = −400 μA
Digital Low-level Input Current	I_{INDL}			−300	μA	V_{INDL} = 0.8 V
Digital High-level Input Current	I_{INDH}			20	μA	V_{INDH} = 2.0 V
Reference Resistance	R_{REF}		315		Ω	V_{RT} − V_{RB}
Analog Input Current	I_{INA}		15	50	μA	V_{IN} = V_{RT}
Clock Input Capacitance	C_{CLK}		2	5	pF	
Analog Input Capacitance	C_{IN}			7	pF	V_{IN} = V_{RB}

MEASUREMENT CIRCUIT

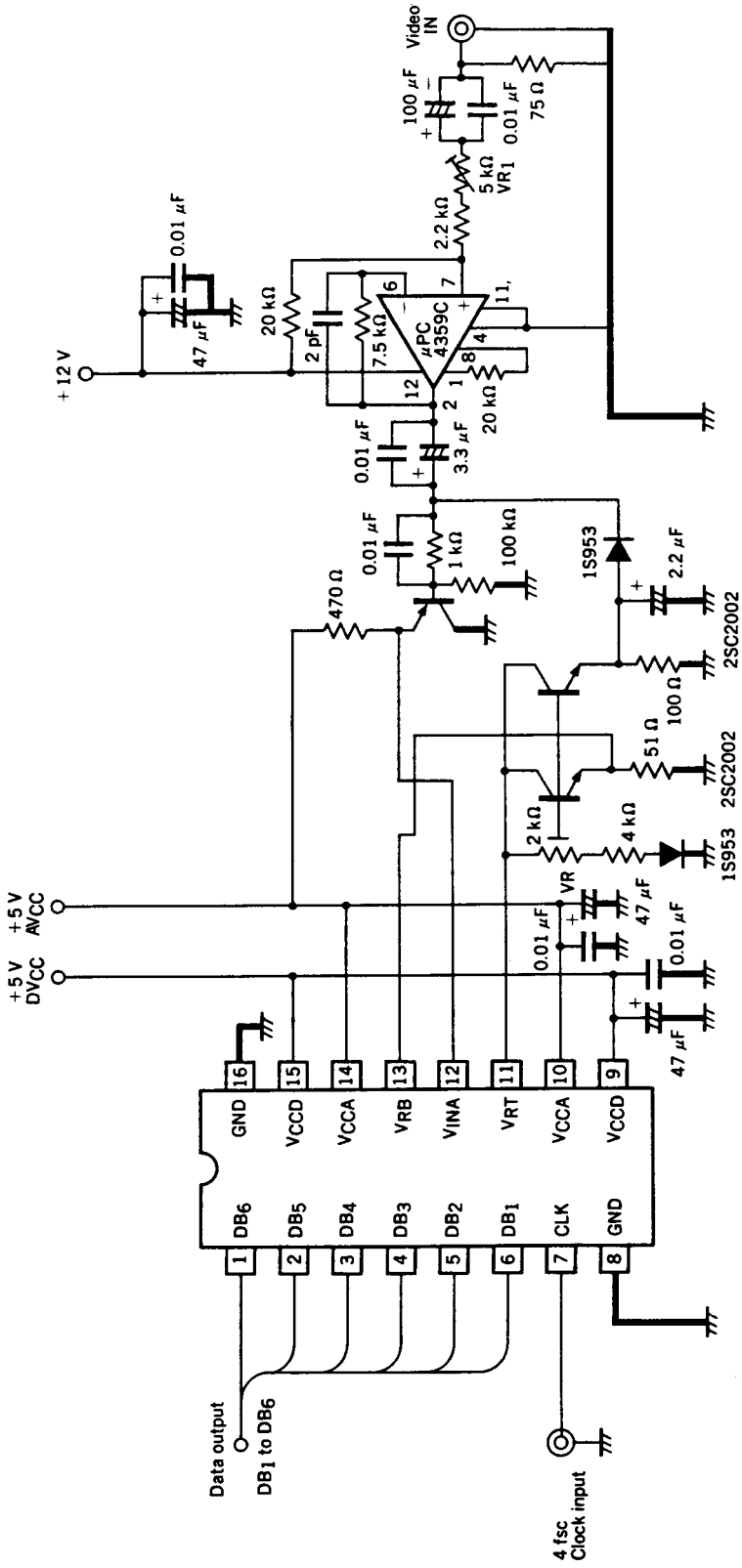


TIMING CHART



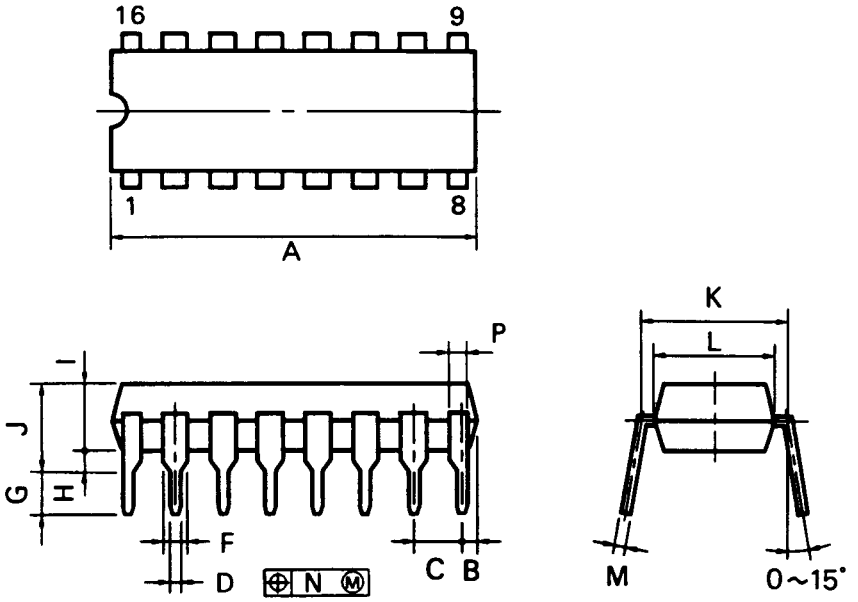
PIN NUMBER	EQUIVALENT CIRCUIT DIAGRAM	DESCRIPTION OF FUNCTIONS
1, 2, 3, 4, 5, 6		1: Digital data output (LSB) 2: Digital data output (5th) 3: Digital data output (4th) 4: Digital data output (3rd) 5: Digital data output (2nd) 6: Digital data output (1st) Digital data output terminals. The data is output one digital output delay period (t_D) after the rise of the clock. (Refer to the Timing Chart). Output at the TTL level.
7		Clock signal input terminal. Analog input is fetched and digital data is output at the rise of the signal input to this terminal.
8, 16	GND	Grounding terminal (Shared by digital and analog terminals).
9, 15		Digital V_{CC}
10, 14		Analog V_{CC}
11, 13		11: Reference voltage input terminal (higher voltage side) 13: Reference voltage input terminal (lower voltage side) V_{RT} = 5.0 V V_{RB} = 4.0 V
12		Analog signal input terminal.

APPLICATION CIRCUIT: EXAMPLE



The application circuits and circuit constants described in this document do not apply to mass production where variations in parts quality and/or temperature characteristics are considered. Note also that our company is not responsible for any patent right of any kind regarding the circuits described in this documents.

16PIN PLASTIC DIP (300 mil)



P16C-100-300B

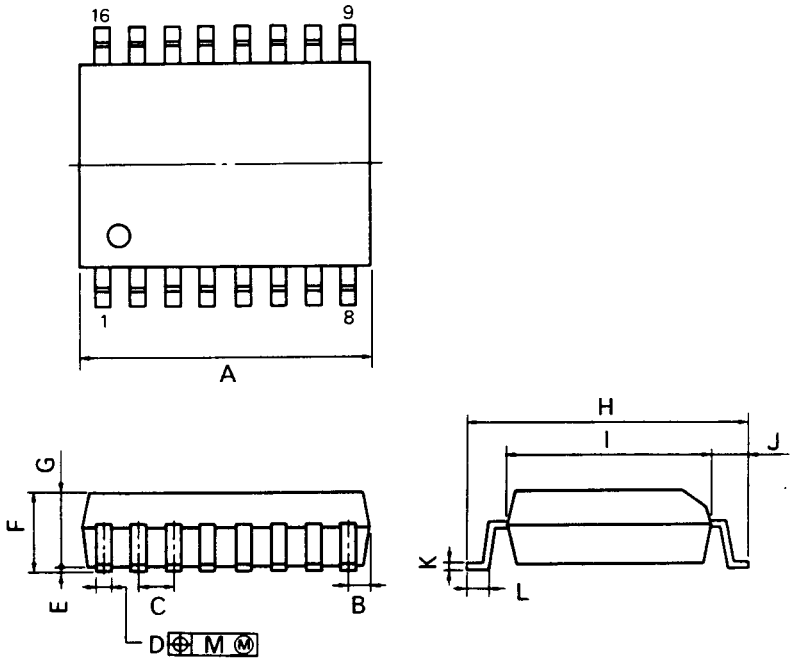
NOTES

1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	20.32 MAX.	0.800 MAX.
B	1.27 MAX.	0.050 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	$0.50^{\pm 0.10}$	$0.020^{+0.004}_{-0.005}$
F	1.1 MIN.	0.043 MIN.
G	$3.5^{\pm 0.3}$	$0.138^{\pm 0.012}$
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	7.62 (T.P.)	0.300 (T.P.)
L	6.5	0.256
M	$0.25^{+0.10}_{-0.06}$	$0.010^{+0.004}_{-0.003}$
N	0.25	0.01
P	1.1 MIN.	0.043 MIN.

16 PIN PLASTIC SOP (375 mil)



P16GM-50-375B

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	10.46 MAX.	0.412 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}_{-0.05}$	$0.016^{+0.004}_{-0.003}$
E	$0.1^{+0.2}_{-0.1}$	$0.004^{+0.008}_{-0.004}$
F	2.9 MAX.	0.115 MAX.
G	2.50	0.098
H	$10.3^{\pm 0.3}$	$0.406^{+0.012}_{-0.013}$
I	7.2	0.283
J	1.6	0.063
K	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.002}$
L	$0.8^{\pm 0.2}$	$0.031^{+0.009}_{-0.008}$
M	0.12	0.005

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