

T6L12

GATE DRIVER FOR TFT LCD PANELS

The T6L12 is a 256-channel output gate driver for TFT LCD panels. Since this device accepts external input of the panel drive voltage, allowing you to change the low-level output voltage. thus, this device can be used for various TFT LCD panel drive systems. The T6L12 offers high integration circuit due to CMOS technology.

Features

- LCD drive output pins : 256 pins
- LCD drive voltage : Max VSS + 42 V
- Data transfer method : Bidirectional shift register
- Operating temperature : -20 to 75°C
- Package : Tape carrier package (TCP)

Unit: mm

T6L12	USER AREA PITCH	
	IN	OUT
(SAM, 6FS)	0.8	0.12

Please contact Toshiba or a distributor for the latest TCP specification and product line-up.

TCP (Tape Carrier Package)

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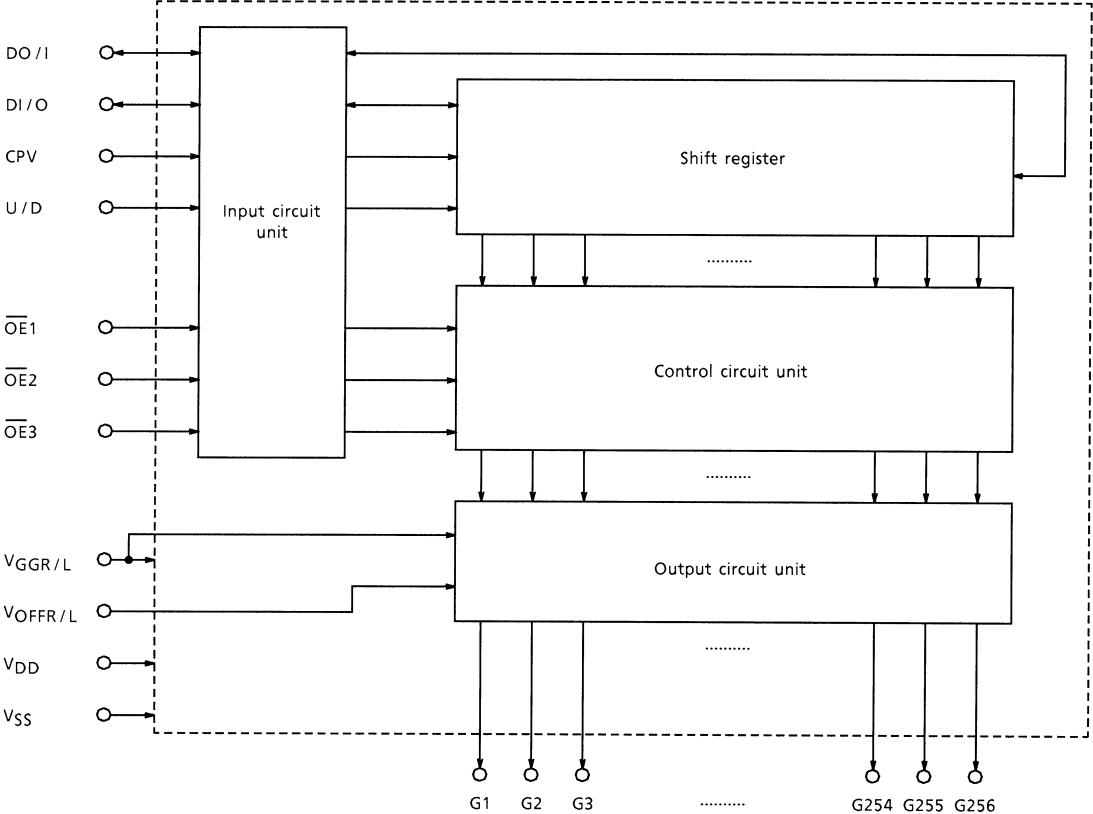
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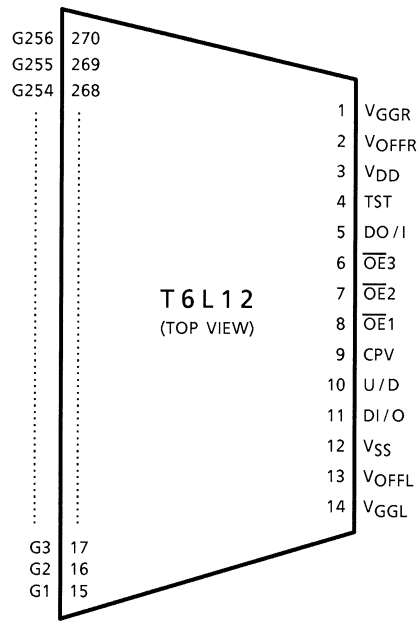
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Block Diagram



Pin Assignment



The above diagram shows the device's pin configuration only and does not necessarily correspond to the pad layout on the chip. Please contact Toshiba or our distributors for the latest TCP specification.

Pin Function

Pin Name	I / O	Function									
DI / O DO / I	I / O	<p>Vertical shift data I / O pins These pins are used to input and output shift data. These pins are switched between input and output by setting the U / D pin as shown below.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>U / D</th> <th>DI / O</th> <th>DO / I</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>INPUT</td> <td>OUTPUT</td> </tr> <tr> <td>L</td> <td>OUTPUT</td> <td>INPUT</td> </tr> </tbody> </table> <p>When set for input This pin is used to feed data into the shift registers at the first stage of the LCD driver. The data is latched into the shift registers at the rising edge of CPV.</p> <p>When set for output When two or more T6L12s are cascaded, this pin outputs the data to be fed into the next stage. This data changes state synchronously with the falling edge of CPV.</p>	U / D	DI / O	DO / I	H	INPUT	OUTPUT	L	OUTPUT	INPUT
U / D	DI / O	DO / I									
H	INPUT	OUTPUT									
L	OUTPUT	INPUT									
U / D	Input	<p>Transfer direction select pin This pin specifies the direction in which data is transferred through the shift registers. The shift register data is shifted synchronously with each rising edge of CPV as follows: When U / D is high, data is shifted in the direction G1 → G2 → G3 → G4 → ... → G256 When U / D is low, the direction is reversed to give G256 → G255 → G254 → ... → G1 The voltage applied to this pin must be a DC-level voltage that is either high (V_{DD}) or low (V_{SS}).</p>									
CPV	Input	<p>Vertical shift clock This is the shift clock for the shift registers. Data is shifted through the shift registers synchronously with the rising edge of CPV.</p>									
$\overline{\text{OE}}$ 1 to 3	Input	<p>Output enable pins These signals control the data appearing at the LCD panel drive pins (G1 through G256). The V_{OFFR} / L voltage is output when $\overline{\text{OE}}$ 1 to 3 are high; normal shift data is output when $\overline{\text{OE}}$ 1 to 3 are low.</p>									
V _{OFFR} V _{OFFL}	Input	<p>Analog input pins These pins accept as their input the OFF level at the LCD panel drive pins (G1 through G256). Make sure that the same voltage is supplied to V_{OFFR} and V_{OFFL}.</p>									
G1 to 256	Output	<p>LCD panel drive pins These pins output the shift register data or the voltage applied to V_{GGR} / L or V_{OFFR} / L depending on the control signals $\overline{\text{OE}}$ 1 to 3.</p>									
V _{GGR} V _{GGL}	—	<p>Power supply for LCD drive Make sure that the same voltage is supplied to V_{GGR} and V_{GGL}.</p>									
V _{DD}	—	<p>Power supply for the internal logic</p>									
V _{SS}	—	<p>Power supply for LCD drive and internal logic</p>									

Device Operation (see timing diagram)

(1) Shift data transfer method

U / D	Shift Data		Data Transfer Method
	IINPUT	OUTPUT	
H	DI / O	DO / I	G1 → G2 → G3 → G4 → ... → G256
L	DO / I	DI / O	G256 → G255 → G254 → ... → G1

The input data is latched into the internal register synchronously with the rising edge of the shift clock CPV. At the same time that the data is shifted to the next register at the next rise of CPV, new vertical shift data is latched into.

In the output operation, the data in the last shift register (G256 or G1) is output synchronously with the falling edge of CPV. (The output high voltage is the V_{DD} level; the output low voltage is the V_{SS} level.)

(2) LCD panel drive outputs

The LCD panel drive outputs are controlled by \overline{OE} 1 to 3 as shown below.

Output Enable Pin	LCD Panel Drive Outputs	
	Lcd Panel Drive Pins Controlled by \overline{OE}	Output
$\overline{OE} 1 = H$	G1, G4, G7, ... G250, G253, G256	V _{OFFR} / L
$\overline{OE} 2 = H$	G2, G5, G8, ... G251, G254	
$\overline{OE} 3 = H$	G3, G6, G9, ... G252, G255	
$\overline{OE} 1 = L$	G1, G4, G7, ... G250, G253, G256	Normal data output
$\overline{OE} 2 = L$	G2, G5, G8, ... G251, G254	
$\overline{OE} 3 = L$	G3, G6, G9, ... G252, G255	

(3) Voltage setting

The VOFFR / L level, which sets the LCD panel drive's output low level, can take on any value between VSS to VSS +15 V.

(Example 1) Negative voltage output

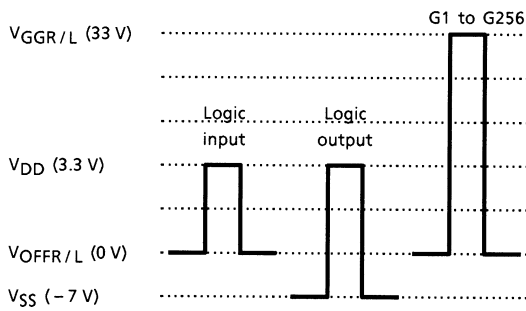
Logic input : High = 3.3 V or low = 0 V amplitude
 Supply voltage : $V_{GGR} = V_{GGL} = 33\text{ V}$
 $V_{DD} = 3.3\text{ V}$
 $V_{OFFR} = V_{OFFL} = 0\text{ V}$
 $V_{SS} = -7\text{ V}$
 LCD panel drive output : High level = V_{GGR} / L (33 V)
 Low level = V_{OFFR} / L (0 V)

(Example 2) Positive voltage output

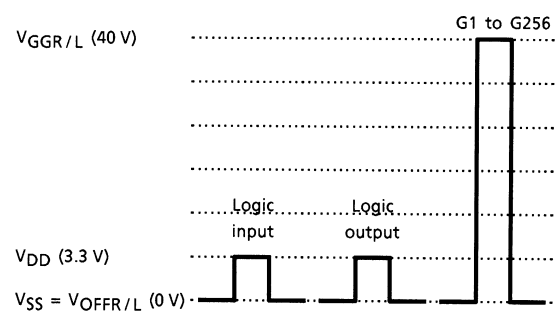
Logic input : High = 3.3 V or low = 0 V amplitude
 Supply voltage : $V_{GGR} = V_{GGL} = 40\text{ V}$
 $V_{DD} = 3.3\text{ V}$
 $V_{OFFR} = V_{OFFL} = V_{SS} = 0\text{ V}$
 LCD panel drive output : High level = V_{GGR} / L (40 V)
 Low level = V_{OFFR} / L (0 V)

Note: The logic input here means input pins DI / O, DO / I, CPV and \overline{OE} 1 to 3.

Make sure that the voltage applied to the U / D pin is a high (= V_{DD}) or low (= V_{SS}) DC-level voltage.



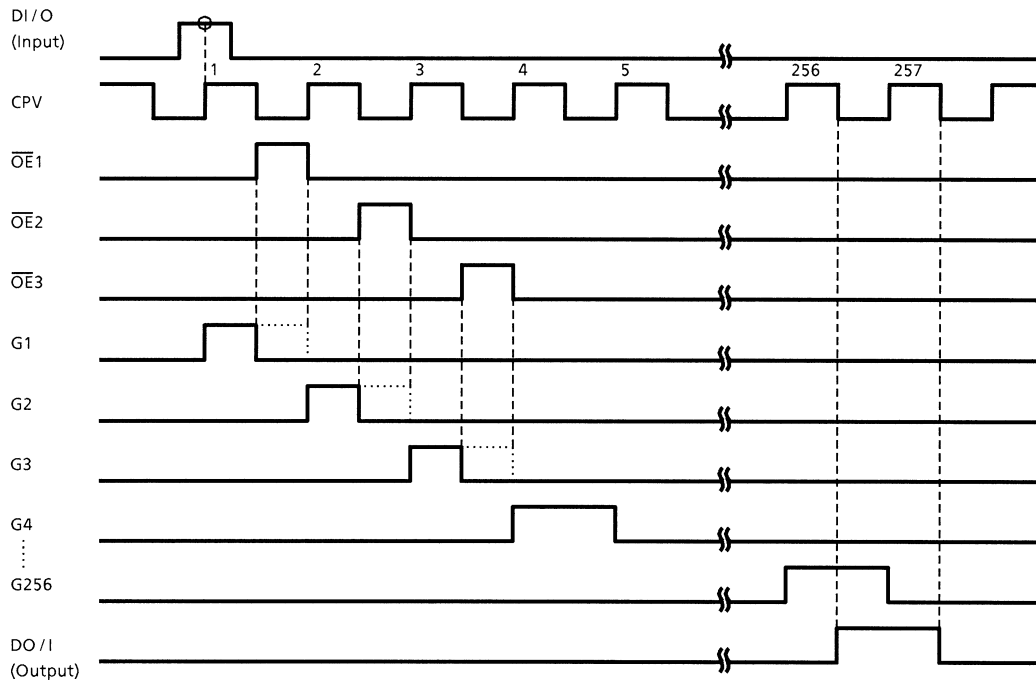
(Example 1)



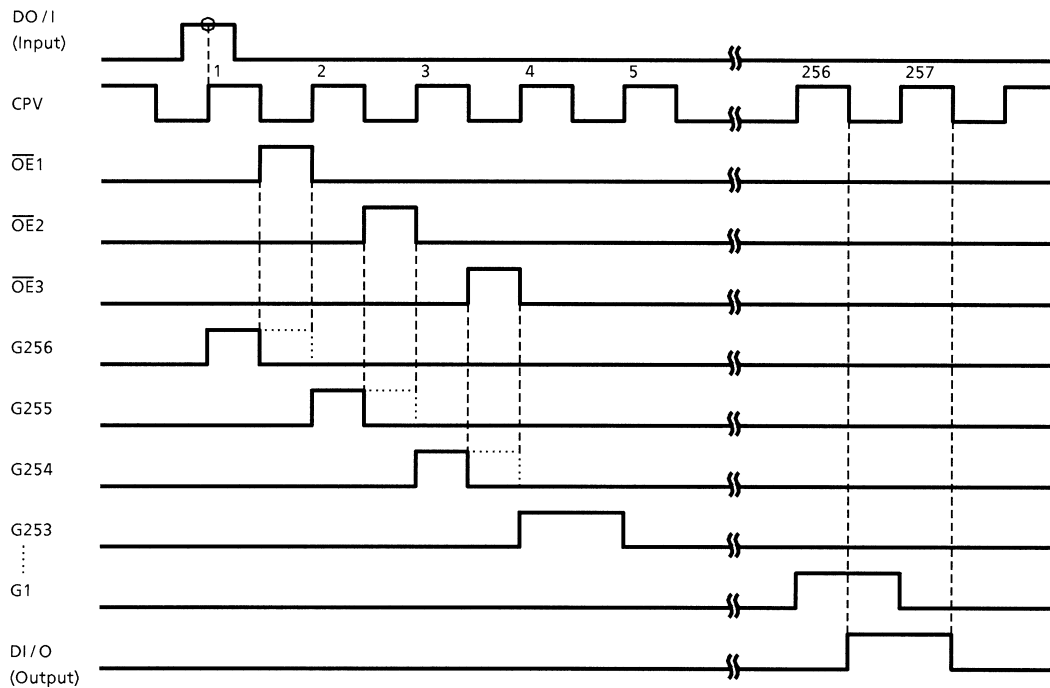
(Example 2)

Timing Diagram

- UP mode (U / D = high)



- DOWN mode (U / D = low)



Absolute Maximum Ratings ($V_{SS} = 0\text{ V}$)

Parameter	Symbol	Rating	Unit
Supply Voltage	$V_{GGR/L}$	-0.3 to 45.0	V
Supply Voltage	V_{DD}	-0.3 to 22.0	V
Input Voltage	V_{IN}	-0.3 to $V_{DD} + 0.3$	V
Analog Input Voltage	$V_{OFFR/L}$	-0.3 to $V_{GG} + 0.3$	V
Storage Temperature	T_{stg}	-55 to 125	°C

Recommended Operating Conditions ($V_{SS} = 0\text{ V}$)

Parameter	Symbol	Rating	Unit
Supply Voltage	$V_{GGR/L}$	25.0 to 42.0	V
Supply Voltage	V_{DD}	3.0 to 16.0	V
Operating Temperature	T_{op}	-20 to 75	°C
Operating Frequency	f_{CPV}	DC to 100	kHz
Output Load Capacitance	C_L	300 (max)	pF / pin
Analog Input Voltage	$V_{OFFR/L}$	0 to 15.0	V

Electrical Characteristics

DC Characteristics (Referenced to $V_{GGR} = V_{GGL} = 25$ to 42 V , $V_{DD} = 3.0$ to 16.0 V ,
 $V_{SS} = 0\text{ V}$, $T_a = -20$ to 75°C Unless Otherwise Noted)

Parameter		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit	Relevant Pin
Input Voltage	Low Level	V_{IL}	—	—	V_{SS}	—	$V_{DD} - 2.5$	V	(Note)
	High Level	V_{IH}	—	—	$V_{DD} - 0.5$	—	V_{DD}		
Output Voltage	Low Level	V_{OL}	—	$I_{OL} = 40\ \mu\text{A}$	V_{SS}	—	$V_{SS} + 0.3$	V	DI / O, DO / I
	High Level	V_{OH}	—	$I_{OH} = -40\ \mu\text{A}$	$V_{DD} - 0.3$	—	V_{DD}		
Output Resistance	Low Level	R_{OL}	—	$V_{OUT} = V_{OFFR/L} + 0.5\text{ V}$	—	—	1500	Ω	G1 to G256
	High Level	R_{OH}	—	$V_{OUT} = V_{GGR/L} - 0.5\text{ V}$					
Current Consumption		I_{GG}	—	$V_{GGR/L} = 42\text{ V}$	—	—	500	μA	$V_{GGR/L}$
Current Consumption		I_{DD}	—	$f_{CPV} = 100\text{ kHz}$	—	—	1.0	mA	V_{DD}

Note: These input pins include DI / O, DO / I, CPV and \overline{OE} 1 to 3.

AC Characteristics (Referenced to $V_{GGR} = V_{GGL} = 25$ to 42 V, $V_{DD} = 3.0$ to 16.0 V, $V_{SS} = 0$ V, $T_a = -20$ to 75°C Unless Otherwise Noted)

Parameter	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Clock Period	tCPV	—	—	10	—	—	μs
CPV Pulse Width (H)	tCPVH	—	—	4	—	—	μs
CPV Pulse Width (L)	tCPVL	—	—	4	—	—	μs
Data Set-up Time	tsDI	—	—	1	—	—	μs
Data Hold Time	thDI	—	—	1	—	—	μs
OE Enable Time	twOE	—	—	1	—	—	μs
Output Delay Time (1)	tpdDO	—	$C_L = 50$ pF	—	—	1	μs
Output Delay Time (2)	tpdG	—	$C_L = 300$ pF	—	—	1	μs
Output Delay Time (3)	tpdOE	—	$C_L = 300$ pF	—	—	1	μs

