

## Description

The μPD28C64 is a 65,536-bit electrically erasable and programmable read-only memory (EEPROM) organized as 8,192 x 8 bits and fabricated with an advanced CMOS process for high performance and low power consumption.

Operating from a single +5-volt power supply, the μPD28C64 provides DATA polling function to indicate the precise end of write cycles. Additional features include chip erase, auto erase and programming, and 32-byte page write cycles.

The μPD28C64 is available in standard 28-pin plastic DIP.

## Features

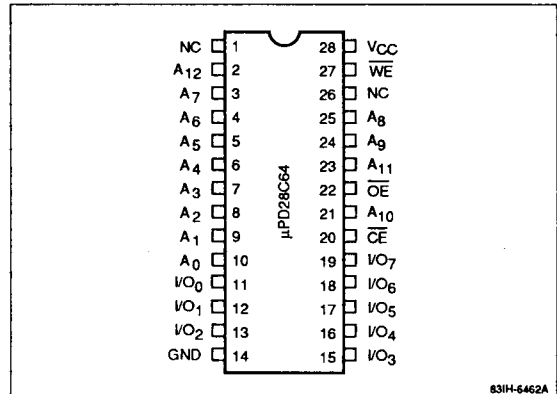
- 8,192 x 8-bit organization
- Single +5-volt power supply
- Chip erase cycles
- Auto erase and programming at 10 ms max
- 32-byte page programming cycles
- DATA polling verification
- Low power dissipation
  - 50 mA max (active)
  - 100 μA max (standby)
- Endurance: 100,000 erase/write cycles per byte
- Silicon signature
- TTL-compatible inputs and outputs
- Three-state outputs
- Advanced CMOS technology
- 28-pin plastic DIP packaging

## Ordering Information

Part Number	Access Time (max)	Package
μPD28C64C-20	200 ns	28-pin plastic DIP
C-25	250 ns	

## Pin Configuration

### 28-Pin Plastic DIP



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## Pin Identification

Symbol	Function
A <sub>0</sub> - A <sub>12</sub>	Address inputs
I/O <sub>0</sub> - I/O <sub>7</sub>	Data inputs and outputs
CE	Chip enable
OE	Output enable
WE	Write enable
GND	Ground
V <sub>CC</sub>	+5-volt power supply
NC	No connection

**Absolute Maximum Ratings**

Supply voltage, $V_{CC}$	-0.6 to +7.0 V
Input voltage, $V_{IN}$	-0.6 to +7.0 V
Input voltage, $A_9$	-0.6 to +13.5 V
$\overline{OE}$	-0.6 to +16.5 V
Output voltage, $V_{OUT}$	-0.6 to +7.0 V
Operating temperature, $T_{OPR}$	-10 to +85°C
Storage temperature, $T_{STG}$	-65 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

**Recommended Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{CC}$	4.5	5.0	5.5	V
Input voltage, high	$V_{IH}$	2.0		$V_{CC} + 0.3$	V
Input voltage, low	$V_{IL}$	-0.3		0.8	V
Operating temperature	$T_A$	0		70	°C

**Capacitance**

$T_A = 25^\circ\text{C}$ ;  $f = 1 \text{ MHz}$ ;  $V_{IN}$  and  $V_{OUT} = 0 \text{ V}$

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	$C_I$			12	pF
Output capacitance	$C_O$			10	pF

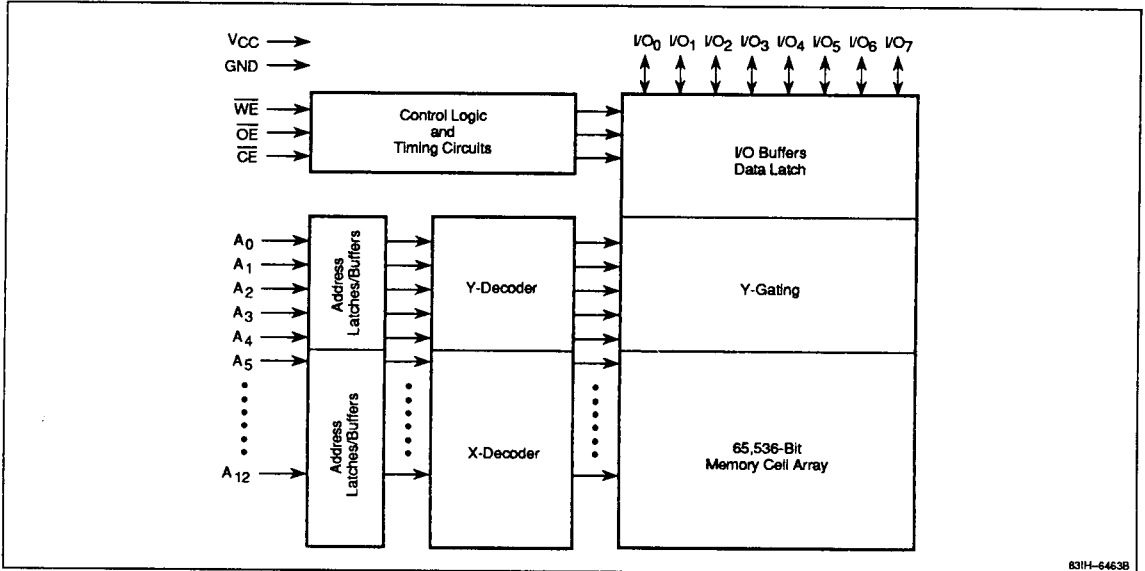
**Truth Table**

Function	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Input/Output	$I_{CC}$
Read	$V_{IL}$	$V_{IL}$	$V_{IH}$	$D_{OUT}$	Active
Standby and write inhibit	$V_{IH}$	X	X	High-Z	Standby
Write	$V_{IL}$	$V_{IH}$	$V_{IL}$	$D_{IN}$	Active
Chip erase	$V_{IL}$	$V_{IHH}$	$V_{IL}$	$D_{IN} = V_{IH}$	Active
Write inhibit	X	$V_{IL}$	X	—	—
	X	X	$V_{IH}$	—	—

**Notes:**

- (1) X can be either  $V_{IL}$  or  $V_{IH}$ .
- (2)  $V_{IHH} = +15 \text{ V} \pm 0.5$ .

**Block Diagram**



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### DC Characteristics

$T_A = 0$  to  $+70^\circ\text{C}$ ;  $V_{CC} = +5.0\text{V} \pm 10\%$

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage, high	$V_{OH1}$	2.4			V	$I_{OH} = -400\ \mu\text{A}$
	$V_{OH2}$	$V_{CC} - 0.7$			V	$I_{OH} = -100\ \mu\text{A}$
Output voltage, low	$V_{OL}$			0.45	V	$I_{OL} = 2.1\ \text{mA}$
Output leakage current	$I_{LO}$			10	$\mu\text{A}$	$V_{OUT} = 0\text{V to } V_{CC}$ ; $\overline{CE}$ or $\overline{OE} = V_{IH}$
Input leakage current	$I_{LI}$			10	$\mu\text{A}$	$V_{IN} = 0\text{V to } V_{CC}$
$V_{CC}$ current (active)	$I_{CCA1}$			20	mA	$\overline{CE} = V_{IL}$ ; $\overline{OE} = V_{IH}$
	$I_{CCA2}$			50	mA	$f = 5\ \text{MHz}$ ; $I_{OUT} = 0\ \text{mA}$
$V_{CC}$ current (standby)	$I_{CCS1}$			1	mA	$\overline{CE} = V_{IH}$
	$I_{CCS2}$			100	$\mu\text{A}$	$\overline{CE} = V_{CC}$ ; $V_{IN} = 0\text{V to } V_{CC}$

### AC Characteristics

$T_A = 0$  to  $+70^\circ\text{C}$ ;  $V_{CC} = +5.0\text{V} \pm 10\%$

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Parameter	Symbol	μPD28C64-20		μPD28C64-25		Unit	Test Conditions
		Min	Max	Min	Max		
<b>Read Operation</b>							
Address to output delay	$t_{ACC}$		200		250	ns	$\overline{CE} = \overline{OE} = V_{IL}$
$\overline{CE}$ to output delay	$t_{CE}$		200		250	ns	$\overline{OE} = V_{IL}$
$\overline{OE}$ or $\overline{CE}$ high to output float	$t_{DF}$	0	60	0	80	ns	$\overline{CE} = V_{IL}$ or $\overline{OE} = V_{IL}$
$\overline{OE}$ to output delay	$t_{OE}$	10	75	10	100	ns	$\overline{CE} = V_{IL}$
Output hold from address, $\overline{OE}$ or $\overline{CE}$ , whichever transition occurs first	$t_{OH}$	0		0		ns	$\overline{CE} = \overline{OE} = V_{IL}$

### AC Characteristics (cont)

$T_A = 0$  to  $+70^\circ\text{C}$ ;  $V_{CC} = +5.0\text{V} \pm 10\%$

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
<b>Write Operation</b>						
Address hold time	$t_{AH}$	200			ns	
Address setup time	$t_{AS}$	10			ns	
Write hold time	$t_{CH}$	0			ns	
Write setup time	$t_{CS}$	0			ns	
$\overline{CE}$ pulse width	$t_{CW}$	150			ns	
$\overline{OE}$ high hold time	$t_{OEH}$	10			ns	
$\overline{OE}$ high setup time	$t_{OES}$	10			ns	
Write cycle time	$t_{WC}$	10			ms	
$\overline{WE}$ pulse width	$t_{WP}$	150			ns	
$\overline{WE}$ high hold time	$t_{WPH}$	50			ns	

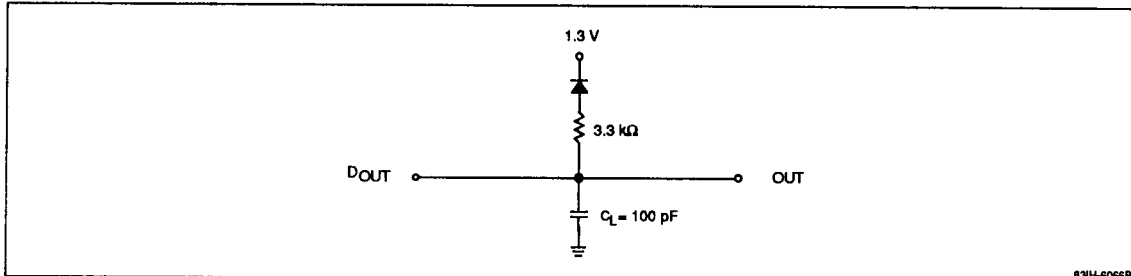
**AC Characteristics (cont)**

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
<b>Write Operation</b>						
Byte load cycle time	$t_{BLC}$	3		100	$\mu s$	
Data hold time	$t_{DH}$	20			ns	
Data setup time	$t_{DS}$	100			ns	
Data valid time	$t_{DV}$			300	ns	
<b>Chip Erase Operation</b>						
$\overline{OE}$ hold time	$t_{CEH}$	$t_{CH} + 3$			$\mu s$	
$\overline{CE}$ hold time	$t_{CH}$	5			$\mu s$	
$\overline{CE}$ setup time	$t_{CS}$	500			ns	
Data hold time	$t_{DH}$	100			ns	
Data setup time	$t_{DS}$	500			ns	
$\overline{OE}$ setup time	$t_{OES}$	500			ns	
$\overline{WE}$ pulse width	$t_{WP}$	10			ms	

**Notes:**

- (1) See figure 1 for the output load. Input rise and fall times  $\leq 20$  ns; input pulse levels = 0.45 and 2.4 V; timing measurement reference levels = 0.8 and 2.0 V for both inputs and outputs.

**Figure 1. Output Load**



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## Read Cycles

Both  $\overline{CE}$  and  $\overline{OE}$  must both be at  $V_{IL}$  in order to read stored data. While the device is executing read cycles, bringing either of these inputs to  $V_{IH}$  will place the outputs in a state of high impedance. This two-line output control allows bus contention to be eliminated in the system application.

## Byte Write Cycles

Low levels on  $\overline{CE}$  and  $\overline{WE}$  and a high level on  $\overline{OE}$  place the μPD28C64 in write operation. Write address inputs are latched by the falling edge of either  $\overline{CE}$  or  $\overline{WE}$ , whichever occurs later. The data inputs are latched by the rising edge of either  $\overline{CE}$  or  $\overline{WE}$ , whichever occurs earlier. Once byte write operation has begun, the internal circuits assume all timing control. The byte being addressed is automatically erased and then programmed. The operation completes within the write cycle time ( $t_{WC}$ ) of 10 ms.

## Page Write Cycle

This option allows the μPD28C64 to be completely programmed in a much shorter time than is required using byte write cycles. The loading of up to 32 bytes of data before internal write cycles program all of these bytes simultaneously allows the μPD28C64 to be completely written in a maximum of 2.6 seconds. The page address is specified by the inputs  $A_5$  through  $A_{12}$ ; once set, this address cannot be changed during a page write cycle. Within the page, address inputs  $A_0$  through  $A_4$  can be used sequentially or in random order to specify individual bytes.

The beginning of a page write cycle is the same as a  $\overline{WE}$ -controlled byte write cycle. If the next falling edge of  $\overline{WE}$  occurs within a byte load cycle time of 100 μs, the internal byte load register will be loaded with another byte of input data. This cycle can be repeated to load a

maximum of 32 bytes of data. At any point in the sequence, if  $\overline{WE}$  does not have a new falling edge within the byte load cycle time of 100 μs, byte load operation will terminate and automatic erasing and programming operations will begin.

## Chip Erase Cycles

All bytes of the μPD28C64 can be erased simultaneously by making  $\overline{CE}$  and  $\overline{WE}$  fall to  $V_{IL}$  after  $\overline{OE}$  has been increased to  $V_{IH}$  (15 V ± 0.5). The address inputs are "don't care," but the data inputs must all be driven to  $V_{IH}$  before the chip erase cycle begins.

## DATA Polling Feature

This feature supports system software by indicating the precise end of byte write and page write cycles. DATA polling can be used to reduce total programming time of the μPD28C64 to a minimum value, which varies with the system environment.

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While internal automatic write operation is in progress, any attempt to read data at the last externally supplied address location will result in inverted data on pin I/O<sub>7</sub> (for example, if write data = 1xxx xxxx, then read data = 0xxx xxxx). Once the write cycle is complete, a read cycle will result in true data being output on I/O<sub>7</sub>.

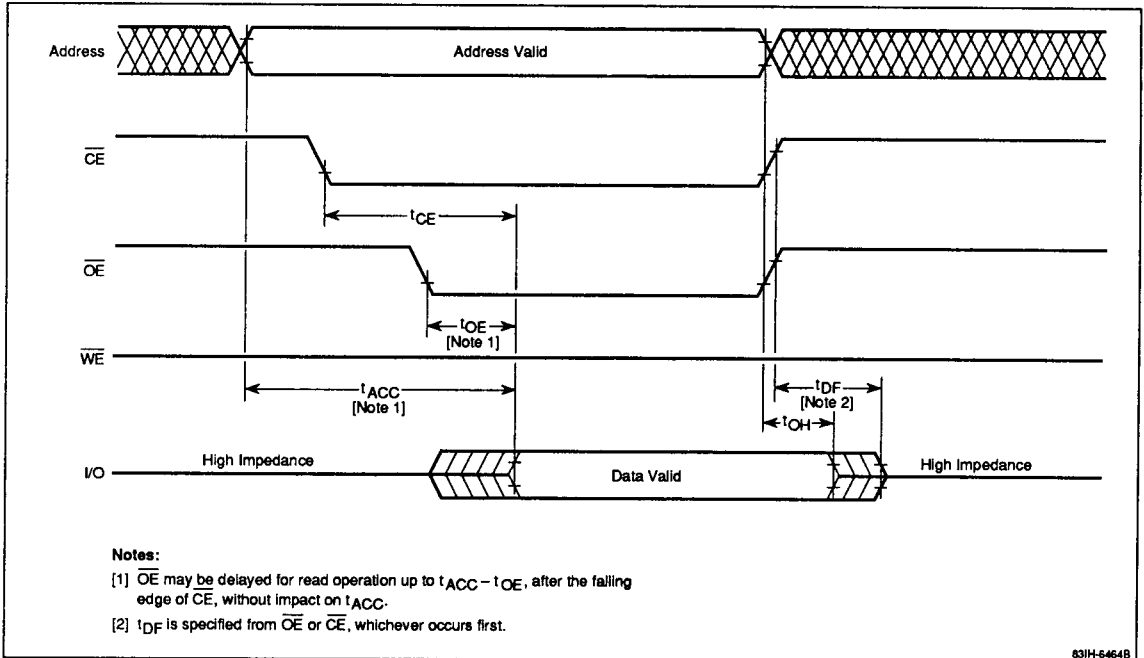
## Write Protection Features

The μPD28C64 provides three features to prevent invalid write cycles.

- Noise immunity, where write operation is inhibited when the  $\overline{WE}$  pulse width is 20 ns or less.
- Supply voltage level detection, where write operation is inhibited when  $V_{CC}$  is 2.5 V or less.
- Write protection logic, where write operation is inhibited if  $\overline{OE}$  is held low or  $\overline{CE}$  or  $\overline{WE}$  is held high during power on or off of the  $V_{CC}$  supply voltage.

Timing Waveforms

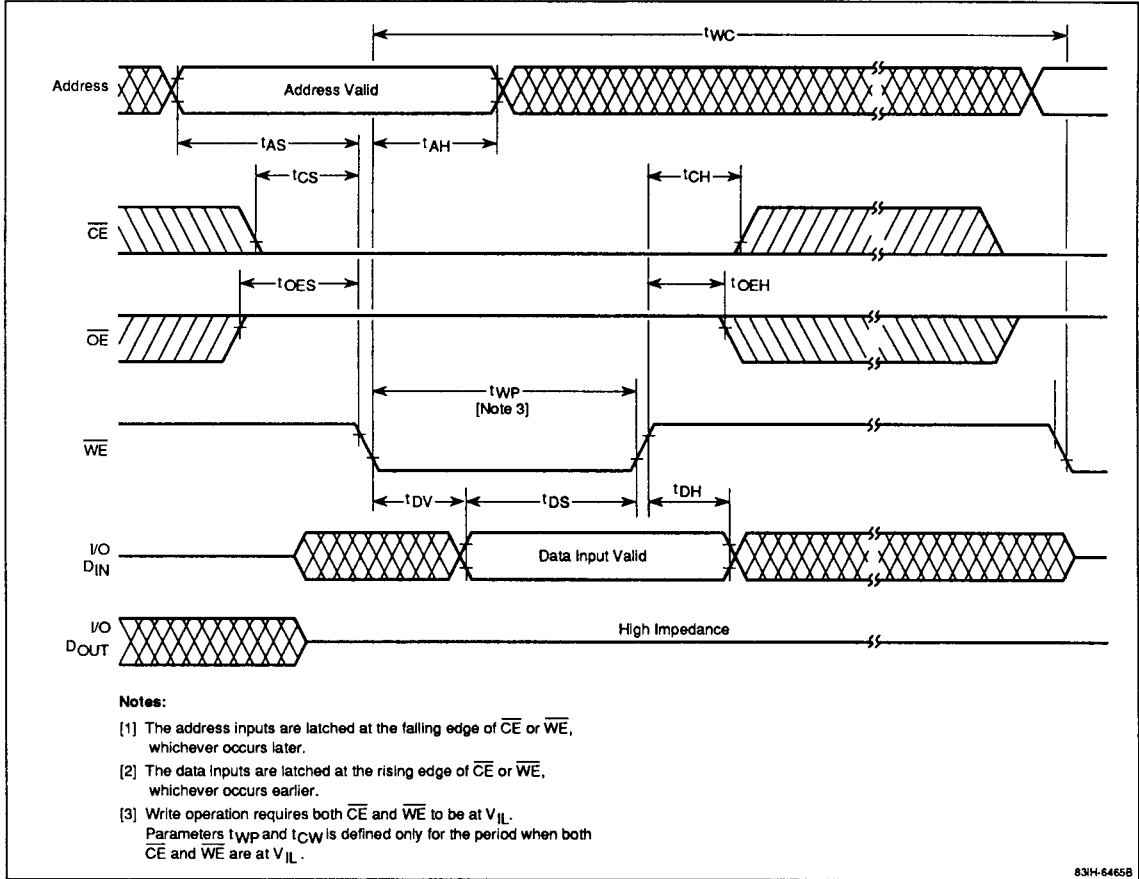
Read Cycle



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## Timing Waveforms (cont)

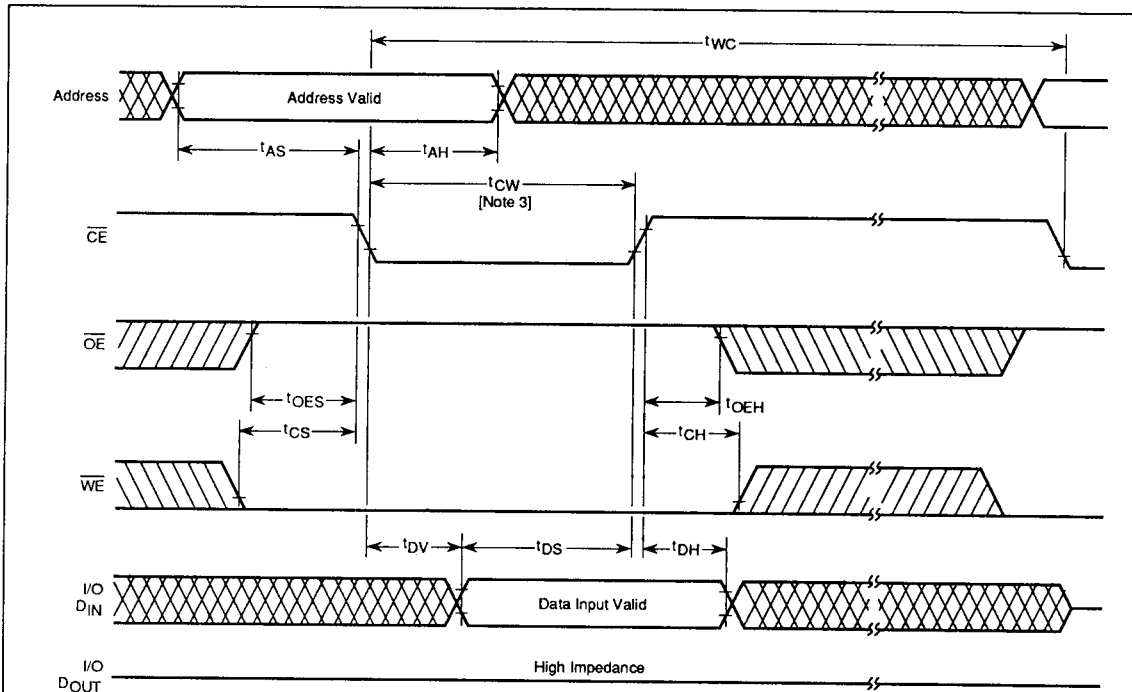
### WE-Controlled Write Cycle



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Timing Waveforms (cont)

**$\overline{CE}$ -Controlled Write Cycle**



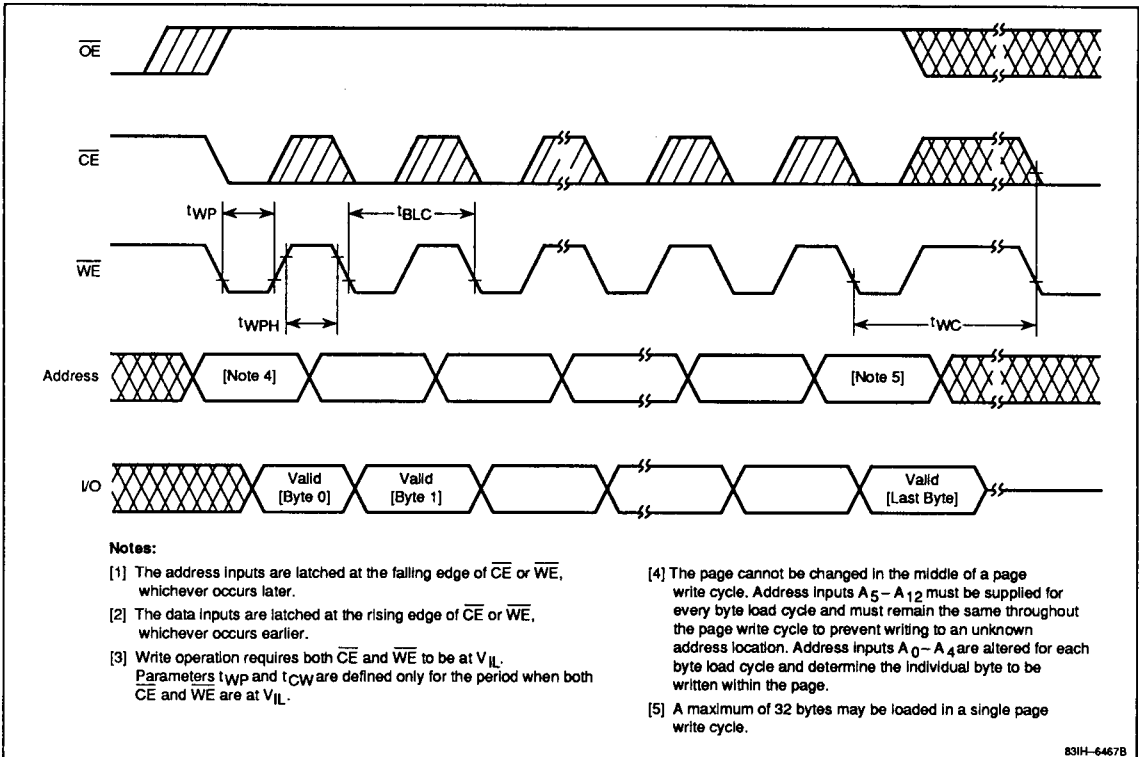
**Notes:**

- [1] The address inputs are latched at the falling edge of  $\overline{CE}$  or  $\overline{WE}$ , whichever occurs later.
- [2] The data inputs are latched at the rising edge of  $\overline{CE}$  or  $\overline{WE}$ , whichever occurs earlier.
- [3] Write operation requires both  $\overline{CE}$  and  $\overline{WE}$  to be at  $V_{IL}$ . Parameters  $t_{WP}$  and  $t_{CW}$  is defined only for the period when both  $\overline{CE}$  and  $\overline{WE}$  are at  $V_{IL}$ .
- [4]  $\overline{OE}$  may be delayed up to  $(t_{ACC} - t_{OE})$  without impacting  $t_{ACC}$ .

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## Timing Waveforms (cont)

### Page Write Cycle



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Timing Waveforms (cont)

Chip Erase Cycle

