HARRIS SEMICONDUCTOR

HC5506

ADVANCE INFORMATION

May 1995

DSLIC
Dual Ringing Subscriber Line Interface Circuit

Features

- Integration of Two SLICs in One Package
- Includes the Ringing Relay
- Current Limited Feed for Short Loops
- On-Hook Transmission
- TIP and RING Open State
- 2-Wire AC Loopback
- Zero Voltage On/Zero Current Off Switching of Ringing Waveform
- Switch Hook and Ground Key Detect on Separate Outputs
- Low Standby Power
- Meets CCITT Transmission Requirements
- 0°C to +70°C Ambient Temperature Range
- -48V Operation
- Selectable 2-Wire to 4-Wire and 4-Wire to 2-Wire Gains
- Resistive and Complex Impedance Matching
- Surface Mount Packaging

Applications

- Solid State Line Interface for Digital and Analog PBXs

Description

The HC5506 is a Dual Subscriber Line Interface Circuit (DSLIC) fabricated in a High Voltage Dielectrically Isolated Bipolar Process which replaces the transformer and ringing injection relays of two conventional PABX Subscriber Line Circuits, thereby increasing reliability, decreasing space occupied and reducing total system cost.

The DSLIC has been designed to utilize a minimum number of external components and require no precision components to guarantee performance.

The DSLIC contains a number of design innovations aimed at keeping the power dissipation on the die low. The DSLIC allows the use of a wide range of battery supply voltages in addition to a single +5V supply. The DSLIC also contains a number of features designed to facilitate production and field testing of PABX systems. These features include an AC loopback path and the control of the internal ringing switch.

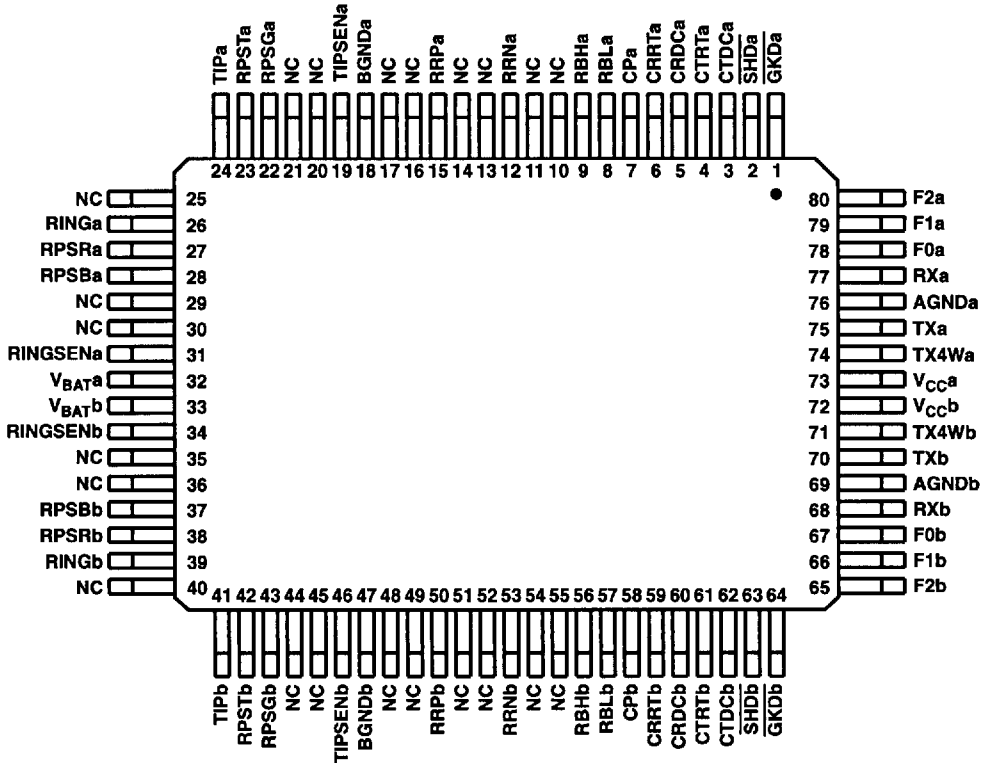
The HC5506 has been designed to easily interface with dual supply CODEC filters of either switched capacitor or DSP technologies. It will also easily interface to multichannel single or dual supply CODEC/filter devices either presently or soon to be available.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HC5506CQ	0°C to +70°C	80 Lead Plastic MQFP

Pinout

HC5506 (MQFP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number 3752.1

Absolute Maximum Ratings

V_{CC} to AGND 7V
V_{BAT} to BGND 60V
AGND to BGND ..... ±1V
VRRN or VRRP to BGND/AGND ..... +150V/-195V
Digital Pins to AGND ..... -1 to V_{CC}+0.5V
ESD Withstand (Human Body Model) 500V
Tip and Ring Pins, Pulse <1ms, t_{REP} >10s (Notes 1, 7) ..... TBD
Power Dissipation (Package) 1W
Junction Temperature ..... +150°C

Operating Conditions

Thermal Constants θ_{JA}
Plastic MQFP ..... 57.5°C/W
Operating Temperature Range
HC5506CQ ..... 0°C to +70°C
Storage Temperature Range ..... -65°C to +150°C
Line Leakage, R_{T-G}, R_{R-G}, R_{T-R} ..... ≥75kΩ

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Recommended Operating Conditions

For maximum integrity, nominal operating conditions should be selected so that operation is always within the following ranges

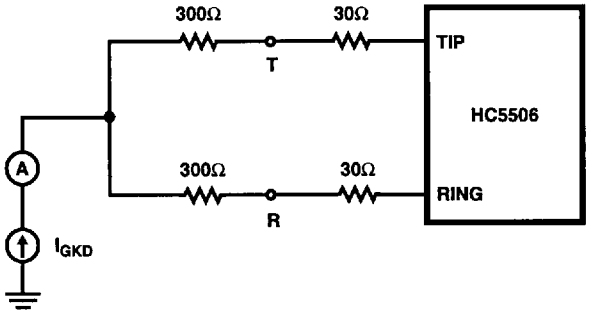
PARAMETER	CONDITIONS	MIN	MAX	UNITS
V_{BAT} to BGND		-42	-58	V
V_{CC} to AGND		4.75	5.25	V
Ringing Voltage	Ground or Battery Referenced, V_{BAT} = -42V to -58V	(0.8)(V_{BAT_MAX})	93	V_{RMS}
Ringing Frequency		18	54	Hz
Ringing Current (On-Hook)	V_{BAT} = -42V, $V_{RINGING}$ and $F_{RINGING}$ = Min to Max Recommended	-	90	mA_{PEAK}
Ringing Current (Off-Hook)		-	135	mA_{PEAK}

Electrical Specifications

Unless Otherwise Specified: Typical parameters are at T_A = +25°C, V_{CC} = +5V, V_{BAT} = -48V, AGND = BGND = 0V, Min-Max parameters are over operating temperature range. All parameters are specified at 600Ω 2-wire terminating resistance and impedance. The specifications are with respect to exact external component values.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
BATTERY/DC FEED - OFF-HOOK					
DC Loop Current	R_L = 1800Ω, V_{BAT} = -42.5V (Note 2)	16	-	-	mA
	R_L = 200Ω	-	35	TBD	mA
DC SIGNALING					
Switch-Hook Detect ($\overline{SHD}$)					
Off-Hook Detect Threshold	(Notes 1, 2)	5	7.5	10	mA
On-Hook Detect Threshold	$\overline{SHD}$ initially asserted (Notes 1, 2)	5	7.5	10	mA
Longitudinal Current Immunity (Per Wire)	(On-Hook, $\overline{SHD}$ not asserted) (Notes 1, 2, 4)	12	20	-	mA_{RMS}
	(Off-Hook, $\overline{SHD}$ not dropped) (Notes 1, 2, 3)	20	-	-	mA_{RMS}
Ground Key Detect ($\overline{GKD}$)					
Ground Detect Threshold	See Figure 1 (Notes 1, 2)	7	-	32.5	mA
Ground Release Threshold	$\overline{GKD}$ initially asserted (Notes 1, 2)	7	15	32.5	mA
Longitudinal Current Immunity (Per Wire)	I_{GKD} ≥ 30mA ($\overline{GKD}$, $\overline{SHD}$ not dropped) (Notes 1, 2, 3)	20	-	-	mA_{RMS}

Electrical Specifications Unless Otherwise Specified: Typical parameters are at T_A = +25°C, V_{CC} = +5V, V_{BAT} = -48V, AGND = BGND = 0V, Min-Max parameters are over operating temperature range. All parameters are specified at 600Ω 2-wire terminating resistance and impedance. The specifications are with respect to exact external component values. **(Continued)**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
 **FIGURE 1. GROUND KEY DETECT THRESHOLD**					
Dial Pulse Detect Dial Pulse Distortion (Mark-Space Ratio)	(Notes 1, 2, 3, 6)	-	-	±1	%
Longitudinal Current Immunity (Per Wire)	(Notes 1, 2, 3, 4)	12	20	-	mA_{RMS}
RINGING - ON-HOOK					
Ringing Zero Crossing Distortion	Battery Referenced, $F_{RINGING}$ and $V_{RINGING}$ = $85V_{RMS}$, Z_L = 450Ω + 3.4µF or Z_L = 15kΩ II (6µF + 670Ω) (Notes 1, 2, 8)	-	1.5	2	%
V_T - V_R Residual	$F_{RINGING}$ and $V_{RINGING}$ = Max Recommended, C Message	-	6	-	dBrnC
	$F_{RINGING}$ and $V_{RINGING}$ = Max Recommended (Notes 1, 2)	-	-44	-33	dBm
RINGING - OFF-HOOK					
Ring Trip Comparator Threshold	$\frac{RRS}{RBAL}$ = 484 (Notes 1, 2)	6	10	14	mA_{DC}
WINK-OFF					
Wink-Off Loop Current	R_L = 0Ω (Notes 1, 2, 3, 5)	-	-	±750	µA
Propagation Delay Loop Start to Wink-Off	R_L = 600Ω, I_L < 1mA (Notes 1, 2)	-	-	2	ms
Propagation Delay Wink-Off to Loop Start	R_L = 600Ω, I_L > 90% of Nominal (600Ω) Value (Notes 1, 2)	-	-	20	ms
ON-HOOK TRANSMISSION					
Signal Level V_T - V_R	Z_L = 600Ω + 2.16µF, 0.1dB Compression (Notes 1, 2)	2.18	3.9	-	V_{PEAK}
Longitudinal Current Immunity (Per Wire)	I_{LOOP} = 0mA, $\overline{SHD}$ and $\overline{GKD}$ not Asserted by Longitudinal Current (Notes 1, 2, 4)	12	20	-	mA_{RMS}
2-WIRE PORT					
2-Wire Return Loss	F = 200Hz to 500Hz, Reference 600Ω (Notes 1, 2)	28	30	-	dB
	F = 500Hz to 3400Hz, Reference 600Ω (Notes 1, 2)	30	36	-	dB

Electrical Specifications Unless Otherwise Specified: Typical parameters are at T_A = +25°C, V_{CC} = +5V, V_{BAT} = -48V, AGND = BGND = 0V, Min-Max parameters are over operating temperature range. All parameters are specified at 600Ω 2-wire terminating resistance and impedance. The specifications are with respect to exact external component values. **(Continued)**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
2WL - 2WM Balance	F = 300Hz to 600Hz, CCITT Test Circuit (Notes 1, 2)	40	-	-	dB
	F = 600Hz to 2400Hz, CCITT Test Circuit (Notes 1, 2)	46	-	-	dB
	F = 2400Hz to 3400Hz, CCITT Test Circuit (Notes 1, 2)	41	-	-	dB
2WL - 4WM Balance	F = 300Hz to 600Hz, CCITT Test Circuit (Notes 1, 2)	40	-	-	dB
	F = 600Hz to 2400Hz, CCITT Test Circuit (Notes 1, 2)	46	-	-	dB
	F = 2400Hz to 3400Hz, CCITT Test Circuit (Notes 1, 2)	41	-	-	dB
AC PERFORMANCE - 4-WIRE TO 2-WIRE TRANSMISSION (Z_L = R_L = 600Ω)					
Absolute Gain Accuracy	V_{RX} = 0dBm at 1kHz, 4-Wire to 2-Wire Gain = -6.02dB (Notes 1, 2)	-	-	±0.15	dB
Insertion Delay	F = 300Hz to 3400Hz	-	2	TBD	µs
Gain Linearity	V_{RX} = +3dBm to -40dBm (Notes 1, 2)		±0.02	±0.05	dB
Reference: V_{RX} = 0dBm at 1kHz 4-Wire to 2-Wire Gain = -6.02dB	V_{RX} = -40dBm to -50dBm (Notes 1, 2)	-	±0.07	±0.10	dB
	V_{RX} = -50dBm to -55dBm (Notes 1, 2)	-	±0.15	±0.30	dB
Frequency Response	F = 300Hz to 3400Hz. Reference: V_{RX} = 0dBm at 1kHz 4-Wire to 2-Wire Gain = -6.02dB (Notes 1, 2)	-	±0.01	±0.05	dB
2-Wire Overload Level Reference: V_{RX} = 0dBm at 1kHz, 4-Wire to 2-Wire Gain = -6.02dB	0.1dB Compression at 2-Wire Interface. (Notes 1, 2)	1.74	4.24	-	V_{PEAK}
SIGNAL DEGRADATION - 4-WIRE TO 2-WIRE TRANSMISSION (Z_L = R_L = 600Ω)					
Idle Channel Noise	P Message (Notes 1, 2)	-	-	-80	dBmOp
2-Wire Crosstalk Attenuation	F = 300Hz to 3200Hz	-	80	-	dB
PSRR V_{BAT} to 2-Wire	F = 30Hz to 60Hz, V_{AC} = 200mV_{RMS} (Notes 1, 2)	15	25	-	dB
PSRR V_{CC} to 2-Wire		15	30	-	dB
PSRR V_{BAT} to 2-Wire	F = 200Hz to 16kHz, V_{AC} = 200mV_{RMS} (Notes 1, 2)	20	30	-	dB
PSRR V_{CC} to 2-Wire		20	30	-	dB
AC PERFORMANCE - 2-WIRE TO 4-WIRE TRANSMISSION (Z_L = R_L = 600Ω)					
Absolute Gain Accuracy	V_{2W} = 0dBm at 1kHz, 2-Wire to 4-Wire Gain = 0dB (Notes 1, 2)	-	±0.05	±0.15	dB
Insertion Delay	F = 300Hz to 3400Hz	-	0.1	TBD	µs
Gain Linearity	V_{2W} = +3dBm to -40dBm (Notes 1, 2)	-	-	±0.05	dB
Reference: V_{2W} = 0dBm at 1kHz, 2-Wire to 4-Wire Gain = 0dB	V_{2W} = -40dBm to -50dBm (Notes 1, 2)	-	-	±0.10	dB
	V_{2W} = -50dBm to -55dBm (Notes 1, 2)	-	-	±0.30	dB
Frequency Response	F = 300Hz to 3400Hz. Reference: V_{2W} = 0dBm at 1kHz, 2-Wire to 4-Wire Gain = 0dB (Notes 1, 2)	-	±0.01	±0.05	dB
4-Wire (V_{TX}) Overload Level Reference: V_{2W} = 0dBm at 1kHz, 2-Wire to 4-Wire Gain = 0dB	0.1dB Compression at 4-Wire Interface, R_L = 1800Ω, V_{BAT} = -42V (Note 2)	1.55	-	-	V_{PEAK}

Electrical Specifications Unless Otherwise Specified: Typical parameters are at T_A = +25°C, V_{CC} = +5V, V_{BAT} = -48V, AGND = BGND = 0V, Min-Max parameters are over operating temperature range. All parameters are specified at 600Ω 2-wire terminating resistance and impedance. The specifications are with respect to exact external component values. **(Continued)**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SIGNAL DEGRADATION - 2-WIRE TO 4-WIRE TRANSMISSION ($Z_L = R_L$ = 600Ω)					
Idle Channel Noise	P Message (Notes 1, 2)	-	-	-80	dBmOp
4-Wire Crosstalk Attenuation	F = 300Hz to 3200Hz	-	80	-	dB
PSRR V_{BAT} to 4-Wire	F = 30Hz to 60Hz, V_{AC} = 200mV_{RMS} (Notes 1, 2)	15	25	-	dB
PSRR V_{CC} to 4-Wire		15	25	-	dB
PSRR V_{BAT} to 4-Wire	F = 200Hz to 16kHz, V_{AC} = 200mV_{RMS} (Notes 1, 2)	20	25	-	dB
PSRR V_{CC} to 4-Wire		15	22	-	dB
AC PERFORMANCE - 4-WIRE TO 4-WIRE TRANSMISSION ($Z_L = R_L$ = 600Ω)					
Absolute Gain Accuracy	V_{RX} = 0dBm at 1kHz, 4-Wire to 2-Wire Gain = -6.02dB, 2-Wire to 4-Wire Gain = 0dB (Notes 1, 2)	-	-	±0.15	dB
Insertion Delay		-	2	TBD	µs
DIGITAL PINS					
V_{IH}	LSTTL (Notes 1, 2)	2.0	-	-	V
V_{IL}		-	-	0.8	V
I_{OH}		-	-	-80	µA
I_{OL}	LSTTL, $\overline{SHD}$ (Notes 1, 2)	-	-	10	mA
	LSTTL, $\overline{GKD}$ (Notes 1, 2)	-	-	800	µA
V_{OH}	V_{CC} = 5.0V, I_{OH} = -80µA ($\overline{SHD}$, $\overline{GKD}$) (Notes 1, 2)	2.4	-	5.5	V
V_{OL}	V_{CC} = 5.0V, I_{OL} = 10mA ($\overline{SHD}$), I_{OL} = 800µA ($\overline{GKD}$) (Notes 1, 2)	0	-	0.5	V
I_{IH}	V_{CC} = 5.25V, V_I = 2.0V to 5V (Notes 1, 2)	-	-	40	µA
I_{IL}	V_{CC} = 5.25V, V_I = 0.0V to 0.8V (Notes 1, 2)	-	-	-0.4	mA
SUPPLY CURRENTS					
I_{CC} Supply Current (Package)	Both SLICs: Loop Start, R_L = Open, V_{BAT} = -58V, V_{CC} = 5.25V (Note 2)	-	8.2	13.0	mA
I_{BAT} Supply Current (Package)		-	11.3	15.0	mA
I_{CC} Supply Current (Package)	Both SLICs: Wink-Off, R_L = Open, V_{BAT} = -58V, V_{CC} = 5.25V (Note 2)	-	7.6	13.0	mA
I_{BAT} Supply Current (Package)		-	1.5	3.5	mA

NOTE:

1. Minimum and Maximum apply for V_{BAT} = -42V to -58V and V_{CC} = 4.75V to 5.25V (unless otherwise stated in the conditions).
2. Minimum and Maximum limits apply for $T_{AMBIENT}$ = 0°C to +70°C.
3. Minimum and Maximum values apply for R_{LOOP} = 200Ω to 1800Ω.
4. On-Hook Longitudinal Current Immunity is a function of $T_{AMBIENT}$ as described in the applications section of this datasheet. For $T_{AMBIENT}$ = +25°C, typical on-hook Longitudinal Current Immunity is 20mA_{RMS}.
5. Leakage dominated by V_{BAT} and two 80kΩ (RS) sense resistors.
6. Measured while in On-Hook Transmission.
7. Pulse applied outside RP. RP is 30Ω ±10%.
8. Distortion approximately inversely proportional to RMS ringing level.

Pin Descriptions

MQFP	SYMBOL	DESCRIPTION
1	$\overline{\text{GKDa}}$	Ground Key Detect a - An active low logic output. A line supervisory output. Valid when $\overline{\text{SHDa}}$ is also asserted.
2	$\overline{\text{SHDa}}$	Switch Hook Detect a - An active low logic output. A line supervisory output.
3	CTDCa	Capacitor Tip DC a - An external capacitor to be connected between this terminal and CTRTa; required to properly separate the Tip AC current from the DC loop current and for proper ring trip operation. This node will be a virtual ground when SLIC A is in the ringing state.
4	CTRTa	Capacitor Tip Ring Trip a - An external capacitor to be connected between this terminal and CTDCa; required to properly separate the Tip AC current from the DC loop current and for proper ring trip operation. This node will be a virtual ground when SLIC A is in all but the ringing state.
5	CRDCa	Capacitor Ring DC a - An external capacitor to be connected between this terminal and CRRTa; required to properly separate the Ring AC current from the DC loop current and for proper ring trip operation. This node will be a virtual ground when SLIC A is in the ringing state.
6	CRRTa	Capacitor Ring - Ring Trip a - An external capacitor to be connected between this terminal and CRDCa; required to properly separate the Ring AC current from the DC loop current and for proper ring trip operation. This node will be a virtual ground when SLIC A is in all but the ringing state.
7	CPa	Capacitor Power battery supply filtering a - An external capacitor to be connected between this terminal and battery ground. Used to provide a filtered virtual battery for the SLIC.
8	RBLa	Ringer Ballast Sense Low Side a - RBLa and RBHa connect across one of the ringer ballast resistors. RBL is connected on the side of the ballast resistor where the lower DC potential exists when the set goes off-hook.
9	RBHa	Ringer Ballast Sense High Side a - RBLa and RBHa connect across one of the ringer ballast resistors. RBH is connected on the side of the ballast resistor where the higher DC potential exists when the set goes off-hook.
12	RRNa	Ring Relay Negative a - The Ring side ring generator connection for SLIC A. RRPa and RRNa allow the SLIC to ring the line. When the ringing state is selected using the logic inputs, this node is connected to the RINGa output through an internal ring relay. For battery backed or earth backed ringing, this node should be connected such that its DC potential is battery and should always include a current limiting ballast resistor between it and the battery or the ringer.
15	RRPa	Ring Relay Positive a - The Tip side ring generator connection for SLIC A. RRPa and RRNa allow the SLIC to ring the line. When the ringing state is selected using the logic inputs, this node is connected to the TIPa output through an internal ring relay. For battery backed or earth backed ringing, this node should be connected such that its DC potential is ground and should always include a current limiting ballast resistor between it and ground or the ringer.
18	BGNDa	Battery Ground a - To be connected to zero potential. All loop current and longitudinal current flow from this ground. Internally separate from BGNDb but it is recommended that it is connected to the same potential as BGNDb.
19	TIPSENa	Tip Sense a - A low impedance analog input to be connected to the 2-Wire Tip terminal of SLIC A through an external resistor. Senses the 2-Wire Tip voltage present on the line.
22	RPSGa	Resistor Power Sharing Ground a - An external resistor connected between this node and RPSTa diverts power from SLIC A during short loops and longitudinal currents. This node will nominally be at ground potential.
23	RPSTa	Resistor Power Sharing Tip a - An external resistor connected between this node and RPSGa diverts power from SLIC A during short loops and longitudinal currents. This node will nominally be at the same potential as TIPa.
24	TIPa	Tip a - A current feed analog output to be connected to the 2-Wire Tip terminal of SLIC A through an external feed resistor. Functions with RINGa to supply loop current and feed voice signals to the 2-Wire loop and also to sink longitudinal currents.
26	RINGa	Ring a - A current feed analog output to be connected to the 2-Wire Ring terminal of SLIC A through an external resistor. Functions with TIPa to supply loop current and feed voice signals to the 2-Wire loop and also to sink longitudinal currents.
27	RPSRa	Resistor Power Sharing Ring a - An external resistor connected between this node and RPSBa diverts power from SLIC A during short loops and longitudinal currents. This node will nominally be at the same potential as RINGa.
28	RPSBa	Resistor Power Sharing Battery a - An external resistor connected between this node and RPSRa diverts power from SLIC A during short loops and longitudinal currents. This node will nominally be at battery potential.
31	RINGSENa	Ring Sense a - A low impedance analog input to be connected to the 2-Wire Ring terminal of SLIC A through an external resistor. Senses the 2-Wire Ring voltage present on the line.

Pin Descriptions (Continued)

MQFP	SYMBOL	DESCRIPTION
32	$V_{BAT}a$	Voltage Battery a - The battery voltage source. The most negative supply. Internal ohmic connection to $V_{BAT}b$ so it should be at same potential as $V_{BAT}b$. All loop and longitudinal currents flow into this node.
33	$V_{BAT}b$	Voltage Battery b - The battery voltage source. The most negative supply. Internal ohmic connection to $V_{BAT}a$ so it should be at same potential as $V_{BAT}a$. All loop and longitudinal current flow into this node.
34	RINGSENb	Ring Sense b - A low impedance analog input to be connected to the 2-Wire Ring terminal of SLIC B through an external resistor. Senses the 2-Wire Ring voltage present on the line.
37	RPSBb	Resistor Power Sharing Battery b - An external resistor connected between this node and RPSRb diverts power from SLIC B during short loops and longitudinal currents. This node will nominally be at battery potential.
38	RPSRb	Resistor Power Sharing Ring b - An external resistor connected between this node and RPSBb diverts power from SLIC B during short loops and longitudinal currents. This node will nominally be at the same potential as RINGb.
39	RINGb	Ring b - A current feed analog output to be connected to the 2-Wire Ring terminal of SLIC B through an external resistor. Functions with TIPb to supply loop current and feed voice signals to the 2-Wire loop and also to sink longitudinal currents.
41	TIPb	Tip b - A current feed analog output to be connected to the 2-Wire Tip terminal of SLIC B through an external feed resistor. Functions with RINGb to supply loop current and feed voice signals to the 2-Wire loop and also to sink longitudinal currents.
42	RPSTb	Resistor Power Sharing Tip b - An external resistor connected between this node and RPSGb diverts power from SLIC B during short loops and longitudinal currents. This node will nominally be at the same potential as TIPb.
43	RPSGb	Resistor Power Sharing Ground b - An external resistor connected between this node and RPSTb diverts power from SLIC B during short loops and longitudinal currents. This node will nominally be at ground potential.
46	TIPSENb	Tip Sense b - A low impedance analog input to be connected to the 2-Wire Tip terminal of SLIC B through an external resistor. Senses the 2-Wire Tip voltage present on the line.
47	BGNDb	Battery Ground b - To be connected to zero potential. All loop current and longitudinal current flow from this ground. Internally separate from BGNDa but it is recommended that it is connected to the same potential as BGNDa.
50	RRPb	Ring Relay Positive b - The Tip side ring generator connection for SLIC B. RRPb and RRNb allow the SLIC to ring the line. When the ringing state is selected using the logic inputs, this node is connected to the TIPb output through an internal ring relay. For battery backed or earth backed ringing, this node should be connected such that its DC potential is ground and should always include a current limiting ballast resistor between it and ground or the ringer.
53	RRNb	Ring Relay Negative b - The Ring side ring generator connection for SLIC B. RRPb and RRNb allow the SLIC to ring the line. When the ringing state is selected using the logic inputs, this node is connected to the RINGb output through an internal ring relay. For battery backed or earth backed ringing, this node should be connected such that its DC potential is battery and should always include a current limiting ballast resistor between it and the battery or the ringer.
56	RBHb	Ringer Ballast Sense High Side b - RBLa and RBHa connect across one of the ringer ballast resistors. RBH is connected on the side of the ballast resistor where the higher DC potential exists when the set goes off-hook.
57	RBLb	Ringer Ballast Sense Low Side b - RBLa and RBHa connect across one of the ringer ballast resistors. RBL is connected on the side of the ballast resistor where the lower DC potential exists when the set goes off-hook.
58	CPb	Capacitor Power Battery Supply Filtering b - An external capacitor to be connected between this terminal and battery ground. Used to provide a virtual battery for the SLIC.
59	CRRTb	Capacitor Ring - Ring Trip b - An external capacitor to be connected between this terminal and CRDCb; required to properly separate the Ring AC current from the DC loop current and for proper ring trip operation. This node will be a virtual ground when SLIC B is in all but the ringing state.
60	CRDCb	Capacitor Ring DC b - An external capacitor to be connected between this terminal and CRRTb; required to properly separate the Ring AC current from the DC loop current and for proper ring trip operation. This node will be a virtual ground when SLIC B is in the ringing state.
61	CTRTb	Capacitor Tip Ring Trip b - An external capacitor to be connected between this terminal and CTDCb; required to properly separate the Tip AC current from the DC loop current and for proper ring trip operation. This node will be a virtual ground when SLIC B is in all but the ringing state.

Pin Descriptions (Continued)

MQFP	SYMBOL	DESCRIPTION
62	CTDCb	Capacitor Tip DC b - An external capacitor to be connected between this terminal and CTRTb; required to properly separate the Tip AC current from the DC loop current and for proper ring trip operation. This node will be a virtual ground when SLIC B is in the ringing state.
63	$\overline{SHDb}$	Switch Hook Detect b - An active low logic output. A line supervisory output.
64	$\overline{GKDb}$	Ground Key Detect b - An active low logic output. A line supervisory output. Valid when $\overline{SHDa}$ is also asserted.
65	F2b	Function Control 2 b - A logic input which along with F1b and F0b control the operational state of SLIC B. See the Truth Table below.
66	F1b	Function Control 1 b - A logic input which along with F2b and F0b control the operational state of SLIC B. See the Truth Table below.
67	F0b	Function Control 0 b - A logic input which along with F2b and F1b control the operational state of SLIC B. See the Truth Table below.
68	RXb	Receive b - Four wire receive input. A current-sense input whose signal appears differentially across TIPb and RINGb. Nominal voltage is AGND but must be AC coupled.
69	AGNDb	Analog Ground b - To be connected to zero potential. Serves as a reference for the transmit output and the receive input of SLIC B.
70	TXb	Transmit b - Four wire transmit output. A low impedance analog output representing the differential signal sensed across TIPb and RINGb. Transhybrid balancing must be performed beyond this output to completely implement two to four wire conversion. Nominal voltage is AGND but must be AC coupled.
71	TX4Wb	Transmit Gain 4-Wire b - A current output/voltage sensing input. Placing an external resistor to AGND at this node establishes the two to four wire gain (loss) as described in the applications section.
72	$V_{CC}b$	Positive Voltage Supply b - Most positive supply. Internally separate from $V_{CC}a$.
73	$V_{CC}a$	Positive Voltage Supply a - Most positive supply. Internally separate from $V_{CC}b$.
74	TX4Wa	Transmit Gain 4-Wire a - A current output/voltage sensing input. Placing an external resistor to AGND at this node establishes the two to four wire gain (loss) as described in the applications section.
75	TXa	Transmit a - Four wire transmit output. A low impedance analog output representing the differential signal sensed across TIPa and RINGa. Transhybrid balancing must be performed beyond this output to completely implement two to four wire conversion. Nominal voltage is AGND but must be AC coupled.
76	AGNDa	Analog Ground a - To be connected to zero potential. Serves as a reference for the transmit output and the receive input of SLIC A.
77	RXa	Receive a - Four wire receive input. A current-sense input whose signal appears differentially across TIPa and RINGa. Nominal voltage is AGND but must be AC coupled.
78	F0a	Function Control 0 a - A logic input which along with F2a and F1a control the operational state of SLIC A. See the Truth Table below.
79	F1a	Function Control 1 a - A logic input which along with F2a and F0a control the operational state of SLIC A. See the Truth Table below.
80	F2a	Function Control 2 a- A logic input which along with F1a and F0a control the operational state of SLIC A. See the Truth Table below.
10,11, 13, 14, 16, 17, 20, 21, 25, 29, 30, 35, 36, 40, 44, 45, 48, 49, 51, 52, 54, 55	NC	No Internal Connection

Truth Table

F2	F1	F0	OPERATION	ABBREVIATION	COMMENTS
0	0	0	Wink Off	WO	
0	0	1	Loop Start	LS	
0	1	0	Not Used	na	
0	1	1	Not Used	na	
1	0	0	Ringing	RING	
1	0	1	Loop Start (Not Used)	na	Use Above Loop Start Code
1	1	0	Loop Start (Not Used)	na	Use Above Loop Start Code
1	1	1	On Hook Transmission	OHT	

0 - Analog Ground 1 - V_{CC}

Application Information

Design Equations

$$A_{2-4} = \frac{RTX}{171.3k} \quad \text{(EQ. 1)}$$

$$RTX = 171.3k \times A_{2-4} \quad \text{(EQ. 2)}$$

$$Z_M = \frac{171.3k \times RZAC}{(RTX) \times 390} \quad \text{(EQ. 3)}$$

$$RZAC = \frac{(RTX) \times (Z_M) \times 390}{171.3k} \quad \text{(EQ. 4)}$$

$$A_{4-2} = \frac{-171.3k \times RZAC}{(RRX) \times (RTX)} \times \frac{1}{1 + \frac{Z_M}{Z_L}} \quad \text{(EQ. 5)}$$

$$RRX = \frac{171.3k\,(RZAC)}{(A_{4-2}) \times (RTX)} \times \frac{1}{1 + \frac{Z_M}{Z_L}} \quad \text{(EQ. 6)}$$

$$A_{4-4} = \frac{-RZAC}{RRX} \times \frac{1}{1 + \frac{Z_M}{Z_L}} \quad \text{(EQ. 7)}$$

where:

1. Z_M = Desired SLIC 2-Wire synthesized impedance
2. Z_L = 2-Wire Line Impedance
3. 390 = G = internal SLIC current gain
4. 171.3k = 2(80k + 5.65k) where
   80k = external Tip or Ring sense resistor (R_S) and
   5.65k = internal sense resistance

Ring Trip Design Equations:

$$I_{TH} = \frac{10mA}{484} \times \frac{RRS}{RBal}, \quad RBal = \text{resistance between RBH and RBL (= RBALN or RBALP)} \quad \text{(EQ. 8)}$$

For I_{TH} = 10mA:

$$\frac{RRS}{RBal} = 484 \quad \text{(EQ. 9)}$$

Applications Diagram

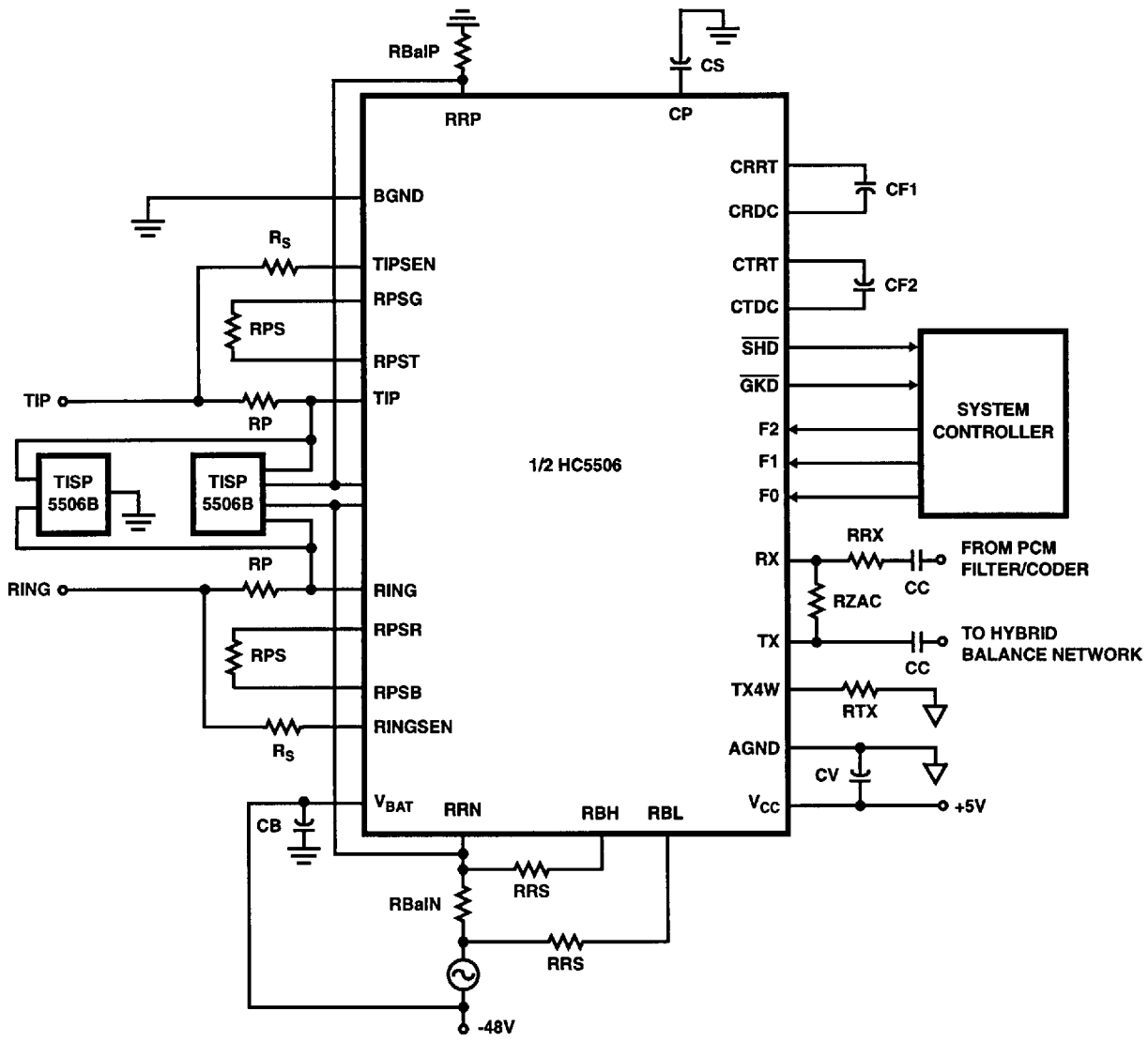


FIGURE 1. TYPICAL LINE CIRCUIT APPLICATION WITH THE MONOLITHIC SLIC

Typical Component Values 2-Wire to 4-Wire Gain = 0dB; 4-Wire to 2-Wire Gain = -6.02dB, Z_{MATCH} = 600Ω

COMPONENT	VALUE	TOLERANCE	% MATCH	RATING	FUNCTION
RBALN	620Ω	1%	-	-	Ring Generator Resistor, Battery Referenced
RBALP	620Ω	1%	-	-	Ring Generator Resistor, Ground Referenced
RRS	301kΩ	1%	-	-	Ring Trip Sensing Resistor
RPS	700Ω	1%	-	1W	Tip and Ring Power Sharing Resistors
RP	30Ω	1%	-	1/2W	Tip and Ring Protection Resistors
RS	80kΩ	1%	0.5 to RS	1/8W	Tip and Ring Sensing Resistors
RRX	234kΩ	1%	0.5 to RZAC	1/8W	Receive Input Resistor, Sets 4-Wire to 2-Wire Gain
RZAC	234kΩ	1%	0.5 to RRX	1/8W	Tip-Ring AC Impedance Setting Resistor
RTX	171.3kΩ	1%	0.5 to RS	1/8W	Transmit Output Resistor, Sets 2-Wire to 4-Wire Gain

Typical Component Values 2-Wire to 4-Wire Gain = 0dB; 4-Wire to 2-Wire Gain = -6.02dB, Z_{MATCH} = 600Ω **(Continued)**

COMPONENT	VALUE	TOLERANCE	% MATCH	RATING	FUNCTION
CF2	0.2µF	20%	-	70V	Tip Filter and Ring Trip Capacitor
CF1	0.2µF	20%	-	70V	Ring Filter and Ring Trip Capacitor
CS	0.2µF	20%	-	70V	Battery Supply Filtering Capacitor
CRX	1.0µF	-	-	10V	Receive Coupling Capacitor
CB	0.1µF	20%	-	100V	Power Supply Filter Capacitor
CV	0.1µF	20%	-	10V	Power Supply Filter Capacitor
CC	0.2µF - 1µF	20%	-	10V	CODEC Coupling Capacitor

Functional Description

General Circuit Operations

The HC5506 has four operating states controlled by three digital inputs: F0, F1, F2. The Logic and Control circuitry must interpret these input signals as well as the signals from various threshold detectors and then direct the proper circuit operations through the use of control signals. In addition, it must channel the proper signal to the digital outputs. These operating states are:

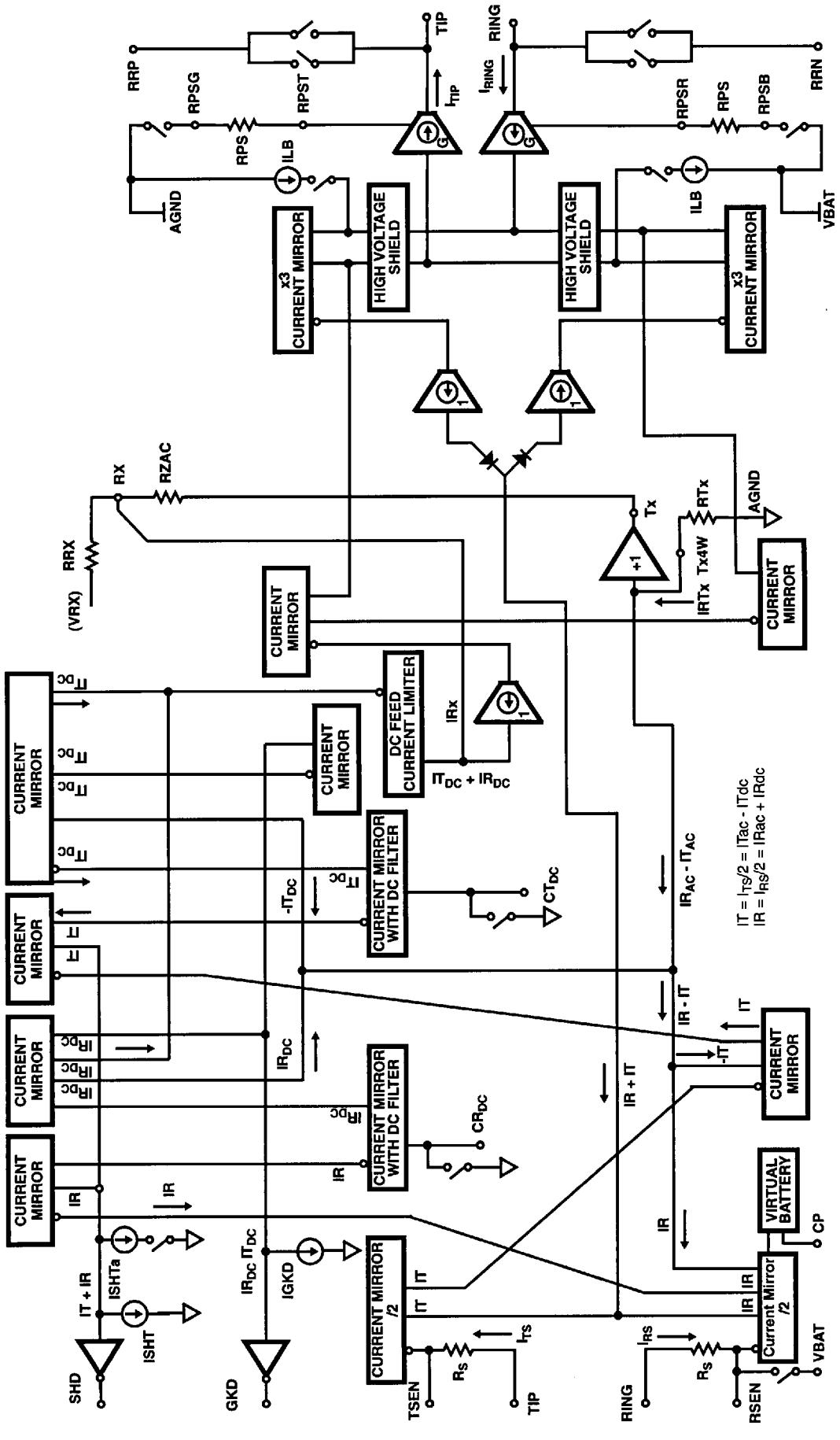
Loop Start (LS) - Normal loop feeding. The feed amplifiers are powered and the SLIC is prepared to detect off-hook and feed the line. The default state.

Wink Off (WO) - All hybrid circuitry is powered down, placing the Tip and Ring amplifiers in a high impedance state. No valid outputs.

Ringing (Ring) - Internal SCR switches connect the ringing signal to the line when the ringer goes through a zero crossing. The zero crossing is determined to have occurred when the voltage at RRP is greater than the voltage at RRN by approximately battery. The Ring Trip Detector is active and the feed amplifiers are powered down until an off-hook occurs or the state is changed. Upon an off-hook condition, the SLIC deactivates the SCR switches and reactivates the Hybrid. Once an off-hook occurs, $\overline{SHD}$ is held low until the SLIC's state is externally switched to Loop Start (or something other than RING) whereby $\overline{SHD}$ then follows the Switch Hook Detector. Therefore, the SLIC must be changed to the Loop Start mode after $\overline{SHD}$ goes low.

On Hook Transmission (OHT) - Tip and Ring DC voltages levels pulled towards each other to enable AC transmission. It also modifies the $\overline{SHD}$ threshold so that the modified Tip and Ring DC levels are not interpreted as an off-hook condition.

Functional Diagram



NOTE: Tip and Ring are shown twice for clarity; each reference to Tip is the same node, and each reference to Ring is the same node.

Logic Description

Circuit Implementation

The logic is implemented using Schottky Logic gates. Each gate is a wired NAND with multiple inputs and no more than two outputs.

Internal States and Signals

The table below summarizes the link between the SLIC operating states and the actions taken by the SLIC in that state. The actions result from a control signal that comes from either the logic or from the output of one of the detectors. These signals and actions are:

SHDO - Switch Hook Detect Output.

GKDO - Ground Key Detect Output.

SHDet - Internal Switch Hook Detector signal.

GKDet - Internal Ground Key Detector signal.

$\overline{\text{RTDet}}$ - Internal Ring Trip Detector signal used for Ringing.

PFA (Powers the Feed Amplifiers) - control signal generated by the logic which enables the feed amplifiers (when low) and the rest of the Hybrid.

$\overline{\text{FOC}}$ (Feedback Offset Current) - internal control signal generated in the Hybrid using signals from the logic; alters the DC feedback for On-Hook Transmission.

$\overline{\text{RingSw}}$ (Ringing Switch) - internal control signal enabling the switches connecting the ringing signal to the subscriber line.

$\overline{\text{PSRS}}$ (Power Sharing Resistors Switches) - When in Loop Feed, the SLIC closes the switches connecting the power sharing resistors to the feed amplifiers. Upon off-hook condition, The Hybrid controls the switches based upon the status of PFA and OHTO.

Decoder

The decoder interprets the three input signals (F0, F1, F2) to enable a specific Mode (see Truth Table). The decoder output is such that Loop Start mode is the "default" mode. When Loop Start is selected the decoder simply turns off all of the non-Loop Start functions and what is left is Loop Start. The two extra codes also will place the SLIC into Loop Start but it is recommended these codes not be used.

Ring Trip Control Logic

The Ring Trip control logic uses a state variable to store the ringing condition. An R-S flip-flop is used to store the presence of a prior ring trip occurrence in order to prevent ringing from being reapplied if the Subscriber goes Off-Hook and then On-Hook before the command for ringing is removed. Also, circuitry prevents the Ring Relays from being activated while there is an Off-Hook Signal from the Switch Hook Detector.

Loop Start Operation

The feed amplifiers are active and the Power Savings Resistors are connected during both On-Hook and Off-Hook operations. This is the default mode.

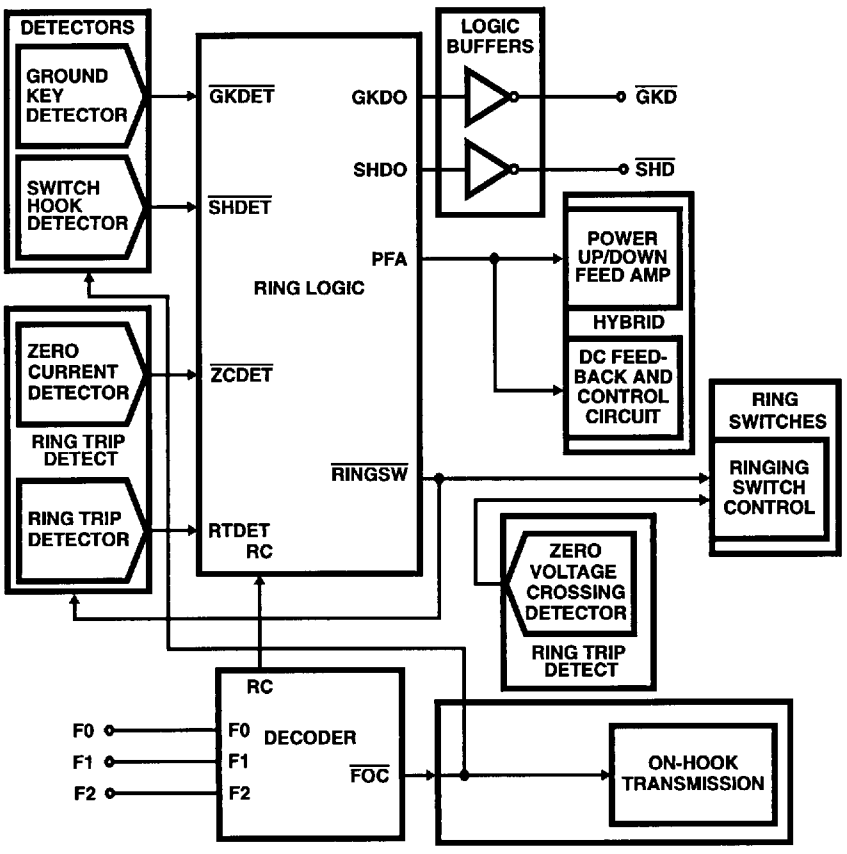


FIGURE 2. LOGIC BLOCK DIAGRAM

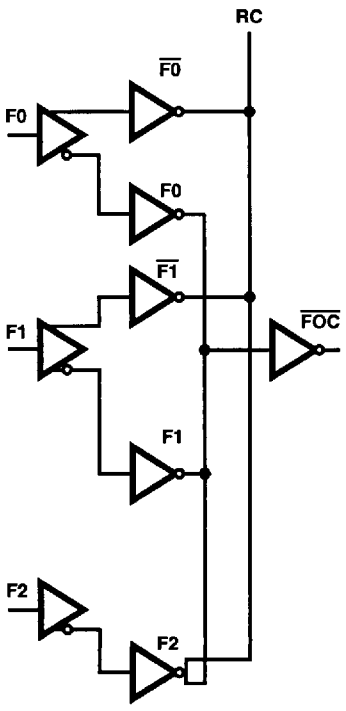


FIGURE 3. DECODER

Wink Off

Wink Off Mode places the output amplifiers into a high impedance state such that subscriber current is near zero. $\overline{SHD}$ and $\overline{GKD}$ are deasserted (held high) because $\overline{GKDet}$ and $\overline{SHDet}$ are held high.

SLIC STATE vs CONTROL SIGNAL/BLOCK STATUS

□ = OUTPUT

SLIC STATE (0-ACTIVE 1-INACTIVE)

SIGNAL OR ACTION	LOOP-START ON- OR OFF-HOOK	WINK OFF (WO)	RINGING (RING)	OHT
$\overline{PSRS}$	0	1	1	1
PFA	0	1	1	0
$\overline{FOC}$	1	1	1	0
$\overline{RingSw}$	1	1	0	1
SHDO	SHD LS	SHD LS Not Valid	Filtered RTD	SHD OHT
GKDO	LS GKD	LS GKD	Always High	LS GKD

Ringing

Upon the Ring Command (RC), the Logic applies a signal to the switches ($\overline{RINGSWT}$). The switches stay on until one of two events take place. One, the initiating caller discontinues the call, RC goes low and $\overline{RINGSWT}$ goes inactive. Two, the Subscriber goes Off-Hook and is detected by the Ring Trip Detector ($\overline{RTDet}$) which immediately inhibits the $\overline{RINGSWT}$. The switches turn off automatically during zero current crossing as the sinusoidal ringing signal reverses the ringing current. The Feed Amplifiers power up only after the switches are turned off. A Zero Current Detection ($\overline{ZCD}$) signal after the command to turn off the switches is necessary before the Feed Amplifiers (PFA) can be activated. Once a valid Off-Hook occurs and the switches disconnected, the switches cannot be reconnected unless the control signal is changed from the RING mode to something else and then back to the RING mode. Furthermore, $\overline{SHD}$ is latched active low after Ring Trip until the part is switched to Loop Start, where the $\overline{SHDet}$ is used to monitor the loop status. Also, if $\overline{SHDet}$ is low prior to (and during) a RC, the logic will prevent the $\overline{RINGSWT}$ from being activated until $\overline{SHDet}$ goes inactive. This prevents ringing from being connected to an off hook line.

One thing to keep in mind, $\overline{SHDet}$ and $\overline{GKDet}$ are ignored when the PFA signal is high to prevent false operation.

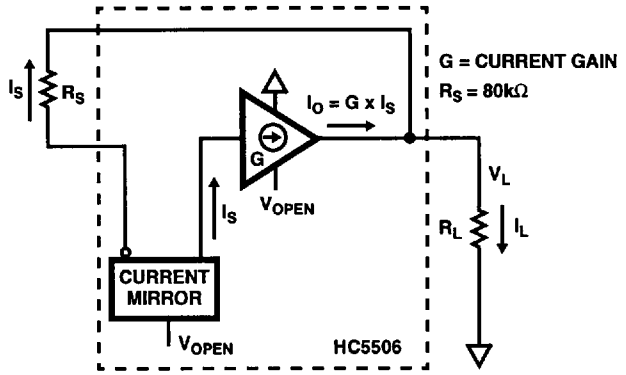
On Hook Transmission

The On Hook Transmission mode allows the transmission and reception of signals on the Subscriber line when there is no DC load present. The logic activates the offset current ($\overline{FOC}$) used to move Tip and Ring voltage positions from the supply rails, allowing AC transmission. Also, the OHT $\overline{SHD}$ threshold is selected so as to not cause inadvertent $\overline{SHD}$ due only to the offset of the Tip and Ring DC voltages.

Basic Operation

Battery Feed

The current feed architecture of the HC5506 offers advantages over a voltage feed arrangement. These include: longitudinal rejection capability is achieved by feedback which makes it independent of feed resistor mismatches, the DC feed resistance can be programmed in the feedback loop (this ability is not available in the HC5506), power dissipating components can be placed outside the device package and can be part of the DC feedback loop, and lower component count for supervisory functions. Figure 4 shows the single ended battery feed model for the HC5506.



$V_{OPEN} = V_{TIP\text{-}RING}$ open loop voltage

$$I_S = \frac{V_{OPEN} - V_L}{R_S}$$

$$I_L = G \times I_S + I_S = I_S \times (G+1)$$

$$\frac{I_L}{(G+1)} = I_S = \frac{V_{OPEN} - V_L}{R_S}$$

$$V_L = V_{OPEN} - \left(\frac{R_S}{G+1}\right) \times I_L$$

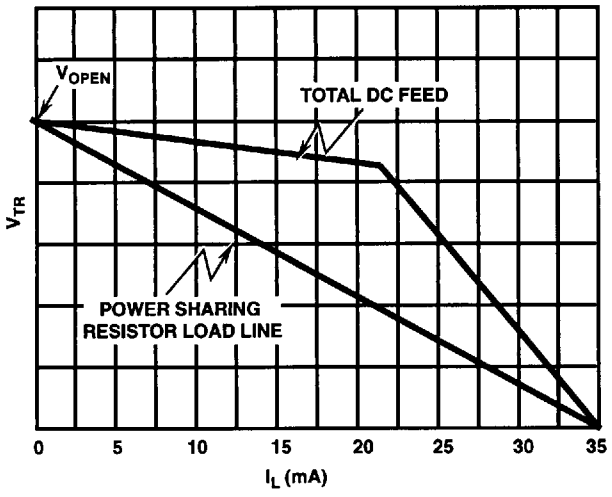
where

$$R_{FEED} = \frac{\Delta V_L}{\Delta I_L} = \frac{R_S}{G+1}$$

FIGURE 4. BATTERY FEED MODEL (SINGLE ENDED)

The V/I characteristics are shown in Figure 5. At currents below the current limit point, the DC feed circuit is equivalent to a battery voltage source V_{OPEN} and a feed resistance of approximately 400Ω (200 + 200).

From the Figure 5 equations, it is evident that the feed resistance is controlled by R_S, the external sense resistor. It is possible to modify the feed resistance by varying this value, but the architecture of the SLIC does not allow independent variation of this component without affecting other characteristics.



$\frac{R_S}{G+1}$ = DC Feed Resistance

$V_{OPEN} = V_{TIP-RING}$ open loop voltage

FIGURE 5. SLIC FEED CHARACTERISTIC (SINGLE ENDED)

DC Loop (see Figure 6)

The HC5506 uses a current feed/voltage sense architecture. As shown in Figure 6, the Tip voltage relative to ground and the Ring voltage relative to battery are sensed independently through two sense resistors (RS). By sensing the voltage with a resistor, a current proportional to the Tip and Ring voltage is developed (I_{TS} and I_{RS}). This current is divided by two and mirrored and DC filtered resulting in the currents ITdc and IRdc. These two currents are added and the resultant current is proportional to the difference between the battery voltage and the Tip-Ring voltage. This is then routed to the DC Feed Current Limiter which causes the V/I characteristic to current limit, with the SLIC behaving like a constant current source independent of the 2-Wire loop voltage. Finally, the output of the current limiter is mirrored to the Tip and Ring power amplifier separately, providing the DC Feed current to the 2-Wire loop.

Power Sharing

In order to reduce the power dissipated by the silicon and package, a parallel DC Feed arrangement is provided as shown in Figure 7.

A current sharing resistor (R_{PS}) is placed externally but still within the output amplifier closed loop configuration. For a given DC load, the SLIC DC feedback sets the load current and voltage conditions according to the Total DC Feed load line as show in Figure 5. However, the SLIC does not supply the total loop current to the load, a portion of the current is delivered through the power sharing resistors. The amount supplied by the power sharing resistors is determined by the voltage conditions and according to the Power Sharing Resistor Load line in Figure 5. The net current delivered by the SLIC is the difference current between the two load lines in Figure 5.

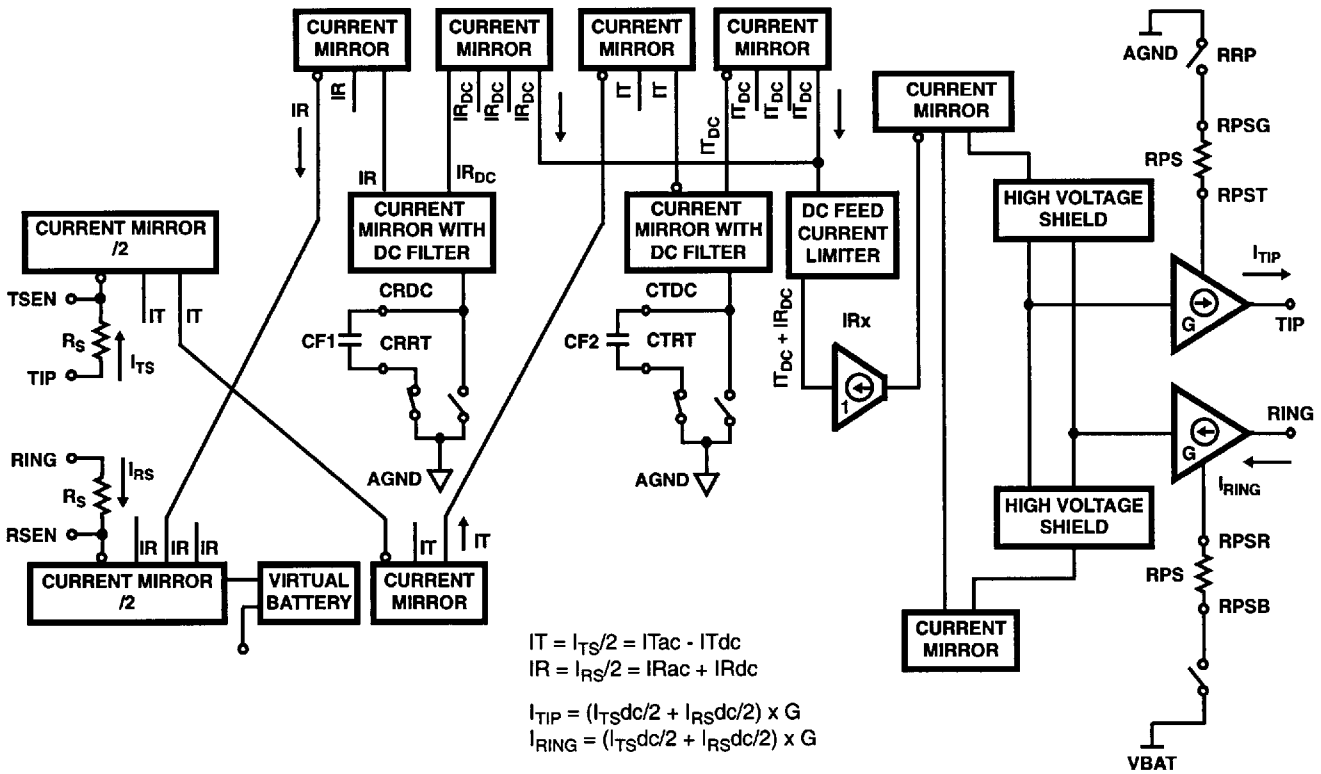


FIGURE 6. DC LOOP

In Figure 7, a switch is shown in series with the power sharing resistors. This allows Power Sharing to be disabled during fault conditions and while ringing the line.

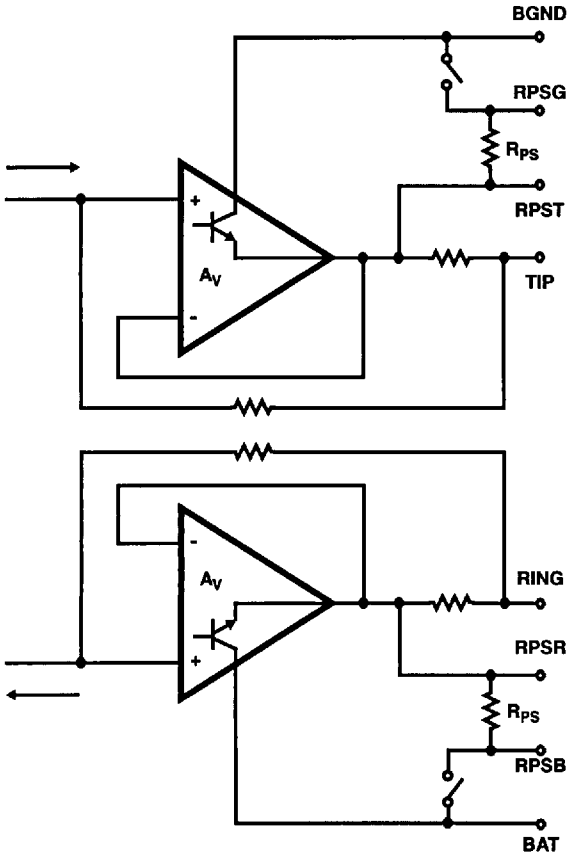


FIGURE 7. POWER SHARING IMPLEMENTATION

Transmission

Overview

Design Equations (Repeating)

$$A_{2-4} = \frac{RTX}{171.3k} \quad \text{(EQ. 1)}$$

$$RTX = 171.3k \times A_{2-4} \quad \text{(EQ. 2)}$$

$$Z_M = \frac{171.3k \times RZAC}{(RTX) \times 390} \quad \text{(EQ. 3)}$$

$$RZAC = \frac{(RTX) \times (Z_M) \times 390}{171.3k} \quad \text{(EQ. 4)}$$

$$A_{4-2} = \frac{-171.3k \times RZAC}{(RRX) \times (RTX)} \times \frac{1}{1 + \frac{Z_M}{Z_L}} \quad \text{(EQ. 5)}$$

$$RRX = \frac{171.3k\,(RZAC)}{(A_{4-2}) \times (RTX)} \times \frac{1}{1 + \frac{Z_M}{Z_L}} \quad \text{(EQ. 6)}$$

$$A_{4-4} = \frac{-RZAC}{RRX} \times \frac{1}{1 + \frac{Z_M}{Z_L}} \quad \text{(EQ. 7)}$$

where:

1. Z_M = Desired SLIC 2-Wire sythesized impedance
2. Z_L = 2-Wire Line Impedance

Transmission Example 1

Requirement:

A_{4-2} = -6.02dB = 0.5

A_{2-4} = 0dB = 1

Z_M = 600Ω = SLIC 2-Wire impedance

Z_B = 600Ω = 2-Wire termination for transhybrid balance

From Equation 2:

$$RTX = 171.3k \times A_{2-4} = 171.3k \times 1 = 171k\Omega$$

use169k, 1% standard value.

From Equation 4:

$$RZAC = \frac{Z_M \times RTX}{439} = \frac{Z_M \times 169k}{439} = 385 \times Z_M = = 385 \times 600$$

RZAC = 231k

use 232k, 1% standard value.

We designed for Z_M = 600Ω, but since we chose standard 1% resistor values:

$$Z_M = \frac{171.3k}{390} \times \frac{RZAC}{RTX} = \frac{171.3k}{390} \times \frac{232k}{169k} = 603\Omega$$

From Equation 6:

$$RRX = \frac{171.3 \times RZAC}{RTX \times A_{4-2}} \times \frac{Z_L}{Z_M + Z_L}$$

$$RRX = \frac{171.3k \times 232k}{169k \times 0.5} \times \frac{600}{603 + 600}$$

RRX = 234.6k

use 232k, 1% standard value.

Summarizing (using actual component values):

$$A_{2-4} = \frac{RTX}{171.3k} = \frac{169k}{171.3k} = 0.987 = -0.12dB$$

Z_M = 603Ω

$$|A_{4-2}| = \frac{171.3k \times RZAC}{RRX \times RTX} \times \frac{Z_L}{Z_M + Z_L}$$

$$|A_{4-2}| = \frac{171.3k \times 232k}{237k \times 169k} \times \frac{600}{1203} = 0.506$$

$|A_{4-2}|$ = -5.92dB

$$|A_{4-4}| = \frac{RZAC}{RRX} \times \frac{Z_L}{Z_M + Z_L} = \frac{232k}{232k} \times \frac{600}{603 + 600} = 0.499$$

$|A_{4-4}|$ = -6.04dB

Calculate Balance Network: (See Figure 8)

$$|A_{4-4}| \equiv \frac{V_{TX}}{V_{RX}}$$

Transhybrid balance requires

$$\frac{V_{RX}}{Z_B}+\frac{V_{TX}}{Z_T}=0\Rightarrow\frac{Z_T}{Z_B}=\frac{V_{TX}}{V_{RX}}=|A_{4-4}|$$

From Equation 7:

$$\frac{Z_T}{Z_B}=|A_{4-4}|=\frac{RZAC}{RRX}\left[\frac{Z_L}{Z_M+Z_L}\right]=0.499$$

$$Z_T=0.499Z_B$$

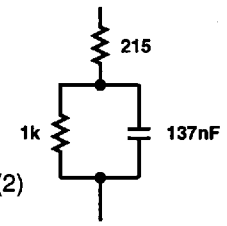
Use Z_T, $Z_B \geq 10k\Omega$ so as not to load the CODEC op amp.

let $Z_B = 20.5k\Omega$, then
$Z_T = 10.2k\Omega$,
and $Z_F = Z_T = 10.2k\Omega$

all standard 1% values.

Transmission Example 2

Requirement:
$A_{4-2} = 0dB$
$A_{2-4} = -7dB = 0.446684$
$Z_M = 215\Omega + 1000\Omega \parallel 137nF \Rightarrow$
$Z_{BALANCE} = Z_M$ (1); $Z_{BALANCE} = 600\Omega$ (2)



From Equation 2:

$RTX = (171.3k) \times (A_{2-4}) = (171.3k) \times (0.44668) = 76.5k\Omega$

RTX = 76.5kΩ

From Equation 4:

$$RZAC=\frac{Z_M\times RTX}{439}=Z_M\times\frac{76.5k}{439}=Z_M\times(174)$$

$$RZAC = 174\times Z_M = 174\,[215+1000\parallel 137n]$$

RZAC = 37.4kΩ + 174kΩ ∥ 787pF

From Equation 6:

$$RRX=\frac{171.3k\times RZAC}{RTX\times A_{4-2}}\times\frac{Z_L}{Z_M+Z_L}$$

$$=\frac{171.3k\times RZAC}{76.5k\times 1}\times\frac{1}{2}$$

$$X = 1.12\times RZAC = 1.12\,(37.4k+174k\,(179)\,k\parallel 787pF)$$

RRX = 41.9kΩ + 195kΩ ∥ 703pF

Transhybrid Balance (see Figure 8)

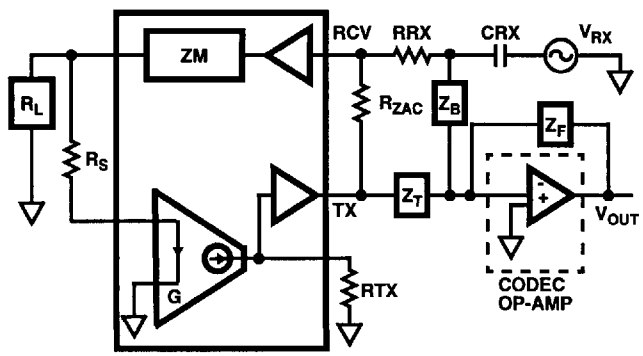


FIGURE 8. HYBRID FUNCTION

As before, from Equation 7

$$\frac{Z_T}{Z_B}=|A_{4-4}|=\frac{RZAC}{RRX}\left[\frac{Z_L}{Z_M+Z_L}\right]$$

but we found RRX = 1.12 RZAC thus,

$$\frac{Z_T}{Z_B}=\frac{1}{1.12}\left[\frac{Z_L}{Z_M+Z_L}\right]$$

Case 1: $Z_L = Z_{COMPLEX} = Z_M$

$$\frac{Z_T}{Z_B}=\frac{1}{1.12}\times\left[\frac{1}{2}\right]=0.4464=A_{4-4}$$

Also,

$$\left|\frac{Z_F}{Z_T}\right|=\frac{V_{OUT}}{V_{TX}}=1\Rightarrow Z_F=Z_T=0.4464Z_B$$

Select Z_T, Z_B and Z_F to satisfy these relationships.

Case 2: $Z_L = 600\Omega \neq Z_{COMPLEX}$

$$\frac{Z_T}{Z_B}=\frac{1}{1.12}\left[\frac{Z_L}{Z_M+Z_L}\right]$$

$$=\frac{1}{1.12}\times\left[\frac{600}{Z_M+600}\right]$$

$$\frac{Z_B}{Z_T}=\frac{1.12\,(Z_M+600)}{600}$$

Note:

$$Z_M = 215\Omega + 1000\Omega \parallel 137nF$$
$$= R_S + R_P \parallel C_P$$
$$Z_M=\frac{R_S+R_P+sR_PC_PR_S}{1+sR_PC_P}$$

thus,

$$\frac{Z_B}{Z_T}=\frac{1.12}{600}\left[\frac{R_S+R_P+sR_SR_PC_P+600\,(1+sR_PC_P)}{1+sR_PC_P}\right]$$

$$\frac{Z_B}{Z_T}=\frac{1.12}{600}\underbrace{\left[\frac{\overbrace{(R_S+600)}^{R_S'}+R_P+sR_PC_P\overbrace{(R_S+600)}^{R_S'}}{1+sR_PC_P}\right]}_{\text{same as } Z_M \text{ with } R_S'=R_S+600}$$

thus,

$$Z_B = Z_T\times\frac{1.12}{600}\times[R_S'+R_P\parallel C_P]$$

Select Balance Network Values

Choose $Z_T=\frac{600}{1.12}=536\times k$

where k is a scale factor, such that $Z_T > 10k\Omega$ to not load CODEC op amp.

If scaled by

$$k=\frac{76.5k}{439}=174.1\Rightarrow Z_T=93.2k\Omega, \text{ and}$$

$$Z_B=\begin{cases}R_S'=142k\Omega\\ R_P=174k\Omega\\ C_P=787pF, \text{ and}\end{cases}$$
$$Z_F = Z_T$$

Fault Conditions

The SLIC utilizes a thermal shutdown circuit to protect itself from excessive current flow. When the die temperature exceeds 150°C (nominally), the SLIC shuts down the drive to the feed amplifiers and enters a high impedance state similar to Wink Off. In this state, there is very little current flow and the die will begin to cool. When the die temperature then drops below 150°C, the SLIC will again power the feed amplifiers and should the fault condition still exist, excessive current will again flow and the die will heat up. This "oscillation" will continue until the fault condition is removed or the controller shuts down the SLIC. The frequency of the oscillation is a function of the fault condition and ambient temperature. Typical is a few hertz.

Prior to entering the high impedance state, the SLIC is capable of sourcing or sinking fault currents as given in the table below.

FAULT CONDITIONS	TYP	UNITS
$I_{TIP\ TO\ RING}$	38-80	mA
$I_{TIP\ TO\ GND}$ (See Note)	28-50	mA
$I_{RING\ TO\ GND}$ (See Note)	110-220	mA
$I_{TIP\ TO\ GND} + I_{RING\ TO\ GND}$	220	mA
$I_{TIP\ TO\ V_{BAT}}$ (See Note)	110-220	mA
$I_{RING\ TO\ V_{BAT}}$ (See Note)	30-50	mA
$I_{TIP\ TO\ GND} + I_{RING\ TO\ V_{BAT}}$ (See Note)	50	mA

NOTE: R_L = Open

Operation Notes

Ring Trip

To prevent latching of the ring switches from occurring, the SLIC should be Winked-Off after ring trip occurs for at least 30ms when using a 20Hz ringer. For other than 20Hz, use $t = T_{Ring} \times 1/2 + 5ms$. This guarantees that the ring switches have opened before the SLIC begins to feed the loop.

The sequence of events is shown in Figure 9. During interval 1, the SLIC is in the RING mode and the line is being rung. In 2 the subscriber has gone off-hook; the ringer current increases because the DC resistance of the set is much less than the ac impedance and there is a DC offset due to the battery offset of the ringer. Some time later, the SLIC detects the off-hook subscriber as shown in 3. At this point SHD is asserted (goes low). Once the controller acknowledges SHD, it should change the SLIC state to Wink-Off as show in 4. The SLIC should stay in this state for a minimum of 30ms to ensure that the ring switches have opened. Interval 5 begins 30ms later when the controller changes the SLIC state to Loop Start and the call proceeds normally.

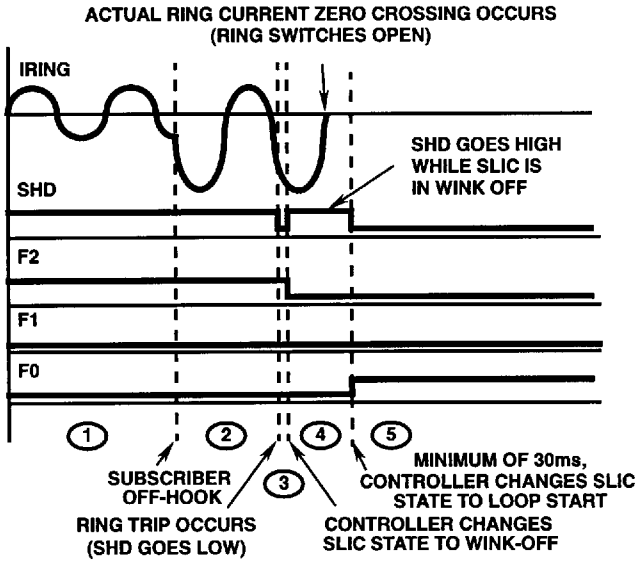
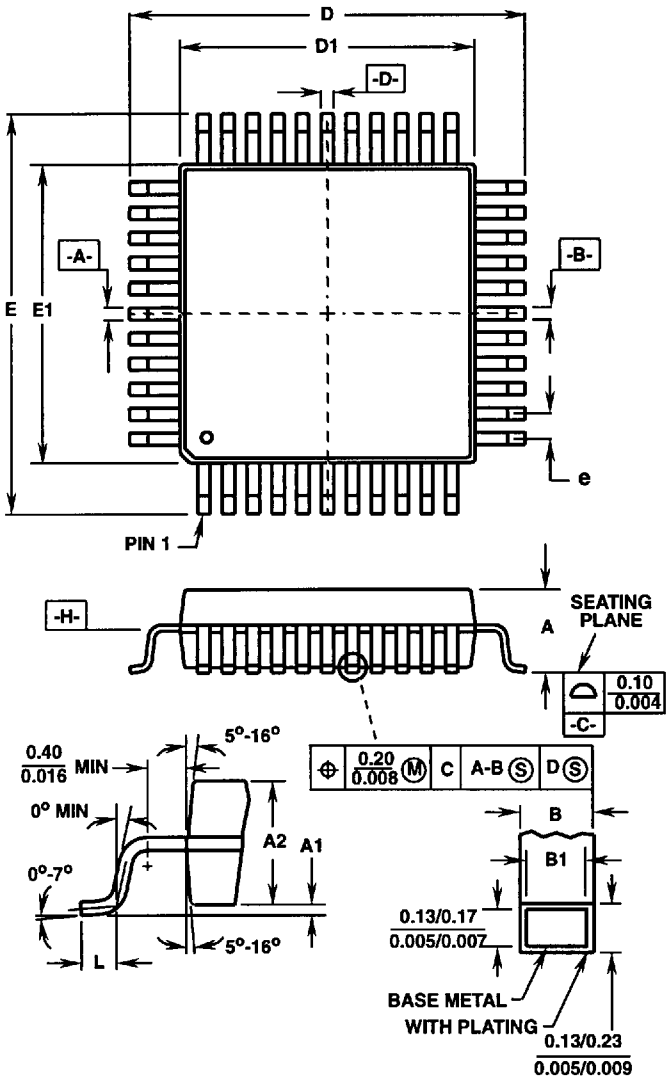


FIGURE 9. PROPER RING TRIP SEQUENCE

Dial Pulse Detect

In systems using pulse dialing the SLIC should idle in the On-Hook Transmission state, and should only go into Loop Start after dialing has completed. This optimizes the dial pulse distortion performance.

Metric Plastic Quad Flatpack Packages (MQFP)



Q80.14x20 (JEDEC MO-108CB-1 ISSUE A)
80 LEAD METRIC PLASTIC QUAD FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.134	-	3.40	-
A1	0.010	-	0.25	-	-
A2	0.100	0.120	2.55	3.05	-
B	0.012	0.018	0.30	0.45	6
B1	0.012	0.016	0.30	0.40	-
D	0.904	0.923	22.95	23.45	3
D1	0.783	0.791	19.90	20.10	4, 5
E	0.667	0.687	16.95	17.45	3
E1	0.547	0.555	13.90	14.10	4, 5
L	0.026	0.037	0.65	0.95	-
N	80		80		7
e	0.032 BSC		0.80 BSC		-
ND	24		24		-
NE	16		16		-

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NOTES:

1. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
2. All dimensions and tolerances per ANSI Y14.5M-1982.
3. Dimensions D and E to be determined at seating plane -C-.
4. Dimensions D1 and E1 to be determined at datum plane -H-.
5. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm (0.010 inch) per side.
6. Dimension B does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total.
7. "N" is the number of terminal positions.